Automotive, Programmable Stepper Driver

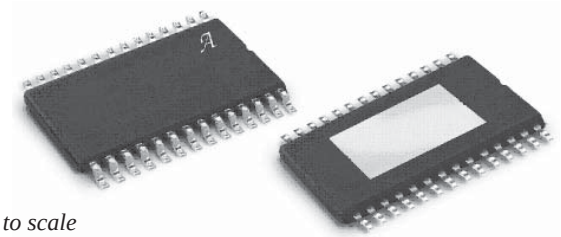
Features and Benefits

- Peak motor current up to ±1.4 A, 28 V
- Low $R_{DS(on)}$ outputs, 0.5 Ω source and sink, typical
- Automatic current decay mode detection/selection
- Mixed, Fast, and Slow current decay modes
- Synchronous rectification for low power dissipation
- Internal OVLO, UVLO, and Thermal Shutdown circuitry
- Crossover-current protection
- Short circuit, and open load diagnostics
- Hot and cold thermal warning
- Stall detect features
- SPI-compatible or simple Step and Direction motion control
- Highly configurable via SPI-compatible serial interface

Applications

- Automotive stepper motors
- Engine management
- Headlamp positioning

Package: 28-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

Description

The A4980 is a flexible microstepping motor driver with built-in translator for easy operation. It is a single-chip solution, designed to operate bipolar stepper motors in full-, half-, quarter- and sixteenth-step modes, at up to 28 V and ±1.4 A. The A4980 can be controlled by simple Step and Direction inputs, or through the SPI-compatible serial interface that also can be used to program many of the integrated features and to read diagnostic information.

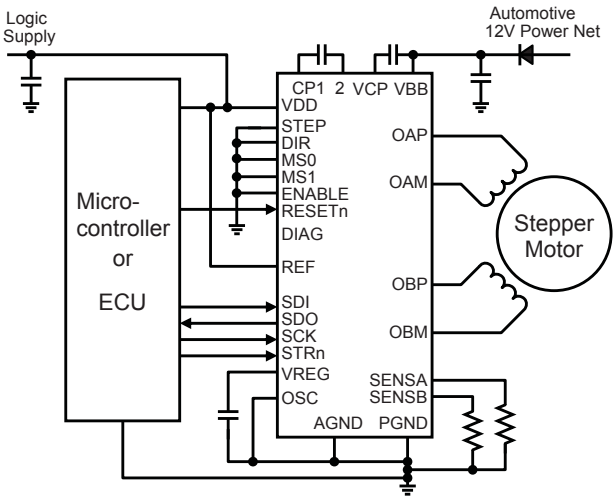
The current regulator can be programmed to operate in fixed off-time or fixed frequency PWM, with several decay modes to reduce audible motor noise and increase step accuracy. In addition the phase current tables can be programmed via the serial interface to create unique microstep current profiles to further improve motor performance for specific applications.

The current in each phase of the motor is controlled through a DMOS full bridge, using synchronous rectification to improve power dissipation. Internal circuits and timers prevent cross-conduction and shoot-through, when switching between high-side and low-side drives.

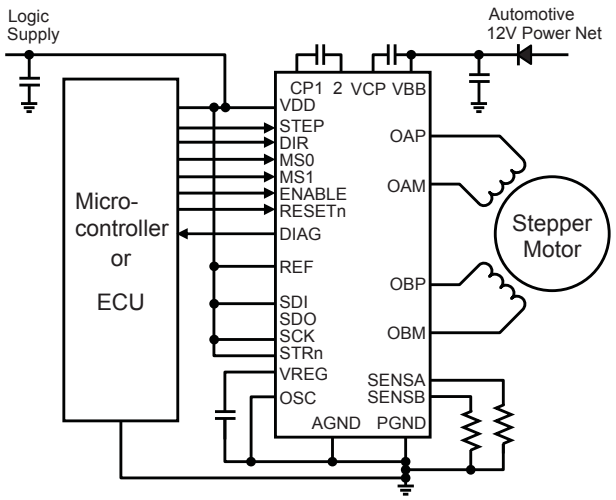
The outputs are protected from short circuits, and features for low load current and stalled rotor detection are included. Chip-level protection includes: hot and cold thermal warnings, overtemperature shutdown, and overvoltage and undervoltage lockout.

The A4980 is supplied in a 28-pin TSSOP power package with an exposed thermal pad (package type LP). This package is lead (Pb) free with 100% matte-tin leadframe plating.

Typical Applications



Serial Interface Control



Parallel Control

Selection Guide

Part Number	Packing*	
A4980KLP-T	50 pieces per tube	4.4 mm × 9.7 mm, 1.2 mm nominal height TSSOP with exposed thermal pad
A4980KLPTR-T	4000 pieces per reel	

*Contact Allegro® for additional packing options

Absolute Maximum Ratings With respect to GND

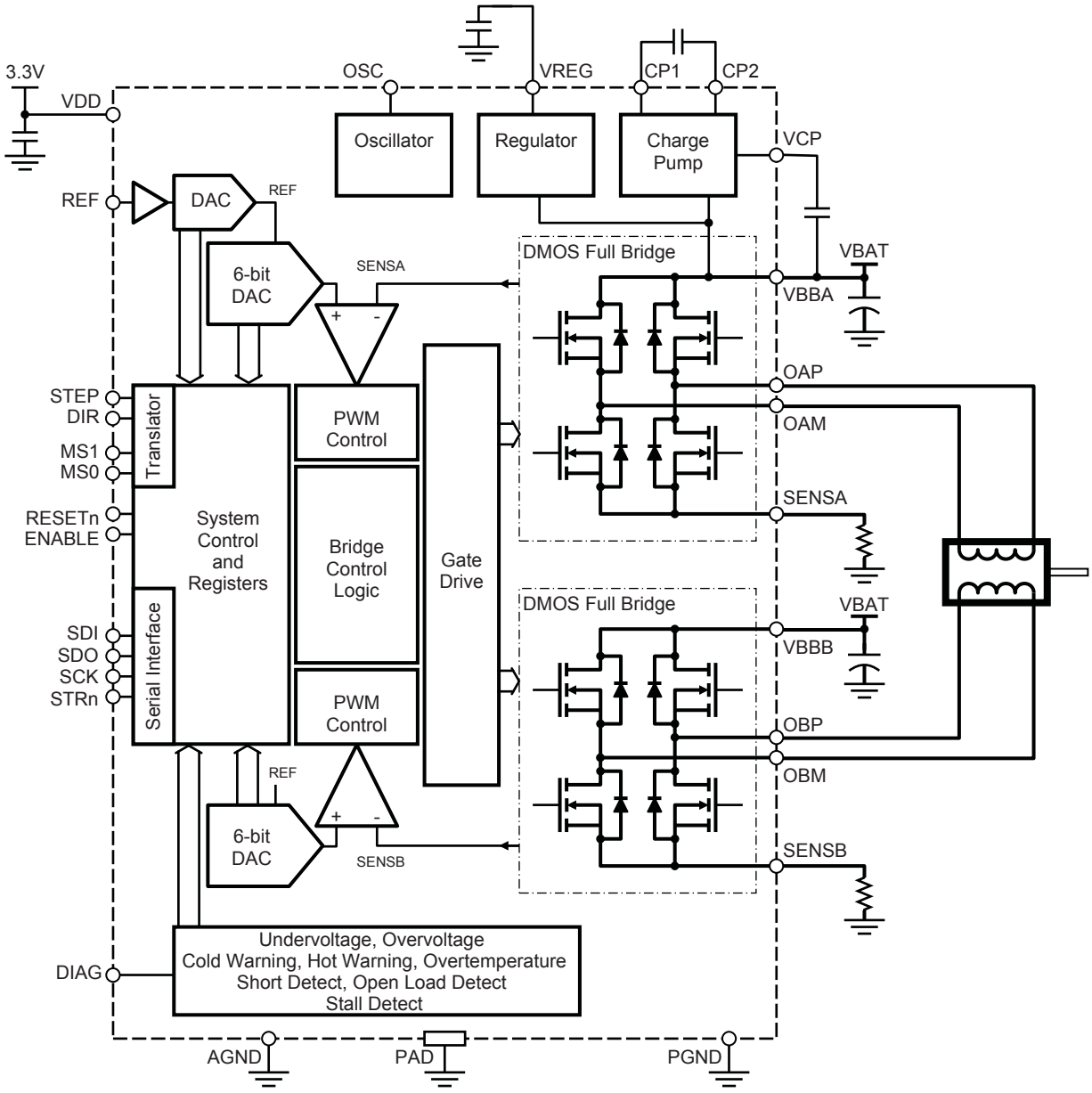
Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BBx}	Applies to V_{BBA} and V_{BBB}	–0.3 to 50	V
Logic Supply Voltage	V_{DD}		–0.3 to 6	V
Pin CP1			–0.3 to V_{BB}	V
Pins CP2, VCP			–0.3 to V_{BB}+8	V
Pins STEP, DIR, ENABLE, DIAG			–0.3 to 6	V
Pin VREG			–0.3 to 8.5	V
Pin RESETn		Can be pulled to V_{BB} with 38 kΩ	–0.3 to 6	V
Pin OSC			–0.3 to 6	V
Pins MS0, MS1			–0.3 to 6	V
Pins SDI, SDO, SCK, STRn			–0.3 to 6	V
Pin REF			–0.3 to 6	V
Pins OAP, OAM, OBP, OBM			–0.3 to V_{BB}	V
Pins SENSA, SENSB			–0.3 to 1	V
Ambient Operating Temperature Range	T_A	Range K; limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	T_J(max)		150	°C
Transient Junction Temperature	T_{tJ}	Overtemperature event not exceeding 10 s, lifetime duration not exceeding 10 hours, guaranteed by design and characterization	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

Thermal Characteristics may require derating at maximum conditions

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	28	ºC/W
		2-layer PCB with 24.52 cm^2 of copper area each side	32	ºC/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	ºC/W

*Additional thermal information available on the Allegro website

Functional Block Diagram



ELECTRICAL CHARACTERISTICS[1,2] Valid at T_J = –40°C to 150°C, V_{BB} = 6 to 28 V, V_{DD} = 3.3 V; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supplies						
Load Supply Voltage Range[3]	V_{BB}	Functional	0	–	50	V
		Outputs Driving	3.3	–	V_{BBOV}	V
Load Supply Quiescent Current	I_{BBQ}	ENABLE = 0	–	–	4	mA
		Sleep mode	–	1	10	µA
Logic Supply Voltage Range	V_{DD}		3	–	5.5	V
Logic Supply Quiescent Current	I_{DDQ}	ENABLE = 0	–	–	5	mA
		Sleep mode	–	4	15	µA
Charge Pump Voltage	V_{CP}	With repect to VBB, V_{BB} >7.5 V, ENABLE = 0, RESETn = 1	–	6.7	–	V
Internal Regulator Voltage	V_{REG}	ENABLE = 0, RESETn = 1, V_{BB} > 7.5 V	–	7.2	–	V
Internal Regulator Dropout Voltage	V_{REGDO}	ENABLE = 0, RESETn = 1, V_{BB} > 3.5 V	–	100	200	mV
Motor Bridge Output						
High-Side On-Resistance	R_{ONH}	V_{BB} = 13.5 V, I_{OUT} = –1 A, T_J = 25°C	–	500	600	mΩ
		V_{BB} = 13.5 V, I_{OUT} = –1 A, T_J = 150°C	–	900	1100	mΩ
		V_{BB} = 7 V, I_{OUT} = –1 A, T_J = 25°C	–	625	750	mΩ
High-Side Body Diode Forward Voltage	V_{FH}	I_F = 1 A	–	–	1.4	V
Low-Side On-Resistance	R_{ONL}	V_{BB} = 13.5 V, I_{OUT} = 1 A, T_J = 25°C	–	500	600	mΩ
		V_{BB} = 13.5 V, I_{OUT} = 1 A, T_J = 150°C	–	900	1100	mΩ
		V_{BB} = 7 V, I_{OUT} = 1 A, T_J = 25°C	–	625	750	mΩ
Low-Side Body Diode Forward Voltage	V_{FL}	I_F = –1 A	–	–	1.4	V
Output Leakage Current	I_{LO}	ENABLE = 0, RESETn = 1, V_O = V_{BB}	–120	–65	–	µA
		ENABLE = 0, RESETn = 1, V_O = 0 V	–200	–120	–	µA
		ENABLE = 0, RESETn = 0, V_O = V_{BB}	–	<1.0	20	µA
		ENABLE = 0, RESETn = 0, V_O = 0 V	–20	<1.0	–	µA
Current Control						
Internal Oscillator Frequency	f_{OSC}	OSC = AGND	3.2	4	4.8	MHz
		51 kΩ from OSC to VDD	3.6	–	4.4	MHz
External Oscillator Frequency Range	f_{EXT}		3	–	5	MHz
Blank Time[4]	t_{BLANK}	Default Blank-Time	–	1500	–	ns
Off-Time (In Fixed Off-Time Mode)[4]	t_{OFF}	Default Off-Time	–	44	–	µs
PWM Frequency (In Fixed Frequency Mode)[4]	f_{PWM}	Default PWM Frequency	–	16.7	–	kHz
Fast Decay Time[4]	t_{FAST}	Default Fast Decay Time	–	8	–	µs
Reference Input Voltage	V_{REF}		0.8	–	2	V
Internal Reference Voltage	V_{REFint}	REF tied to VDD	1.1	1.2	1.3	V

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ELECTRICAL CHARACTERISTICS[1,2] (continued) Valid at T_J = –40°C to 150°C, V_{BB} = 6 to 28 V, V_{DD} = 3.3 V; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Control (continued)						
Reference Input Current	I_{REF}		–3	0	3	µA
Maximum Sense Voltage	V_{SMAX}		–	125	–	mV
Current Trip Point Error[5]	E_{ITrip}	V_{REF} = 2 V, MxI0 = MxI1 = 1	–	–	±5	%
Logic Input And Output – DC Parameters						
Input Low Voltage	V_{IL}		–	–	$0.3 \times V_{DD}$	V
Input High Voltage	V_{IH}		$0.7 \times V_{DD}$	–	–	V
Input Hysteresis	V_{Ihys}		250	500	–	mV
Input Current (Except RESETn)	I_{IN}	$0 V < V_{IN} < V_{DD}$	–1	–	1	µA
Input Pull-Down Resistor (RESETn)	R_{PD}		–	50	–	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 2 mA	–	0.2	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –2 mA	V_{DD}–0.4	V_{DD}–0.2	–	V
Output Leakage (SDO)	I_O	$0 V < V_O < V_{DD}$, STRn = 1	–1	–	1	µA
Logic Input And Output – Dynamic Parameters						
Reset Pulse Width	t_{RST}		0.2	–	4.5	µs
Reset Shutdown Width	t_{RSD}		10	–	–	µs
Input Pulse Filter Time (STEP, DIR)	t_{PIN}		–	35	–	ns
Clock High Time	t_{SCKH}	A in figure 1	50	–	–	ns
Clock Low Time	t_{SCKL}	B in figure 1	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in figure 1	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in figure 1	30	–	–	ns
Strobe High Time	t_{STRH}	E in figure 1	300	–	–	ns
Data Out Enable Time	t_{SDOE}	F in figure 1	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in figure 1	–	–	30	ns
Data Out Valid Time from Clock Falling	t_{SDOV}	H in figure 1	–	–	40	ns
Data Out Hold Time from Clock Falling	t_{SDOH}	I in figure 1	5	–	–	ns
Data In Set-Up Time to Clock Rising	t_{SDIS}	J in figure 1	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	K in figure 1	10	–	–	ns
STEP Rising to STRn Rising Setup Time	t_{SPS}	L in figure 1, only when D15 = 1 and D14 = 0	100	–	–	ns
STEP Rising from STRn Rising Hold Time	t_{SPH}	M in figure 1, only when D15 = 1 and D14 = 0	300	–	–	ns
Step High Time	t_{STPL}		1	–	–	µs
Step Low Time	t_{STPH}		1	–	–	µs
Setup Time Control Input Change to STEP	t_{SU}	MS1, MS2, DIR	200	–	–	ns
Hold Time Control Input Change from STEP	t_H	MS1, MS2, DIR	200	–	–	ns
Wake-Up from RESET	t_{EN}		–	–	1	ms

Continued on the next page…

ELECTRICAL CHARACTERISTICS[1,2] (continued) Valid at T_J = –40°C to 150°C, V_{BB} = 6 to 28 V, V_{DD} = 3.3 V; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Diagnostics and Protection						
VBB Overvoltage Threshold	V_{BBOV}	V_{BB} rising	32	34	36	V
VBB Overvoltage Hysteresis	$V_{BBOVHys}$		2	–	4	V
VBB Undervoltage Threshold	V_{BBUV}	V_{BB} falling	5.2	5.5	5.8	V
VBB Undervoltage Hysteresis	V_{BBHys}		500	760	–	mV
VREG Undervoltage Threshold – High	V_{REGUVH}	V_{REG} falling	4.6	4.8	4.95	V
VREG Undervoltage Hysteresis – High	$V_{RGUVHHys}$		250	370	–	mV
VREG Undervoltage Threshold – Low	V_{REGUVL}	V_{REG} falling	2.85	3	3.15	V
VREG Undervoltage Hysteresis – Low	$V_{RGUVLHys}$		100	230	–	mV
VDD Undervoltage Threshold	V_{DDUV}	V_{DD} falling	2.6	–	2.9	V
VDD Undervoltage Hysteresis	$V_{DDUVHys}$		50	100	–	mV
OSC Timeout	t_{WD}	Bit 13 = 1	0.5	1	1.5	µs
High-Side Overcurrent Threshold	I_{OCH}	Sampled after t_{SCT}	1.4	2.05	2.65	A
High-Side Current Limit	I_{LIMH}	Active during t_{SCT}	3	5.5	8	A
Low-Side Overcurrent Sense Voltage	V_{OCL}	Sampled after t_{SCT}	210	250	290	mV
Overcurrent Fault Delay	t_{SCT}	Default Fault Delay	1500	2000	2700	ns
Open Load Current Threshold Error	E_{IOC}	V_{REF} = 2 V, Mx0 = Mx1 = 1	–	–	±10	%
Temperature Voltage Output Offset	V_{TO}	Temperature output selected on DIAG pin	–	1440	–	mV
Temperature Voltage Output Slope	A_T		–	–3.92	–	mV/°C
Cold Temperature Warning Threshold	T_{JWC}	Temperature decreasing	–20	–10	0	ºC
Cold Temperature Warning Hysteresis	T_{JWChys}		–	15	–	ºC
Hot Temperature Warning Threshold	T_{JWH}	Temperature increasing	125	135	145	ºC
Hot Temperature Warning Hysteresis	T_{JWHhys}		–	15	–	ºC
Overtemperature Shutdown Threshold	T_{JF}	Temperature increasing	155	170	–	ºC
Overtemperature Hysteresis	T_{Jhys}	Recovery = T_{JF} – T_{Jhys}	–	15	–	ºC

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2]All references to "VBB" apply to VBBA and VBBB.
[3]Function is correct but parameters are not guaranteed above or below the general limits (6 to 28 V). Outputs not operational above V_{BBOV} or below V_{REGUVL}.
[4]Assumes 4 MHz clock.
[5]Current Trip Point Error is the difference between actual current trip point and the target current trip point, referred to maximum full scale (100%) current: $E_{itrip} = 100 \times [I_{trip}(actual) – I_{trip}(target)] / I_{fullscale}$ (%).

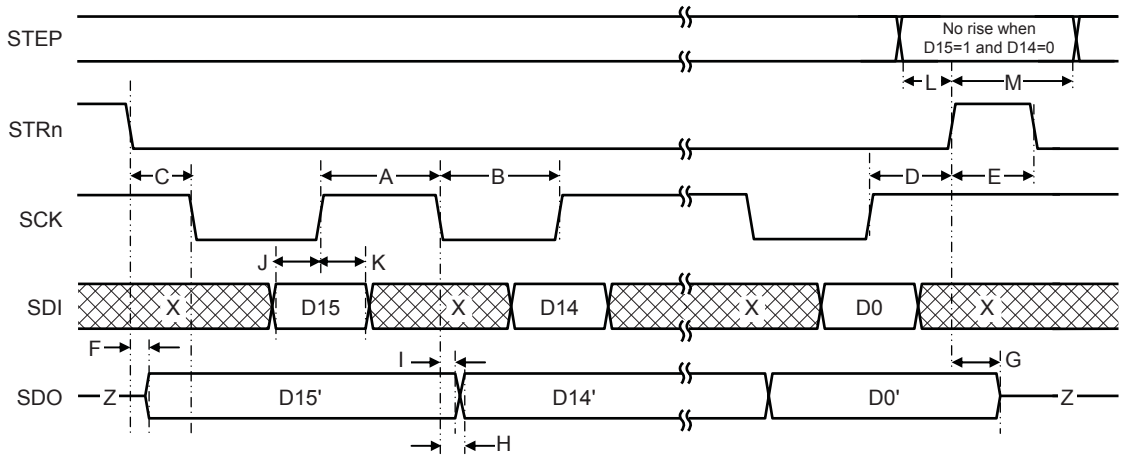


Figure 1. Serial Interface Timing Diagram

Key	Characteristic	Key	Characteristic
A	Clock High Time	H	Data Out Valid Time from Clock Falling
B	Clock Low Time	I	Data Out Hold Time from Clock Falling
C	Strobe Lead Time	J	Data In Set-Up Time to Clock Rising
D	Strobe Lag Time	K	Data In Hold Time From Clock Rising
E	Strobe High Time	L	STEP Rising to STRn Rising Setup Time
F	Data Out Enable Time	M	STEP Rising from STRn Rising Hold Time
G	Data Out Disable Time	X	“Don’t care”
		Z	High-impedance (tristate)

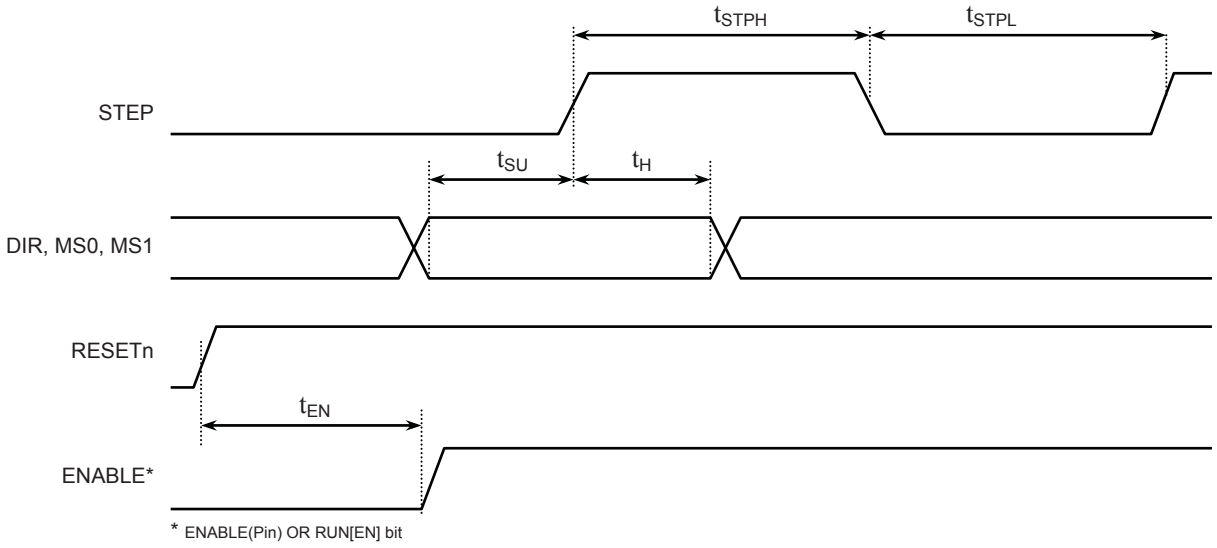


Figure 2. Control Input Interface Timing Diagram

Functional Description

The A4980 is an automotive stepper motor driver suitable for high temperature applications such as headlamp bending and leveling, throttle control, and gas recirculation control. It is also suitable for other low current stepper applications such as air conditioning and venting. It provides a highly flexible microstepping motor driver that can be configured via the SPI-compatible serial interface. It can be controlled with simple Step and Direction inputs, for high speed stepping applications, or directly through the serial interface by writing a step change value.

The two DMOS full bridges are capable of driving bipolar stepper motors in full-, half-, quarter-, eighth- and sixteenth-step modes, at up to 28 V and ±1.4 A. The current in each phase of the stepper motor is regulated by a peak detect PWM current control scheme that can be programmed to operate in fixed off-time or fixed frequency. Several decay modes can be selected to reduce audible motor noise and increase step accuracy. In addition the phase current tables, which default to a sinusoidal current profile, can be programmed via the serial interface to create unique microstep current profiles to further improve motor performance for specific applications.

The outputs are protected from short circuits, and features for open load and stalled rotor detection are included. Chip level protection includes hot and cold thermal warning, overtemperature shutdown, and overvoltage and undervoltage lockout.

Pin Functions

VBBA, VBBB Main motor supply and chip supply for internal regulators and charge pump. VBBA and VBBB should be connected together and each decoupled to ground with a low ESR electrolytic capacitor and a good ceramic capacitor.

Note: Any reference to “VBB” in this specification is defined as applying to both VBBA and VBBB.

CP1, CP2 Pump capacitor connection for charge pump. Connect a 100 nF (50 V) ceramic capacitor between CP1 and CP2.

VCP Above-supply voltage for high-side drive. A 100 nF (16 V) ceramic capacitor should be connected between VCP and VBB to provide the pump storage reservoir.

VDD Logic supply. Compatible with 3.3 V and 5 V logic. Should be decoupled to ground with a 100 nF (10 V) ceramic capacitor.

VREG Regulated supply for bridge gate drive. Should be decoupled to ground with a 470 nF (10 V) ceramic capacitor.

AGND Analog reference ground. Quiet return for measurement and input references. Connect to PGND (see Layout section).

PGND Digital and power ground. Connect to supply ground and AGND (see Layout section).

OAP, OAM Motor connection for phase A. Positive motor phase current direction is defined as flowing from OAM to OAP.

OBP, OBM Motor connection for phase B. Positive motor phase current direction is defined as flowing from OBM to OBP.

SENSA Phase A current sense. Connect sense resistor between SENSA and PGND.

SENSB Phase B current sense. Connect sense resistor between SENSB and PGND.

REF Reference input to set absolute maximum current level for both phases. Defaults to internal reference when tied to VDD.

STEP Step logic input. Motor advances on rising edge. Filtered input with hysteresis.

DIR Direction logic input. Direction changes on the next STEP rising edge. When high, the Phase Angle Number is increased on the rising edge of STEP. Has no effect when using the serial interface. Filtered input with hysteresis.

MS0 Microstep resolution select input.

MS1 Microstep resolution select input.

RESETn Resets faults when pulsed low. Forces low-power shutdown (sleep) when held low for more than the Reset Shutdown Width, t_{RSD}. Can be pulled to VBB with 30 kΩ resistor.

ENABLE Controls activity of bridge outputs. When held low, deactivates the outputs, that is, turns off all output bridge FETs. Internal logic continues to follow input commands.

SDI Serial data input. 16-bit serial word input MSB first.

SDO Serial data output. High impedance when STRn is high. Outputs bit 15 of the diagnostic registers (Fault Register 0 and Fault Register 1), the Fault Register flag, as soon as STRn goes low.

SCK Serial interface clock. Data is latched in from SDI on the rising edge of the SCK clock signal. There must be 16 rising edges per write and SCK must be held high when STRn changes.

STRn Serial data strobe and serial access enable. When STRn is high any activity on SCK or SDI is ignored, and SDO is high

impedance allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

DIAG Diagnostic output. Function selected via the serial interface, setting Configuration Register 1. Default is Fault output.

OSC With bit 13 in Configuration Register 1 set to 0, either connect this pin to AGND to use the internal oscillator running at the default frequency of 4 MHz, or connect a resistor to VDD to set the internal oscillator frequency. (The approximate frequency is calculated from:

$$f_{OSC} = 10\,000 / (48\,R_{OSC} - 20)$$

where f_{OSC} is the internal oscillator frequency in MHz, and R_{OSC} is the value, in kΩ of the resistor between OSC and VDD.)

If bit 13 in Configuration Register 1 is set to 1, then OSC is the input for an external system clock, which must have a frequency between 3 and 5 MHz. In this mode a watchdog is provided to detect loss of the system clock. If the OSC pin remains high or low for more than the watchdog time, t_{WD}, 1 µs typical, then the Fault Register flag (bit 15 in the diagnostic registers) is set and the outputs are disabled until the clock restarts.

Driving a Stepper Motor

A two-phase stepper motor is made to rotate by sequencing the relative currents in each phase. In its simplest form, each phase is simply fully energized in turn by applying a voltage to the winding. For more precise control of the motor torque over temperature and voltage ranges, current control is required. For efficiency this is usually accomplished using pulse width modulation (PWM) techniques. In addition current control also allows the relative current in each phase to be controlled, providing more precise control over the motor movement and hence improvements in torque ripple and mechanical noise. Further details of stepper motor control are provided in Appendix 1.

For bipolar stepper motors the current direction is significant, so the voltage applied to each phase must be reversible. This requires the use of a full bridge (also known as an H-bridge) which can switch each phase connection to supply or to ground.

Phase Current Control

In the A4980, current to each phase of the two-phase bipolar stepper motor is controlled through a low impedance N-channel DMOS full bridge. This allows efficient and precise control of the phase current using PWM switching. The full-bridge configuration provides full control over the current direction during the PWM on-time, and over the current decay mode during the PWM off-time. Due to the flexibility of the A4980 these control techniques can be completely transparent to the user or can be partially- or fully-programmed through the serial interface.

Each leg (high-side, low-side pair) of a bridge is protected from shoot-through by a fixed dead time. This is the time between switching off one FET and switching on the complementary FET. Cross-conduction is prevented by lock-out logic in each driver pair.

The phase currents and in particular the relative phase currents are defined in the Phase Current table (table 7). This table defines the two phase currents at each microstep position. For each of the two phases, the currents are measured using a sense resistor, R_S, with voltage feedback to the respective SENSx pin. The target current level is defined by the voltage from the digital-to-analog converter (DAC) for that phase. The sense voltage is amplified by a fixed gain and compared to the output of the DAC.

There are two types of *maximum current*: the absolute maximum, I_{SMAX}, the maximum possible current defined by the sense resistor and the reference input; and the phase maximum, I_{PMAX}, the maximum current delivered to a motor phase.

The absolute maximum current, I_{SMAX}, is defined as:

$$I_{SMAX} = V_{REF} / (16 \times R_S)$$

where V_{REF} is the voltage at the REF pin, and R_S is the sense resistor value.

The phase maximum, I_{PMAX}, is the 100% reference level for the phase current table and may be a fraction of the absolute maximum current, I_{SMAX}, depending on the value of the MXI0 and MXI1 bits in Configuration Register 0.

For example:

- if R_S = 180 mΩ and V_{REF} = 2 V, then I_{SMAX} = 694 mA
- if MXI1= 1 and MXI0 = 0, then I_{PMAX} = 520 mA

The actual current delivered to each phase at each Step Angle Number is determined by the value of I_{PMAX} and the contents of the Phase Current table. For each phase, the value in the table is passed to the DAC, which uses I_{PMAX} as the reference 100% level (code 63) and reduces the current target depending on the DAC code. The output from the DAC is used as the input to the current comparators.

The current comparison is ignored at the start of the PWM on-time for a duration referred to as the *blank time*. The blank time is necessary to prevent any capacitive switching currents from causing a peak current detection.

The PWM on-time starts at the beginning of each PWM period. The current rises in the phase winding until the sense voltage reaches the required current level. At this point the PWM off-time

starts and the bridge is switched into one of two decay modes, slow decay or fast decay:

- Slow decay is most effective when the current is rising from step to step. and it occurs when the phase winding is effectively shorted by switching-on either both high-side FETs or both low-side FETs in the full bridge.
- Fast decay is most effective when the current is falling from step to step, and it occurs when the voltage on the phase is reversed.

One disadvantage of fast decay is the increased current ripple in the phase winding. However, this can be reduced while maintaining good current control, by using a short time of fast decay followed by slow decay for the remainder of the PWM off-time. This technique is commonly referred to as *mixed* decay.

The A4980 provides two methods to determine the PWM frequency: fixed off-time and fixed frequency. At power-up the default mode is fixed off-time. Fixed frequency can be selected through the serial interface. Fixed off-time provides a marginal improvement in current accuracy over a wide range of current levels. Fixed frequency provides a fixed fundamental frequency to allow more precise supply filtering for EMC reduction. In both cases the PWM off-time will not be present if the peak current limit is not attained during the PWM on-time.

Phase Current Table

The relative phase currents are defined by the Phase Current table. This table contains 64 lines and is addressed by the Step Angle Number, where Step Angle Number 0 corresponds to 0° or 360°. The Step Angle Number is generated internally by the step sequencer, which is controlled either by the STEP and DIR inputs or by the step change value from the serial input. The Step Angle Number determines the motor position within the 360° electrical cycle and a sequence of Step Angle Numbers determines the motor movement. Note that there are four full mechanical steps per 360° electrical cycle.

Each line of the Phase Current table (table 7) has a 6-bit value per phase to set the DAC level for that phase, plus an additional bit per phase to determine the current direction for that phase. The Step Angle Number sets the electrical angle of the stepper motor in one-sixteenth microsteps, approximately equivalent to electrical steps of 5.625°.

On first power-up or after a VDD power-on reset, the Phase Current table values are reset to define a sinusoidal current profile and the Step Angle Number is set to 8, equivalent to the electrical cycle 45° position. This position is defined as the “home” position. The maximum current in each phase, I_{PMAX}, is defined by the sense resistor and the Maximum Current setting (bits MXI[0..1]) in Configuration Register 0. The phase currents for each entry in the Phase Current table are expressed as a percentage of this maximum phase current.

When using the STEP and DIR inputs to control the stepper motor, the A4980 automatically increases or decreases the Step Angle Number according to the step sequence associated with the selected step mode. The default step mode, reset at power-up or after a power on reset, is full step. Half-, quarter-, and sixteenth-step sequences are also available when using the STEP and DIR inputs, and are selected using the logical OR of the MS0 and MS1 inputs and the MS0 and MS1 bits in Configuration Register 0. The eighth-step sequence is shown in the Phase Current table for reference only.

When using the serial interface to control the stepper motor, a step change value (6-bit) is input through the serial interface to increase or decrease the step angle. The step change value is a two’s complement (2’sC) number, where a positive value increases the step angle and a negative value decreases the Step Angle Number. A single step change in the Step Angle Number is equivalent to a single one-sixteenth microstep. Therefore, for correct motor movement, the step change value should be restricted to no greater than 16 steps, positive or negative.

This facility enables full control of the stepper motor at any microstep resolution up to and including sixteenth-step, plus the ability to change microstep resolution “on-the-fly” from one microstep to the next.

In both control input method cases, the resulting Step Angle Number is used to determine the phase current value and current direction for each phase, based on the Phase Current table. The decay mode is determined by the position in the Phase Current table and the intended direction of rotation of the motor.

Diagnostics

The A4980 integrates a number of diagnostic features to protect the driver and load as far as possible from fault conditions and extreme operating environments. At the system level the supply voltages and chip temperature are monitored. A number of these features automatically disable the current drive to protect the outputs and the load. Others only provide an indication of the likely fault status, as shown in the Fault table (table 1). A single diagnostic output pin (DIAG) can be programmed through the serial interface to provide several different internal signals. At power-up, or after a power-on-reset the DIAG pin outputs a simple Fault Output flag which will be low if a fault is present. The Fault Output flag remains low while the fault is present or if

one of the latched faults (for example, a bridge short circuit) has been detected and the outputs disabled.

Alternative to the Fault Output flag, the DIAG output can be programmed via the serial interface to output: the stall detect signal, which goes low when a stall is detected; the phase A PWM-on signal, which is high during the phase A PWM on-time; or an analog signal indicating the silicon temperature.

If required, specific fault information can be determined by reading the diagnostic registers (see Serial Interface section).

The first bit (bit 15) in both diagnostic registers contains a common Fault Register flag which will be high if any of the fault bits in either register has been set. This allows a fault condition to be detected using the serial interface, by simply taking STRn low. As soon as STRn goes low the fist bit in the diagnostic registers can be read to determine if a fault has been detected at any time since the last diagnostic registers reset. In all cases the fault bits in the diagnostic registers are latched and only cleared after a diagnostic registers reset.

Note that the Fault Register flag in the diagnostic registers, does not provide the same function as the Fault Output flag on the DIAG pin. The Fault Output flag on the DIAG pin provides an indication that either a fault is present or the outputs have been disabled due to a short circuit fault. The Fault Register flag simply provides an indication that a fault has occurred since the last diagnostic registers reset and has been latched.

Table 1. Fault Table

Diagnostic	Action	Latched
VBB Overvoltage	Disable outputs, set Fault Register flag	No
VBB Undervoltage	Set Fault Register flag	No
VREG Undervoltage	Disable outputs, set Fault Register flag	No
VDD Undervoltage	Power-down, full reset	No
Temperature Warning	Set Fault Register flag	No
Overtemperature	Disable outputs, set Fault Register flag	No
Bridge Short	Disable outputs, set Fault Register flag	Yes
Bridge Open	Set Fault Register flag	No
Stall Detect	Set ST flag	No

At the system level the supply voltages and chip temperature are monitored.

Supply Voltage Monitors

The logic supply, the motor supply, and the regulator output are monitored: the motor supply for overvoltage, and the regulator output and logic supply for undervoltage.

- If the motor supply voltage, V_{BBA} and V_{BBB}, goes above the VBB overvoltage threshold, the A4980 will disable the outputs and indicate the fault. When the motor supply voltage goes below the VBB overvoltage threshold, the outputs will be re-enabled and the fault flag removed. The fault bits in the diagnostic registers remain set until cleared by a diagnostic registers reset.
- If the motor supply voltage, V_{BBA} and V_{BBB}, goes below the VBB undervoltage threshold, the A4980 will indicate the fault and reduce the VREG undervoltage threshold to the low level. When the motor supply voltage goes above the VBB undervoltage threshold, the VREG undervoltage threshold will be increased to the high level and the fault flag removed. The fault bits in the diagnostic registers remain set until cleared by a diagnostic registers reset.
- If the output of the internal regulator, V_{REG}, goes below the VREG undervoltage threshold, the A4980 will disable the outputs and indicate the fault. When the regulator output rises above the VREG undervoltage threshold, the outputs will be re-enabled and the fault flag removed. The fault bits in the diagnostic registers remain set until cleared by a diagnostic registers reset.
- If the logic supply voltage, V_{DD}, goes below the VDD undervoltage threshold, the A4980 will be completely disabled except to monitor the V_{DD} voltage level. When the logic supply voltage rises above the VDD undervoltage threshold, a power-on reset will take place and all registers will be reset to the default state.

Note that both the VREG undervoltage monitor and the V_{BB} undervoltage monitor indicate a fault by using the same fault bit, UV, in both Fault registers. The state of the UV fault bit is determined by the logical OR of the fault output from these two undervoltage monitors.

The VREG undervoltage threshold level is determined by the state of the VBB undervoltage monitor. If V_{BB} falls enough to create a VBB undervoltage fault, then the VREG threshold is reduced to the low level, V_{REGUVL}. When V_{BB} is above the VBB undervoltage threshold, the VREG undervoltage threshold is set to the high level, V_{REGUVH}. This allows the A4980 to continue to drive a stepper motor with a motor supply (VBB) voltage as low

as 3.5 V without disabling the outputs. By retaining the higher threshold (when V_{BB} is above the VBB undervoltage threshold), the A4980 also provides protection for its outputs from excessive power dissipation during a high voltage transient on VBB when an independent VREG undervoltage condition is present.

Note that the point at which the A4980 stops driving the motor is always less than 3.5 V. The maximum value for the low-level VREG undervoltage threshold is 3.15 V, and for the VREG dropout, it is 200 mV. This means that the VREG undervoltage will never occur until V_{BB} falls below 3.3 V, giving a 200 mV margin for noise. Typically the VREG undervoltage will occur when V_{BB} drops below 3.1 V. The A4980 will continue with full PWM current control and all output fault detection down to the point at which the VREG undervoltage fault occurs.

Figures 3 and 4 show how the undervoltage thresholds change when a typical cold crank transient occurs.

The standard, ISO7637 Pulse 4, is shown for reference in figure 3. The V_{BB} transient shown (solid line) is lower than the standard ISO pulse due to the forward voltage of a reverse polarity protection diode and switching transients.

Figure 4 provides more detail around the time that the VBB undervoltage is detected. It shows the V_{REG} voltage following below the V_{BB} voltage by the maximum offset voltage of the V_{REG} regulator. Typically this dropout will be less than the 200 mV shown.

When V_{BB} drops below the falling VBB undervoltage threshold, V_{BBUV} (at 1.2 ms and 5.6 V in figure 4), the VREG undervoltage threshold, V_{REGUV}, drops from 4.8 V (V_{REGUVH} typical) to 3.0 V (V_{REGUVL} typical). At the same time, the VBB undervoltage threshold increases by the threshold hysteresis, 760 mV (typical), the UV fault bit in the diagnostic registers is set, and the fault flag is active.

This state remains until V_{BB} increases above the rising VBB undervoltage threshold (at 127 ms and 6.4 V in figure 3). At this point the VREG undervoltage threshold is increased back to the high threshold value of 4.8 V (V_{REGUVH} typical), and the reverse hysteresis is applied to the VBB undervoltage threshold causing it to drop back to the falling level of 5.5 V (V_{BBUV} typical). The Fault flag goes inactive but the UV fault bit remains set in the Fault registers until cleared by a diagnostic registers reset.

When a power-on reset occurs, or the A4980 is activated from sleep mode by taking RESETn high, then the VREG undervoltage threshold is initially set to the high level, V_{REGUVH}. (A power-on reset occurs when power is first applied or the logic supply, V_{DD}, drops below the VDD undervoltage threshold). The threshold will remain at the high level, irrespective of the state of V_{BB}, until the VBB voltage has exceeded the undervoltage threshold for the first time. After this has happened, the VREG undervoltage threshold is then determined by the state of the VBB undervoltage monitor output. When applying power or when activating from sleep mode the outputs should remain inactive for at least the Wakeup from

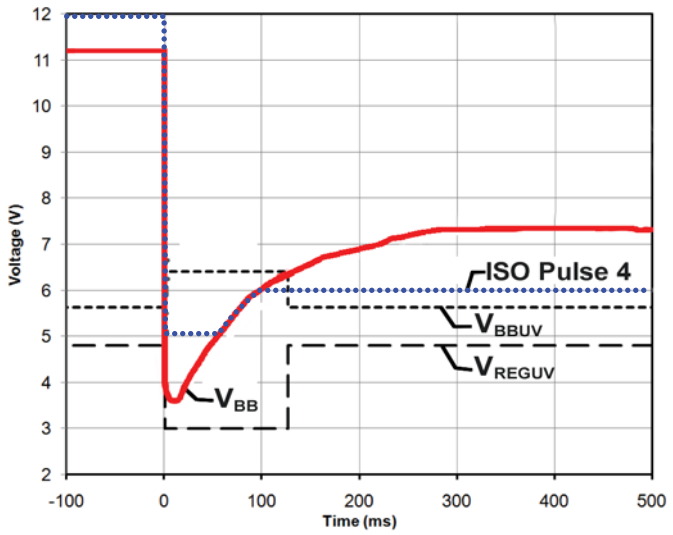


Figure 3. A4980 response to an undervoltage transient

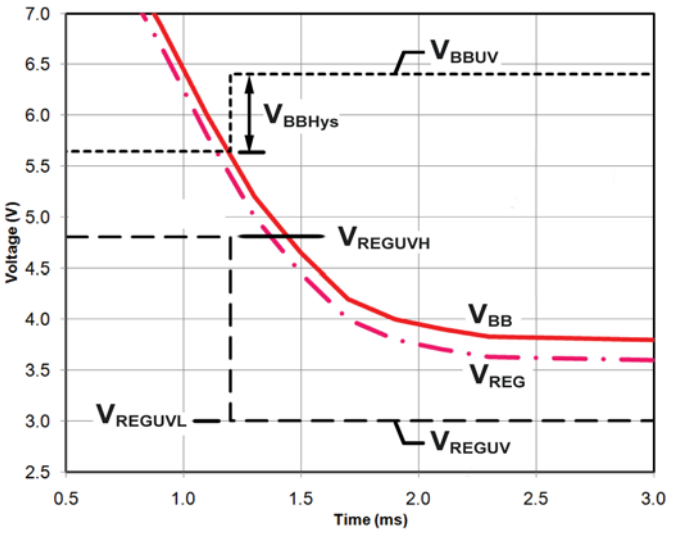


Figure 4. Expanded view of figure 3

Reset Time, t_{EN}, to allow the internal charge pump and regulator to reach their full operating state.

The VBB and VREG undervoltage monitor system is designed to allow the A4980 to continue operating safely during the extreme motor supply voltage drop caused by cold cranking with a weak battery when a reverse battery protection diode is also present. During low voltage transients the A4980 will continue to step a motor. However, current control will not achieve the same accuracy as specified with a motor supply voltage greater than 7 V. In fact a low motor supply voltage may not provide sufficient drive to allow the motor current to reach its normal operating level, especially if the motor is rotating and a back EMF is present. It is therefore recommended that when a VBB undervoltage condition is indicated, the motor is held stationary. This will help ensure that the motor does not slip and that the system retains some degree of control over the motor position, thus avoiding the need to recalibrate the motor position.

The output drive FETs of the A4980 remain protected from short circuits down to the VREG undervoltage level. However, the overcurrent thresholds cannot be guaranteed to meet the precision specified at higher supply voltage. In addition the open load detection may indicate a fault and the stall detection is not likely to correctly identify a motor stall condition when VBB is below the VBB undervoltage level.

Temperature Monitors

Three specific temperature thresholds are provided: a hot warning, a cold warning, and an overtemperature shutdown. In addition, the analog internal signal used to determine the chip temperature can be selected in Configuration Register 1 as the output on the DIAG pin through the serial interface. The analog scale is $T_J \approx (V_{DIAG} - V_{TO}) / A_T$.

Hot Warning If the chip temperature rises above the Hot Temperature Warning Threshold, T_{JWH}, the Fault flag will go low and the Hot Warning bits will be set in the diagnostic registers. No action will be taken by the A4980. When the temperature drops below the Hot Temperature Warning Threshold, the Fault flag will go high but the Hot Warning bits remain set in the diagnostic registers until reset.

Cold Warning If the chip temperature falls below the Cold Temperature Warning Threshold, T_{JWC}, the Fault flag will go low and the Cold Warning bits will be set in the diagnostic registers. No action will be taken by the A4980. When the temperature rises above the Cold Temperature Warning Threshold, the Fault flag will go high but the Cold Warning bits remain set in the diagnostic registers until reset.

Overtemperature Shutdown If the chip temperature rises above the Overtemperature Shutdown Threshold, T_{JF}, the Fault flag will go low and the Thermal Shutdown bits will be set in the diagnostic registers. The A4980 will disable the outputs to try to prevent a further increase in the chip temperature. When the temperature drops below the Overtemperature Shutdown Threshold, the Fault flag will go high but the Thermal Shutdown bits remain set in the diagnostic register until reset.

Bridge and Output Diagnostics

The A4980 includes monitors that can detect a short to supply or a short to ground at the motor phase connections. These conditions are detected by monitoring the current from the motor phase connections through the bridge to the motor supply and to ground.

Low current comparators and timers are provided to help detect possible open load conditions.

Short to Supply A short from any of the motor connections to the motor supply (VBBA or VBBB) is detected by monitoring the voltage across the low-side current sense resistor in each bridge. This gives a direct measurement of the current through the low side of the bridge.

When a low-side FET is in the On state, the voltage across the sense resistor, under normal operating conditions, should never be more than the Maximum Sense Voltage, V_{SMAX}. In this state, an overcurrent is determined to exist when the voltage across the sense resistor exceeds the Low-Side Overcurrent Sense Voltage, V_{OCL}, typically $2 \times V_{SMAX}$. This overcurrent must be continuously present for at least the Overcurrent Fault Delay, t_{SCT}, before the short fault is confirmed by setting the relevant bit in FAULT0 and driving the DIAG output low if the Fault Output flag is selected. The output is switched off and remains off until a fault reset occurs.

Note that the sense resistor cannot distinguish which low-side FET is in an overcurrent state. So, if more than one low-side FET is active when the fault is detected, for example during low-side recirculation with synchronous rectification, then the shorted connection is determined from the internal PWM state.

The actual overcurrent that V_{OCL} represents is determined by the value of the sense resistor and is typically $2 \times I_{SMAX}$.

Short to Ground A short from any of the motor connections to ground is detected by directly monitoring the current through each of the high-side FETs in each bridge.

When a high-side FET is in the On state the maximum current is typically always less than 1 A. In this state, an overcurrent is determined to exist when the current through the active high-side FET exceeds the High-Side Overcurrent Threshold, I_{OCH}.

This overcurrent must be present for at least the Overcurrent Fault Delay, t_{SCT}, before the short fault is confirmed by setting the relevant bit in FAULT0 and driving the DIAG output low if the Fault Output flag is selected. The output is switched off and remains off until a fault reset occurs.

Note that when a short to ground is present the current through the high-side FET is limited to the High-Side Current Limit, I_{LIMH}, during the Overcurrent Fault Delay, t_{SCT}. This prevents large negative transients at the phase output pins when the outputs are switched off.

Shorted Load A short across the load is indicated by concurrent short faults on both high side and low side.

Short Fault Blanking All overcurrent conditions are ignored for the duration of the Overcurrent Fault Delay, t_{SCT}. The short detection delay timer is started when an overcurrent first occurs. If the overcurrent is still present at the end of the short detection delay time then a short fault will be generated and latched. If the overcurrent goes away before the short detection delay time is complete, then the timer is reset and no fault is generated.

This prevents false short detection caused by supply and load transients. It also prevents false short detections resulting from current transients generated by the motor or wiring capacitance when a FET is first switched on.

Short Fault Reset and Retry When a short circuit has been detected all outputs for the faulty phase are disabled until the next occurrence of: the next rising edge on the STEP input, the RESETn input is pulsed low, or until the diagnostic registers are reset by writing to one of the registers through the serial interface. At the next STEP command or after a fault reset, the Fault Register flag is cleared, the outputs are re-enabled, and the voltage across the FET is resampled. Note that the diagnostic registers are not cleared by the rising edge of the STEP input.

While the fault persists the A4980 will continue this cycle, enabling the outputs for a short period then disabling the outputs. This allows the A4980 to handle a continuous short circuit without damage. If, while stepping rapidly, a short circuit appears and no action is taken, the repeated short circuit current pulses will eventually cause the temperature of the A4980 to rise and an overtemperature fault will occur.

Open Load Detection Open load conditions are detected by monitoring the phase current when the phase DAC value is greater than 31. The Open Load Current Threshold, I_{OL}, is defined by the OL0 and OL1 bits in the Run register as a percentage of the maximum (100%) phase current, I_{PMAX}, defined in the Phase Current table. The 100% level in the Phase Current table is defined by the sense resistor value and the contents of the MXI0 and MXI1 bits in Configuration Register 0.

For example:

- if R_S = 180 mΩ and V_{REF} = 2 V, then I_{SMAX} = 694 mA
- if MXI1 = 1 and MXI0 = 0, then I_{PMAX} = 520 mA
- if OL1=0 and OL0=1, then I_{OL} = 156 mA

The open load current monitor is only active after a blank time from the start of a PWM cycle. An open load can only be detected if the DAC value for the phase is greater than 31 and the current has not exceeded the Open Load Current Threshold for more than 15 PWM cycles.

The A4980 continues to drive the bridge outputs under an open load condition and clears the Fault Register flag as soon as the phase current exceeds the Open Load Current Threshold or the DAC value is less than 32. The diagnostic registers retain the open load fault bits, OLA and OLB, and will not be cleared until RESETn is pulsed low or one of the diagnostic registers is written through the serial interface.

Stall Detection A PWM monitor feature is included in the A4980 to assist in determining the stall condition of the stepper motor. A stalled motor condition is when the phase currents are being sequenced to step the motor but the motor remains stationary. This can be due to a mechanical blockage such as an end stop or it can be due to the step sequence exceeding the motor capability for the attached load. Reliable stall detection in a simple stepper driver is only possible by combining the PWM monitor with a continuous step sequence at a sufficiently high step rate.

When a motor is stopped or moving slowly there is no back EMF to impede the current in the phase windings. This allows the

current to rise to the limit quickly and the PWM current control to activate. However, when a motor is running at speed the back EMF, generated by the speed of the magnetic poles in the motor passing the phase windings, acts against the supply voltage and reduces the rise time of the phase current. Therefore the PWM current control takes longer to activate. Assuming a constant step rate, this results in fewer PWM cycles for each step of the motor.

The A4980 uses this difference to detect a motor changing from continuous stepping to stalled. Two PWM counters, one for each phase, accumulate the number of PWM cycles when the phase current is stepped from zero to full current. At the end of each phase current rise, the counter for that phase is compared to the counter for the previous current rise, in the opposite phase. If the difference is greater than the number in the PWM compare register, then the ST bit in the diagnostic registers is set. In addition, if the ST signal is selected as the output on the DIAG pin, then the pin will go low.

This stall detection scheme assumes a number of factors:

- The motor must be stepping fast enough for the back EMF to reduce the phase current slew rate. Stall detection reliability improves as the current slew rate reduces.
- The motor is not being stepped in full step mode.
- The phase current table must conform to the 0% and ±100% conditions at steps 0, 16, 32, and 48.
- The phase current profiles must be the same for both phases.

Although stall detection cannot be guaranteed using this detection method, good stall detection reliability can be achieved by careful selection of motor speed, count difference, and by conforming to the above factors.

In addition to using the integrated features of the A4980, it is also possible to perform stall detection by examining the PWM on-time for a single phase using an external microcontroller. In the A4980 the PWM-on signal for phase A can be selected as the output on the DIAG pin, by using the serial interface.

Serial Interface Description

A three wire synchronous serial interface, compatible with SPI, can be used to configure and control all the features of the A4980. A fourth wire can be used to provide diagnostic feedback. The registers that are accessible through the serial interface are defined in table 2.

The A4980 can be operated without using the serial interface, by using the default configuration and control register settings and the STEP and DIR logic inputs for motor control. However, application-specific configurations are only possible by setting the appropriate register bits through the serial interface. In addition to setting the configuration bits, the serial interface can also be used to control the motor directly.

The serial interface timing requirements are specified in the Electrical Characteristics table, and illustrated in figure 1.

Writing to Configuration and Control Registers

When writing to the serial register, data is received on the SDI pin and clocked through a shift register on the rising edge of the clock signal input on the SCK pin. STRn is normally held high, and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, thus allowing multiple SDI slave units to use common SDI, SCK, and SDO connections. Each independent slave requires a dedicated STRn connection.

The serial data word has 16 bits, MSB input first. After 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs,

Table 2. Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Configuration and Control Registers (Write)																
Configuration Register 0 (CONFIG0)	0	0	SYR	MS1	MS0	MXI1	MXI0	PFD2	PFD1	PFD0	TBK1	TBK0	TOF2 / FRQ2	TOF1 / FRQ1	TOF0 / FRQ0	PWM
			1	0	0	1	1	1	0	0	0	1	1	1	0	0
Configuration Register 1 (CONFIG1)	0	1	OSC	TSC1	TSC0						CD3	CD2	CD1	CD0	DIAG1	DIAG0
			0	1	0	0	0	0	0	0	1	0	0	0	0	0
Run Register (RUN)	1	0	EN	OL1	OL0	HLR	SLEW	BRK	DCY1	DCY0	SC5	SC4	SC3	SC2	SC1	SC0
			0	0	1	0	1	0	0	1	0	0	0	0	0	0
Table Load Register (TBLLD)	1	1								PTP	PT5	PT4	PT3	PT2	PT1	PT0
			0	0	0	0	0	0	0	1	0	0	0	0	0	0
Diagnostic Registers (Read)																
Fault Register 0 (FAULT0)	FF	TW1	TW0	OV	UV	ST	OLB	OLA	BML	BMH	BPL	BPH	AML	AMH	APL	APH
Fault Register 1 (FAULT1)	FF	TW1	TW0	OV	UV	ST	OLB	OLA	0	0	SA5	SA4	SA3	SA2	SA1	SA0

*Power-on reset value shown below each input register bit.

the internal control circuits act on the new configuration and control data, and the diagnostic registers are reset.

If there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the configuration and control registers. In addition the diagnostic registers will not be reset. Instead the FF bit will be set to 1 in the diagnostic registers, to indicate a data transfer error.

The first two bits of the serial word are used to select the register to be written. This provides access to four writable registers:

- The Configuration registers are used for system configuration: CONFIG0 for system parameters, and CONFIG1 for system and diagnostic parameters.
- The RUN register contains motor drive settings used to control the motor movement and phase current.
- The fourth writable register, TBLLD, is a port that allows sequential loading of the 16 distinct phase current table settings.

Reading from Diagnostic Registers

In addition to the writable registers there are two diagnostic registers. The first eight (most significant) bits of both diagnostic registers contain the same flags, only the last eight (least significant) bits differ, as follows:

- FAULT0 contains the short-circuit fault flags
- FAULT1 contains the present Step Angle Number

Each time a configuration and control register is written, one of the diagnostic registers can be read, MSB first, on the serial output pin, SDO (see timing in figure 1). FAULT1 is made the active register for serial transfer and output on SDO only while CONFIG1 is being written, that is, only when the first bit of the input word is 0 and the second bit is 1. FAULT0 is the active register for serial transfer and output on SDO during writes to any other configuration or control register.

When STRn goes low to start a serial write, SDO comes out of its high impedance state and outputs the serial register Fault Register flag. This allows the main controller to poll the A4980 through the serial interface to determine if a fault has been detected. If no faults have been detected then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high the transfer will be terminated and SDO will go into its high impedance state.

Configuration and Run Registers

These registers are used for system configuration and motor control. Access is described in the section Writing to Configuration and Control Registers, above.

CONFIG0 sets certain system parameters, and CONFIG1 sets system and diagnostic output selection parameters. The RUN register contains motor drive settings used to control the motor movement and phase current.

Phase Table Load Register

This is one of the configuration and control registers, accessed when both address bits are 1. It can be used to write a sequence of values to the phase current table in the A4980. This allows the current at each Step Angle Number to be tailored to suit the microstep current profile requirements of a specific motor. In most cases this feature will not be required and the default sinusoidal profile will suffice. However for some motor / load combinations, altering the current profile can improve torque ripple, resulting in lower mechanical vibration and noise.

Although the phase current table contains 64 entries for each of two phases, only 16 distinct values are required. These 16 values correspond to one quadrant of the table for a single phase, and they are repeated for the other three quadrants and again for the four quadrants of the other phase. So each of the 16 values written to the Phase Table Load register are written to 8 locations in the phase current table.

The 16 values must be entered by sequential writes to the Phase Table Load register. The first write to the register after writing to any other register, or after a reset (RESETn pulse low or power-on), puts that value, PT[5..0], into the first phase table address, a 6-bit field defined as PT(0). Subsequent writes put values into successive addresses: PT(1), PT(2), and so forth up to PT(15). After the sixteenth value has been written, no more values are accepted and any writes to the Phase Table Load register are ignored. As each value is received, it is effectively distributed to all eight required locations in the phase current table.

An optional simple odd parity scheme is included to provide some measure of error checking, if required. Each 6-bit value can be supplemented with an additional parity bit, PTP, to ensure an odd number of 1s in the transmission. This is checked by the A4980 and if a the number of 1s in the value plus parity bit is not odd, the FF bit will be set and the SDO pin will go high the next time STRn is taken low, indicating a parity error. That data will still be written to the next phase table value address; it is incumbent upon the external controller to take action, if required.

If the write sequence is broken (by a reset, by writing to another register, or by a data transfer error) before the sequence has been completed, then the phase table value address will be reset to PT(0). If it is required to load the table, then the entire 16-value sequence must be sent.

After loading, although the phase current table is volatile, a reset using a low pulse on the RESETn pin does not corrupt the table. The table is only reset to default values on a power-on reset.

Diagnostic Registers

The diagnostic registers comprise two read-only fault data registers. Access is described in the section Reading from Diagnostic Registers, above.

The diagnostic registers contain fault flags for each fault condition and are reset to all 0s on the completion of each serial access. They are also reset to all 0s each time the RESETn input is low for longer than the Reset Pulse Width, t_{RST} . FAULT0 is set to all 1s at power-up or after a power-on reset. This indicates to the external controller that a power-on reset has taken place and all registers have been reset. Note that a power-on reset only occurs when the V_{DD} supply rises above its undervoltage threshold.

Power-on reset function is not affected by the state of the motor supply or V_{REG}.

The first bit in both registers is the Fault Register flag, FF. This is high if any bits in FAULT0 are set, or if a serial write error or parity error has occurred.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONFIG 0	0	0	SYR	MS1	MS0	MXI1	MXI0	PFD2	PFD1	PFD0	TBK1	TBK0	TOF2 FRQ2	TOF1 FRQ1	TOF0 FRQ0	PWM
			1	0	0	1	1	1	0	0	0	1	1	1	0	0

Configuration Register 0

SYR Synchronous rectification

SYR	Synchronous Rectification	Default
0	Diode recirculation	
1	Synchronous	D

MS[1..0] Microstep mode for external STEP input control

MXI1	MXI0	Microstep Mode	Default
0	0	Full Step	D
0	1	Half Step	
1	0	Quarter Step	
1	1	Sixteenth Step	

MXI[1..0] Max phase current as a percentage of I_{SMAX}

MXI1	MXI0	Maximum Current	Default
0	0	25%	
0	1	50%	
1	0	75%	
1	1	100%	D

PFD[2..0] Fast decay time for mixed decay
Assumes 4-MHz clock

PFD2	PFD1	PFD0	Fast Decay Time	Default
0	0	0	2 µs	
0	0	1	3 µs	
0	1	0	4 µs	
0	1	1	6 µs	
1	0	0	8 µs	D
1	0	1	10 µs	
1	1	0	14 µs	
1	1	1	20 µs	

TBK[1..0] Blank Time
Assumes 4-MHz clock

TBK1	TBK0	Blank Time	Default
0	0	1 µs	
0	1	1.5 µs	D
1	0	2.5 µs	
1	1	3.5 µs	

TOF[2..0] Off time (only valid when PWM bit = 0)
Replaces FRQ bits
Assumes 4-MHz clock

TOF2	TOF1	TOF0	Off Time	Default
0	0	0	20 µs	
0	0	1	24 µs	
0	1	0	28 µs	
0	1	1	32 µs	
1	0	0	36 µs	
1	0	1	40 µs	
1	1	0	44 µs	D
1	1	1	48 µs	

FRQ[2..0] Frequency (only valid when PWM bit = 1)
Replace TOF bits
Assumes 4-MHz clock

FRQ2	FRQ1	FRQ0	Period / Frequency	Default
0	0	0	24 µs / 41.7 kHz	
0	0	1	32 µs / 31.3 kHz	
0	1	0	40 µs / 25.0 kHz	
0	1	1	46 µs / 21.7 kHz	
1	0	0	52 µs / 19.2 kHz	
1	0	1	56 µs / 17.9 kHz	
1	1	0	60 µs / 16.7 kHz	D
1	1	1	64 µs / 15.6 kHz	

PWM PWM configuration

PWM	MODE	Default
0	Fixed off-time	D
1	Fixed frequency	

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONFIG 1	0	1	OSC	TSC1	TSC0						CD3	CD2	CD1	CD0	DIAG1	DIAG0
			0	1	0	0	0	0	0	0	1	0	0	0	0	0
RUN	1	0	EN	OL1	OL0	HLR	SLEW	BRK	DCY1	DCY0	SC5	SC4	SC3	SC2	SC1	SC0
			0	0	1	0	1	0	0	1	0	0	0	0	0	0

Configuration Register 1

OSC Selects clock source

OSC	Clock Source	Default
0	Internal	D
1	External	

Overcurrent fault delay

TSC[1..0] Assumes 4-MHz clock

TSC1	TSC0	Detect Delay Time	Default
0	0	0.5 µs	
0	1	1 µs	
1	0	2 µs	D
1	1	3 µs	

PWM count difference for ST detection

CD[3..0] Default to 8

DIAG[1..0] Selects signal routed to DIAG output

DIAG1	DIAG0	Signal on DIAG Pin	Default
0	0	Fault–low true	D
0	1	ST–low true	
1	0	PWM-on, Phase A	
1	1	Temperature	

Run Register

Phase current enable

EN OR with ENABLE pin

EN	Phase Current Enable	Default
0	Output bridges disabled if ENABLE pin = 0	D
1	Output bridges enabled	

Open load current threshold as a percentage of

OL[1..0] maximum current defined by I_{SMAX} and MXI[1..0]

OL1	OL0	Open Load Current	Default
0	0	20%	
0	1	30%	D
1	0	40%	
1	1	50%	

HLR Selects slow decay and brake recirculation path

HLR	Recirculation Path	Default
0	High side	D
1	Low side	

SLEW Slew rate control

SLEW	Slew Rate Control	Default
0	Disable	
1	Enable	D

BRK Brake enable

BRK	Brake	Default
0	Normal operation	D
1	Brake active	

DCY[1..0] Decay mode selection

DCY1	DCY0	Decay Mode	Default
0	0	Slow	
0	1	Mixed—PFD fixed	D
1	0	Mixed—PFD auto	
1	1	Fast	

SC[5..0] Step change number

2's complement format

Positive value increases Step Angle Number

Negative value decreases Step Angle Number

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBLLD	1	1								PTP	PT5	PT4	PT3	PT2	PT1	PT0
			0	0	0	0	0	0	0	0	1	0	0	0	0	0
Fault 0	FF	TW1	TW0	OV	UV	ST	OLB	OLA	BML	BMH	BPL	BPH	AML	AMH	APL	APH
Fault 1	FF	TW1	TW0	OV	UV	ST	OLB	OLA	0	0	SA5	SA4	SA3	SA2	SA1	SA0

Table Load Register

PTP Parity bit (odd parity)
PT(0..15)[5..0] Phase Table Value

Table Load Register Mapping

	Step Angle Number							
	Phase A				Phase B			
0%	0		32			16		48
PT(0)	1	31	33	63	15	17	47	49
PT(1)	2	30	34	62	14	18	46	50
PT(2)	3	29	35	61	13	19	45	51
PT(3)	4	28	36	60	12	20	44	52
PT(4)	5	27	37	59	11	21	43	53
PT(5)	6	26	38	58	10	22	42	54
PT(6)	7	25	39	57	9	23	41	55
PT(7)	8	24	40	56	8	24	40	56
PT(8)	9	23	41	55	7	25	39	57
PT(9)	10	22	42	54	6	26	38	58
PT(10)	11	21	43	53	5	27	37	59
PT(11)	12	20	44	52	4	28	36	60
PT(12)	13	19	45	51	3	29	35	61
PT(13)	14	18	46	50	2	30	34	62
PT(14)	15	17	47	49	1	31	33	63
PT(15)		16		48	0		32	

Fault Register 0

FF Fault register flag
TW1 Temperature diagnostic
TW0 Temperature diagnostic
OV Overvoltage on VBB detected
UV Undervoltage on VREG or VBB detected
ST Stall detected
OLB Open load detected on phase B
OLA Open load detected on phase A
BML Overcurrent detected on BM output low side
BMH Overcurrent detected on BM output high side
BPL Overcurrent detected on BP output low side
BPH Overcurrent detected on BP output high side
AML Overcurrent detected on AM output low side
AMH Overcurrent detected on AM output high side
APL Overcurrent detected on AP output low side
APH Overcurrent detected on AP output high side

Fault Register 1

FF Fault register flag
TW1 Temperature diagnostic
TW0 Temperature diagnostic
OV Overvoltage on VBB detected
UV Undervoltage on VREG or VBB detected
ST Stall detected
OLB Open load detected on phase B
OLA Open load detected on phase A
SA[0..5] Step Angle Number read back
OLA Open load detected on phase A

TW[0..1] Temperature diagnostic

TW1	TW0	Thermal Indicator
0	0	No Fault
0	1	Cold Warning
1	0	Hot Warning
1	1	Overtemperature Shutdown

Application Information

Motor Movement Control

The A4980 provides two independent methods to control the movement of a stepper motor. The simpler is the Step and Direction method, which only requires two control signals to control the stepper motor in either direction. The other method is through the serial interface, which provides more flexible control capability. Both methods can be used together (although it is not common), provided the timing restrictions of the STEP input in relation to the STRn input are preserved.

Phase Table and Phase Diagram

The key to understanding both of the available control methods lies in understanding the Phase Current table (table 7). This table contains the relative phase current magnitude and direction for each of the two motor phases at each microstep position. The maximum resolution of the A4980 is one-sixteenth microstep. That is 16 microsteps per full step. There are 4 full steps per electrical cycle, so the phase current table has 64 microstep entries. The entries are numbered from 0 to 63. This number represents the phase angle within the full 360° electrical cycle and is called the Step Angle Number. This is illustrated in figure 5.

Figure 5 shows the contents of the phase current table as a phase diagram. The phase B current, I_B, from the phase current table, is plotted on horizontal axis and the phase A current, I_A, is plotted on the vertical axis. The resultant motor current at each microstep is shown as numbered radial arrows. The number shown corresponds to the one-sixteenth microstep Step Angle Number in the phase current table.

Figure 6 shows an example of calculating the resultant motor current magnitude and angle for step number 28. The target is to have the magnitude of the resultant motor current be 100% at all microstep positions. The relative phase currents from the phase current table are:

$$I_A = 37.50\%$$

$$I_B = -92.19\%$$

Assuming a full scale (100%) current of 1A means that the two phase currents are:

$$I_A = 0.3750 \text{ A}$$

$$I_B = -0.9219 \text{ A}$$

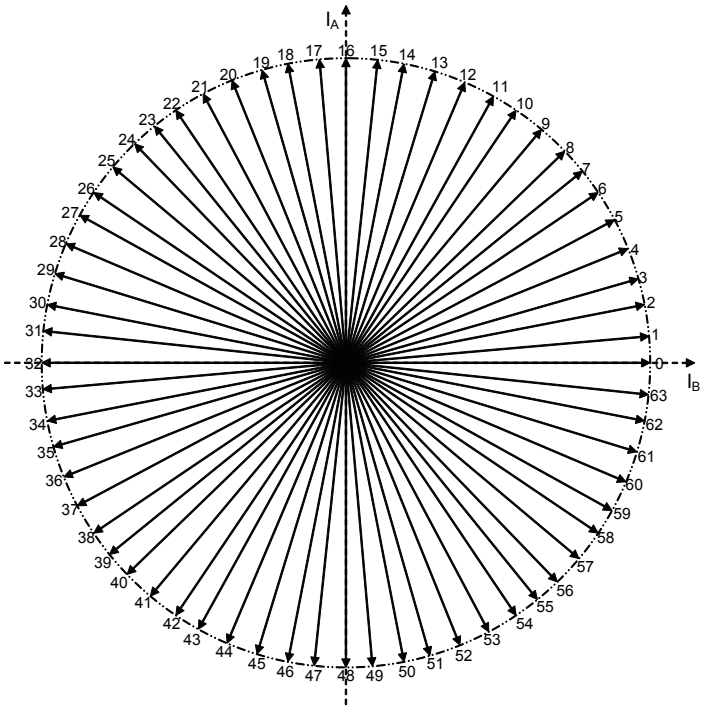


Figure 5. A4980 phase current table as a phase diagram; values shown are referred to as the Step Angle Number

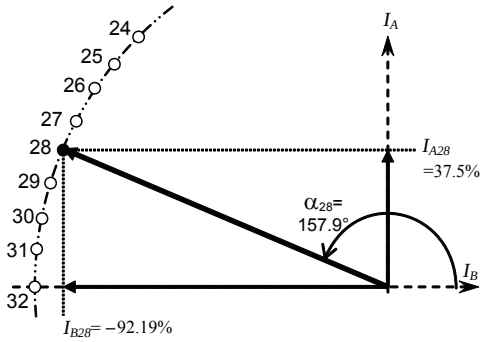


Figure 6. Calculation of resultant motor current

The magnitude of the resultant will be the square root of the sum of the squares of these two currents:

$$|I_{28}| = \sqrt{I_A^2 + I_B^2} = \sqrt{0.1406 + 0.8499} = 0.9953 \text{ (A)}$$

So the resultant current magnitude is 99.53% of full scale. This is within 0.5% of the target (100%) and is well within the ±5% accuracy of the A4980.

The reference angle, zero degrees (0°), within the full electrical cycle (360°), is defined as the angle where I_B is at +100% and I_A is zero. Each full step is represented by 90° in the electrical cycle so each one-sixteenth microstep is: 90°/16 steps = 5.625°. The target angle of each microstep position with the electrical cycle is determined by the product of the Step Angle Number and the angle for a single microstep. So for the example of figure 5:

$$\alpha_{28(TARGET)} = 28 \times 5.625° = 157.5°$$

The actual angle is calculated using basic trigonometry as:

$$\alpha_{28(ACTUAL)} = 180 + \tan^{-1}\left(\frac{I_{A28}}{I_{B28}}\right)$$

$$= 180 + (-22.1) = 157.9°$$

So the angle error is only 0.4°. Equivalent to about 0.1% error in 360° and well within the current accuracy of the A4980.

Note that each phase current in the A4980 is defined by a 6-bit DAC. This means that the smallest resolution of the DAC is 100 / 64 = 1.56% of the full scale, so the A4980 cannot produce a resultant motor current of exactly 100% at each microstep. Nor can it produce an exact microstep angle. However, as can be seen from the calculations above, the results for both are well within the specified accuracy of the A4980 current control. The resultant motor current angle and magnitude are also more than precise enough for all but the highest precision stepper motors.

With the phase current table, control of a stepper motor is simply a matter of increasing or decreasing the Step Angle Number to move around the phase diagram of figure 5. This can be in predefined multiples using the STEP input, or it can be variable using the serial interface.

Using Step and Direction Control

The STEP input moves the motor at the microstep resolution defined by the two microstep select variables, MS0 and MS1, logic levels. The DIR input defines the motor direction. These inputs define the output of a translator which determines the required Step Angle Number in the phase current table. The MS0 and MS1 can be set to select full step, half step, quarter step, or sixteenth step microstepping as follows:

MS1	MS0	Microstep Mode
0	0	Full step
0	1	Half step
1	0	Quarter step
1	1	Sixteenth step

MS0 and MS1 can be accessed through the serial interface or directly on pins 13 and 12 respectively. The values of MS0 and MS1 are defined as the logical OR of the logic level on the input pins and the value in Configuration Register 0. The bits in the register default to 0 so if the serial interface is not used then MS0 and MS1 are defined by the input pins alone. If only the serial interface is used to set the microstep resolution, then the MS0 and MS1 logic input pins should be tied low to ensure that the register retains full control over all resolutions. Note that the microstep select variables, MS0 and MS1, are only used with the STEP input; they can be ignored if the motor is fully controlled through the serial interface.

In sixteenth step mode the translator simply increases or decreases the Step Angle Number on each rising edge of the STEP input, depending on the logic state of the DIR input. In the other three microstep resolution modes the translator outputs specific Step Angle Numbers as defined in the phase current table.

Full step uses four of the entries in the phase current table. These are 8, 24, 40, and 56 as shown in figure 7. Note that the four positions selected for full step are not the points at which only one current is active, as would be the case in a simple on-off full step driver. There are two advantages in using these positions rather than the single full current positions. With both phases active, the power dissipation is shared between two drivers. This slightly improves the ability to dissipate the heat generated and reduces the stress on each driver.

The second reason is that the holding torque is slightly improved because the forces holding the motor are mainly rotational rather than mainly radial.

Half step uses eight of the entries in the phase current table. These are 0, 8, 16, 24, 32, 40, 48, and 56 as shown in figure 8.

Quarter step uses sixteen of the entries in the phase current table. These are 0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, and 60 as shown in figure 9.

In half step and in quarter step, the single phase active positions are used to preserve symmetry. However, if the motor is required to stop with a significant holding torque for any length of time it is recommended that the 45° positions be used; those are Step Angle Numbers 8, 24, 40, and 56, as used with full-step resolution.

The following table summarizes the Step Angle Numbers used for the four resolutions available when using the STEP input to control the output of the A4980:

Mode	Step Angle Numbers used
Full	8, 24, 40, 56
Half	0, 8, 16, 24, 32, 40, 48, 56
Quarter	0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60
Sixteenth	All

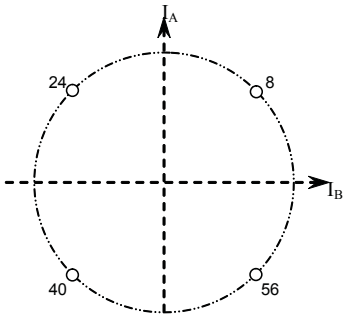


Figure 7. Full-step phase diagram using STEP input

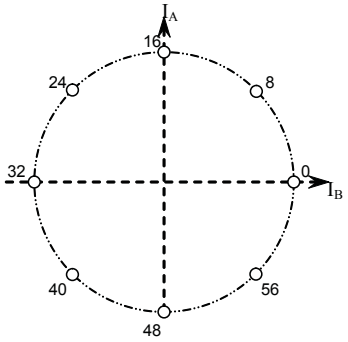


Figure 8. Half-step phase diagram using STEP input

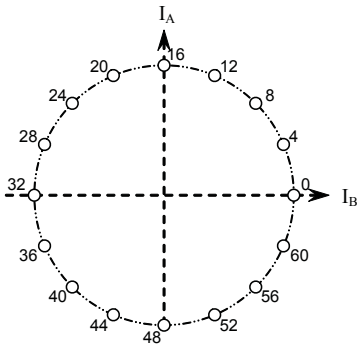


Figure 9. Quarter-step phase diagram using STEP input

The microstep select inputs can be changed between each rising edge of the STEP input. The only restriction is that the MSO and MS1 logic inputs must comply with the set-up and hold timing constraints. When the microstep resolution changes, the A4980 moves to the next available Step Angle Number on the next rising edge of the STEP input. For example, if the microstep mode is sixteenth and the present Step Angle Number is 59, then with the direction forwards (increasing Step Angle Number), changing to quarter step mode will cause the phase number to go to 60 on the next rising edge of the STEP input. If instead the microstep mode is changed to half step then the phase number will go to 0 on the next rising edge of the STEP input. If the microstep mode is changed to full step then the phase number will go to 8 on the next rising edge of the STEP input.

Control Through the Serial Interface

The A4980 provides the ability to directly control the motor movement using only the serial interface. In fact, all features of the A4980, except sleep mode, can be controlled through the serial interface thus removing the requirement for individual control inputs. This can reduce the interface requirement from multiple I/O signals to a single four wire interface.

Motor movement is controlled using the serial interface by increasing or decreasing the Step Angle Number. Note that the maximum value of the Step Angle Number is 63 and the minimum number is 0.Therefore, any increase or decrease in the microstep number is performed using modulo 64 arithmetic. This means that increasing a Step Angle Number of 63 by 1 will produce a Step Angle Number of 0. Increasing by two from 63 will produce 1 and so on. Similarly in the reverse direction, decreasing a Step Angle Number of 0 by 1 will produce a Step Angle Number of 63. Decreasing by two from 0 will produce 62 and so on.

The least significant six bits of the Run register, bits 0 to 5, are the step change number, SC[5..0]. This number is a two's complement number that is added to the Step Angle Number causing it to increase or decrease. Two's complement is the natural integer number system for most microcontrollers. This allows standard

arithmetic operators to be used, within the microcontroller, to determine the size of the next step increment. Table 6 shows the binary equivalent of each decimal number between –16 and +16.

Each increase in the Step Angle Number represents a forwards movement of one-sixteenth microstep. Each decrease in the Step Angle Number represents a reverse movement of one-sixteenth microstep.

To move the motor one full step, the Step Angle Number must be increased or decreased by 16. To move the motor one half step, the Step Angle Number must be increased or decreased by 8. For quarter step the increase or decrease is 4 and for eighth step, 2.

So, for example, to continuously move the motor forwards in quarter-step increments, the number 4 (000100) is repeatedly written to SC[5..0] through the serial interface Run register (see figure 10). To move the motor backwards in quarter step increments, the number -4 (111100) is repeatedly written to SC[5..0] (see figure 11). The remaining bits in the Run register should be set for the required configuration and sent with the step change number each time.

The step rate is controlled by the timing of the serial interface. It is the inverse of the step time, t_{STEP}, shown in figure 10. The motor step only takes place when the STRn goes from low to

Table 6. Binary Equivalents

Decimal	2's Complement	Decimal	2's Complement
0	000000		
1	000001	–1	111111
2	000010	–2	111110
3	000011	–3	111101
4	000100	–4	111100
5	000101	–5	111011
6	000110	–6	111010
7	000111	–7	111001
8	001000	–8	111000
9	001001	–9	110111
10	001010	–10	110110
11	001011	–11	110101
12	001100	–12	110100
13	001101	–13	110011
14	001110	–14	110010
15	001111	–15	110001
16	010000	–16	110000

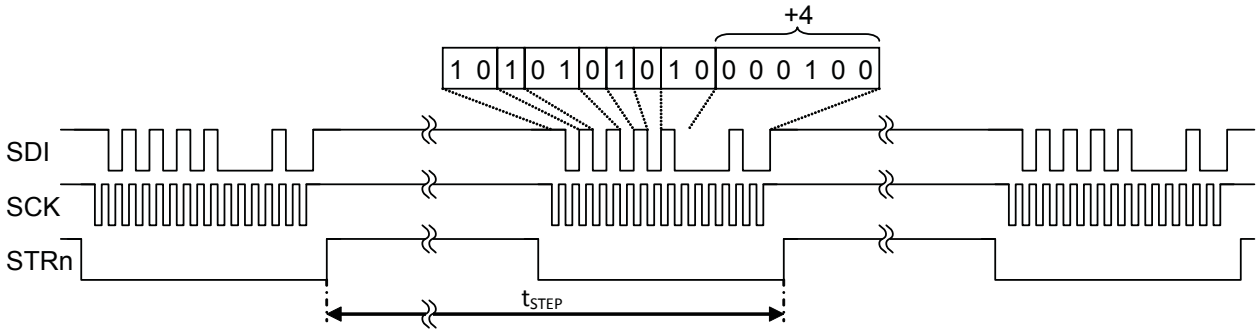


Figure 10. Serial interface sequence for quarter step in forward direction

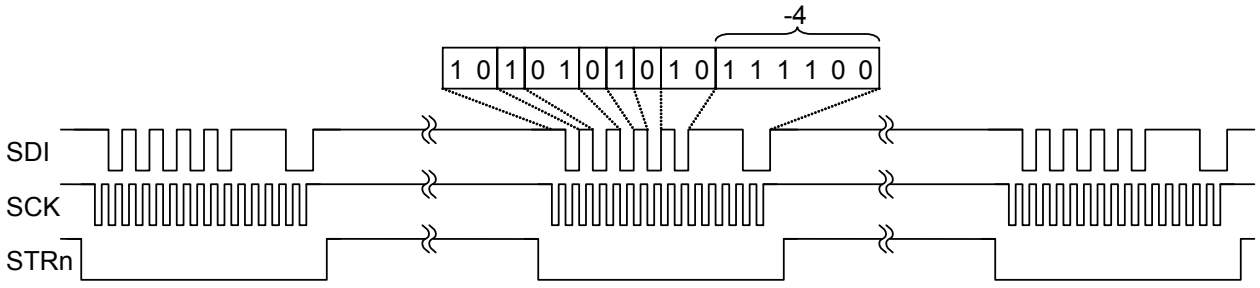


Figure 11. Serial interface sequence for quarter step in reverse direction

high when writing to the Run register. The motor step rate is therefore determined by the timing of the rising edge of the STRn input. The clock rate of the serial interface, defined by the frequency of the SCK input, has no effect on the step rate.

Using the Phase Table Load Capability

Torque Ripple Reduction

The performance and audible noise of any motor drive system is defined, to a large extent, by the torque ripple generated by both the motor and the load. In most cases, when using a stepper motor as the mechanical drive, the torque ripple of the load is not related to the mechanical steps of the motor and must be reduced by means unrelated to the motor and its drive system. However, for stepper motors in particular, torque ripple produced by the motor can be reduced by improvements in the mechanical design of the motor and by improvements in the phase current control system.

Torque ripple will naturally be high when driving a stepper motor in full step mode, due to the nature of stepping. However the torque ripple can be reduced by using microstepping. Increasing the number of microsteps per mechanical step will result in reduced torque ripple. This is one of the major reasons for using microstepping.

In the majority of cases the standard sinusoidal, microstep current profile will be sufficient to achieve a good performance with a good quality motor. In a few cases, further improvements in torque ripple performance may be achieved by modifying the microstep current profile to more closely match the motor characteristics. This is usually only necessary for higher quality, higher power stepper motors.

When using microstepping, the torque ripple is defined by the variation in torque at each microstep. In a hybrid stepper motor this is mostly determined by the mechanical construction of the motor, particularly the shape of the teeth on the poles of the stator. The shape of these teeth determine the variation in the *torque constant*, the ratio between current and torque, as the motor rotates. The variation in the torque constant can be seen by measuring the back EMF of the motor when being driven as a generator, that is when the shaft is driven by external means and the phase voltage is monitored. The back EMF represents the *motor constant,* which is essentially proportional to the torque constant.

If such torque ripple reduction measures are required, the A4980 provides the ability to modify the microstep current profile by programming the internal phase current table through the serial interface. The modified profile is then used, in place of the default sinusoidal profile, to compensate for any variation in motor torque constant. The current at each Step Angle Number can be set to suit the microstep current profile requirements of a specific motor.

Note: This is an advanced feature of the A4980, which will not be required for most applications. In general the default sinusoidal profile will suffice and therefore the phase current table does not have to be loaded.

Loading the Phase Current Table

The full phase current table in the A4980 contains one 6-bit value for each phase, at each microstep position. With 16 microsteps per mechanical step, 4 mechanical steps per electrical cycle, and 2 phases this gives a total of 128 values. However, due to symmetry, described below, this reduces to 17 independent values, one of which is always zero. The remaining 16 values can be loaded sequentially through the serial interface using the Phase Table Load register. Figure 12 shows the default phase table values plotted by Step Angle Number. Similar information is provided in table 7.

The diagram in figure 12 is marked with four quadrants, Q1 to Q4. The set of phase table values is the same in each quadrant in each phase. Consider phase A (bottom graph), quadrant 1 (Q1). This contains Step Angle Numbers 0 to 15. The default values in these 16 positions are selected to produce one quarter of a sinusoid.

Now consider the next quadrant (Q2) of phase A. The sequence of values in this quadrant form a mirror image, by Step Angle Number, of the values in Q1 so the same values are used but entered in the reverse sequence.

The following table shows the Step Angle Number in the first row increasing from 0 to 15, from left to right, and the default values also increasing from left to right in the second row. These first two rows are the entries for Q1 of phase A.

Step	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Q1
Value	0	5	11	18	23	29	35	40	44	48	52	55	58	60	62	63	
Step	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Q2
Value	5	11	18	23	29	35	40	44	48	52	55	58	60	62	63	63	

The second two rows are the entries for Q2 of phase A. The Step Angle Number in the third row increases from 16 to 31, this time from right to left, but the same default values still increase from left to right. A single value is therefore placed in more than one location in the table. Shown outlined above, steps 4 and 28 both contain the value 23.

The same principal can be applied to Q3 and Q4 of phase A. In this case the mirror image is in the horizontal axis, about the zero

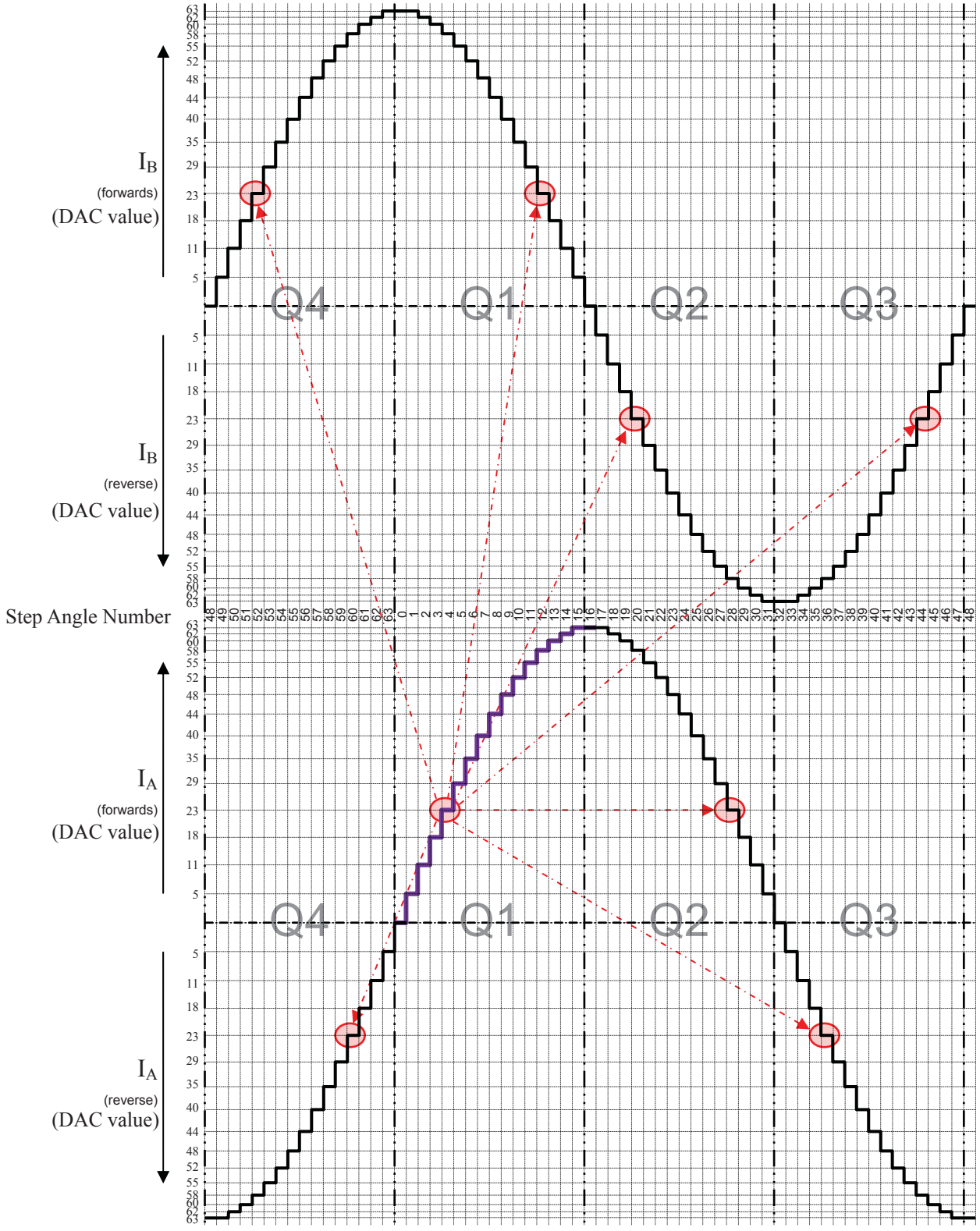


Figure 12. Default phase table values

reference value. Although the current in Q3 and Q4 for phase A is effectively negative, the negation is provided by controlling the direction of the current. The current control scheme still operates using positive values.

As shown below, the table of values can be extended to include Q3 and Q4 with the current direction indicated in the last column. Note that the same value is now applied to four locations in the full 360-degree electrical cycle.

Step	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Q1	FWD
Value	0	5	11	18	23	29	35	40	44	48	52	55	58	60	62	63		
Step		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	Q2	FWD
Value		5	11	18	23	29	35	40	44	48	52	55	58	60	62	63	63		
Step	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	Q3	Rev
Value	0	5	11	18	23	29	35	40	44	48	52	55	58	60	62	63		
Step		63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	Q4	Rev
Value		5	11	18	23	29	35	40	44	48	52	55	58	60	62	63	63		

Shown outlined above, steps 4, 28, 36, and 60 all contain the value 23.

The other phase, phase B, uses the same values as phase A but shifted back by 16 Step Angle Numbers. The full distribution of the value entered in step 4 of phase A is highlighted in figure 12 (and shown in table 7). This single value is used in a total of eight locations. The same distribution of values applies to all the values in steps 1 to 15. These values are defined in the A4980 as PT(0) to PT(14), respectively.

There are two exceptions to this data distribution principal. These are the zero value and the maximum value:

- The values in phase A steps 0 and 32 and phase B steps 16 and 48 are always set to zero and cannot be programmed.
- The maximum value, PT(15), is distributed to only two Step Angle Numbers in each phase. These are the points in the cycle where the peak current is required, namely phase A steps 16 and 48 and phase B steps 0 and 32.

Table 7. Phase Current Table (default, power-on content)

Step Angle Number					Phase Current (% of I_{PMAX})		Step Angle	Phase		DAC		Step Angle Number					Phase Current (% of I_{PMAX})		Step Angle	Phase		DAC	
Full	1/2	1/4	1/8	1/16	A	B		A	B	A	B	Full	1/2	1/4	1/8	1/16	A	B		A	B	A	B
	0	0	0	0	0.00	100.00	0.0	0	0	0	63		4	8	16	32	0.00	-100.00	180.0	0	1	0	63
				1	9.38	100.00	5.4	0	0	5	63					33	-9.38	-100.00	185.4	1	1	5	63
			1	2	18.75	98.44	10.8	0	0	11	62				17	34	-18.75	-98.44	190.8	1	1	11	62
				3	29.69	95.31	17.3	0	0	18	60					35	-29.69	-95.31	197.3	1	1	18	60
		1	2	4	37.50	92.19	22.1	0	0	23	58			9	18	36	-37.50	-92.19	202.1	1	1	23	58
				5	46.88	87.50	28.2	0	0	29	55					37	-46.88	-87.50	208.2	1	1	29	55
			3	6	56.25	82.81	34.2	0	0	35	52				19	38	-56.25	-82.81	214.2	1	1	35	52
				7	64.06	76.56	39.9	0	0	40	48					39	-64.06	-76.56	219.9	1	1	40	48
0	1	2	4	8	70.31	70.31	45.0	0	0	44	44	2	5	10	20	40	-70.31	-70.31	225.0	1	1	44	44
				9	76.56	64.06	50.1	0	0	48	40					41	-76.56	-64.06	230.1	1	1	48	40
			5	10	82.81	56.25	55.8	0	0	52	35				21	42	-82.81	-56.25	235.8	1	1	52	35
				11	87.50	46.88	61.8	0	0	55	29					43	-87.50	-46.88	241.8	1	1	55	29
		3	6	12	92.19	37.50	67.9	0	0	58	23			11	22	44	-92.19	-37.50	247.9	1	1	58	23
				13	95.31	29.69	72.7	0	0	60	18					45	-95.31	-29.69	252.7	1	1	60	18
			7	14	98.44	18.75	79.2	0	0	62	11				23	46	-98.44	-18.75	259.2	1	1	62	11
				15	100.00	9.38	84.6	0	0	63	5					47	-100.00	-9.38	264.6	1	1	63	5
	2	4	8	16	100.00	0.00	90.0	0	0	63	0		6	12	24	48	-100.00	0.00	270.0	1	1	63	0
				17	100.00	-9.38	95.4	0	1	63	5					49	-100.00	9.38	275.4	1	0	63	5
			9	18	98.44	-18.75	100.8	0	1	62	11				25	50	-98.44	18.75	280.8	1	0	62	11
				19	95.31	-29.69	107.3	0	1	60	18					51	-95.31	29.69	287.3	1	0	60	18
		5	10	20	92.19	-37.50	112.1	0	1	58	23			13	26	52	-92.19	37.50	292.1	1	0	58	23
				21	87.50	-46.88	118.2	0	1	55	29					53	-87.50	46.88	298.2	1	0	55	29
			11	22	82.81	-56.25	124.2	0	1	52	35				27	54	-82.81	56.25	304.2	1	0	52	35
				23	76.56	-64.06	129.9	0	1	48	40					55	-76.56	64.06	309.9	1	0	48	40
1	3	6	12	24	70.31	-70.31	135.0	0	1	44	44	3	7	14	28	56	-70.31	70.31	315.0	1	0	44	44
				25	64.06	-76.56	140.1	0	1	40	48					57	-64.06	76.56	320.1	1	0	40	48
			13	26	56.25	-82.81	145.8	0	1	35	52				29	58	-56.25	82.81	325.8	1	0	35	52
				27	46.88	-87.50	151.8	0	1	29	55					59	-46.88	87.50	331.8	1	0	29	55
		7	14	28	37.50	-92.19	157.9	0	1	23	58			15	30	60	-37.50	92.19	337.9	1	0	23	58
				29	29.69	-95.31	162.7	0	1	18	60					61	-29.69	95.31	342.7	1	0	18	60
			15	30	18.75	-98.44	169.2	0	1	11	62				31	62	-18.75	98.44	349.2	1	0	11	62
				31	9.38	-100.00	174.6	0	1	5	63					63	-9.38	100.00	354.6	1	0	5	63
	4	8	16	32	0.00	-100.00	180.0	0	1	0	63		0	0	0	0	0.00	100.00	0.0	0	0	0	63

Each of the 16 values written to the phase table is a 6-bit number that determines the current trip point for the associated step. The highest value, 63, represents the maximum phase current, I_{PMAX}, defined in the section of the specification on phase current control. Other numbers represent a percentage of I_{PMAX}. For example, the number 23 sets the phase current trip point to 23/63 = 36.51% of I_{PMAX}.

There are two restrictions when using the phase table load capability:

- The required current profile must conform to the symmetry shown in figure 12. The forward (positive) current part must be symmetrical about Step Angle Number16 for phase A and about 0 for phase B. The reverse (negative) current part must be symmetrical about Step Angle Number 48 for phase A and about 32 for phase B. The forward and reverse profiles for each phase must be the same.
- The phase current must be zero at Step Angle Numbers 0 and 32 for phase A and Step Angle Numbers 16 and 48 for phase B.

Phase Current Table Programming Example

As an example of programming the phase current table, consider the current profile shown in figure 13. This shows a profile where the torque from each phase is required to be relatively higher at the detent points, that is, the points where only one phase is active. (This current profile does not relate to any specific motor, it is only shown as an example.)

Figure 13 shows the required current for each phase at each Step Angle Number as a percentage of the maximum phase current, I_{PMAX}, defined above. The waveform conforms to the required symmetry and zero crossing restrictions, so the profile for phase A for Step Angle Numbers from 0 to 16 (outlined and shaded) can be used to determine the phase table contents.

The first step is to digitize the profile into microsteps and the percentage values into 6-bit numbers, as shown in figure 14.

At each of the one-sixteenth microsteps, identified by Step Angle Number, the value of the phase current, as a percentage of the maximum phase current, I_{PMAX}, is digitized to a 6-bit value from 0 to 63. The value 63 represents 100% of I_{PMAX}, 32 represents

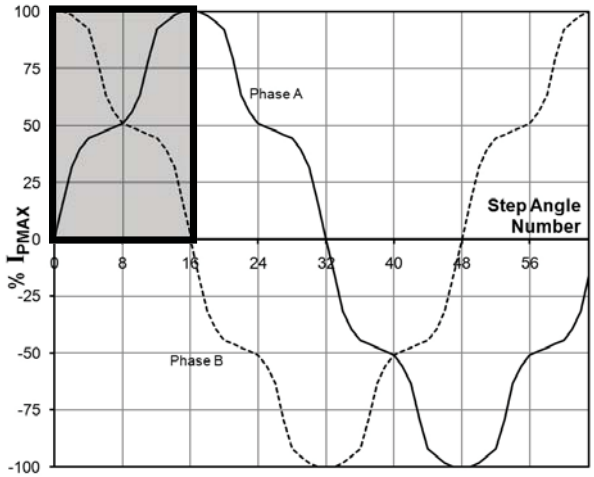


Figure 13. Example current profile

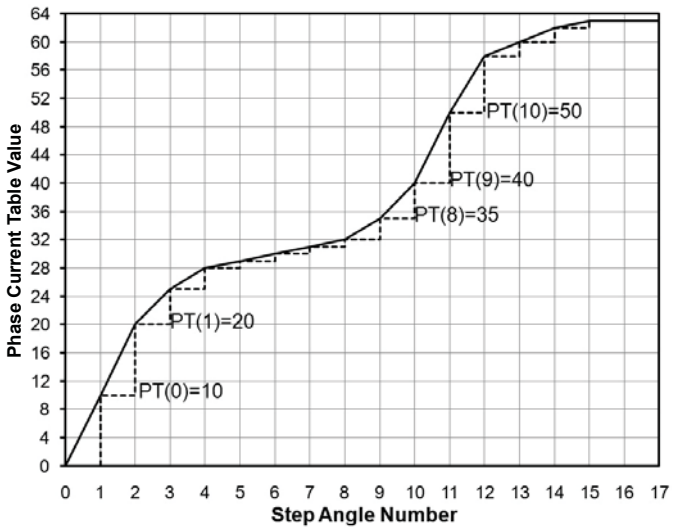


Figure 14. Digitizing the example current profile

32/63=50.8% and so on. The value at each Step Angle Number is then assigned to its corresponding phase table values as follows:

$$PT(n-1) = DI_n$$

where DI_n represents the digitized value of the current at Step Angle Number n.

A selection of the values and the corresponding phase current table entries is shown in figure14. The full set of phase current table values is shown in the table below.

Step	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Value	10	20	25	28	29	30	31	32	35	40	50	58	60	62	63	63
PT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

These 16 values are then loaded sequentially into the phase current table through the Phase Table Load register of the serial interface. Each value is then distributed to the appropriate Step Angle Numbers as described above and as shown in table 4C in the Phase Table Load Register section.

A representation of the final result is shown in figure 15. This is the digitized version of the required current profile shown in figure 13.

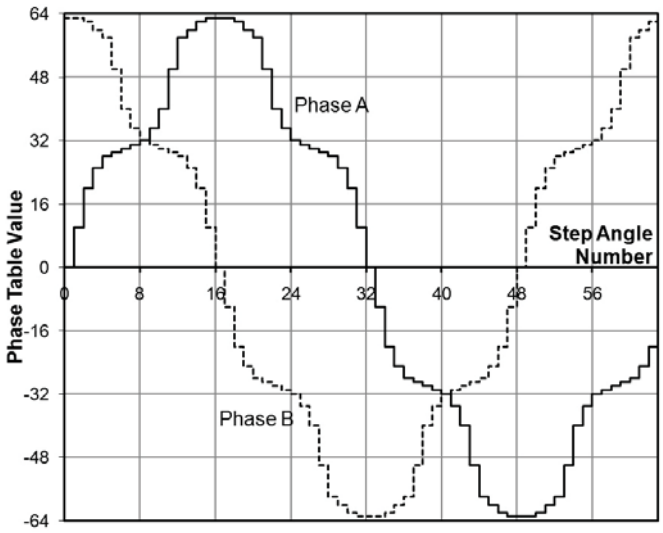


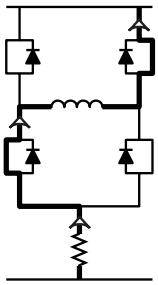
Figure 15. Resulting example current profile

Power Dissipation

The A4980 is a power circuit, therefore careful consideration must be given to power dissipation and the effects of high currents on interconnect and supply wiring.

A first order approximation of the power dissipation in the A4980 can be determined by examining the power dissipation in each of the two bridges during each of the operation modes. When synchronous rectification is used current will flow most of the time through the DMOS transistors that are switched on. When synchronous rectification is not used the current will flow through the body diode of the DMOS transistors during the decay phase. The use of fast or slow decay will also affect the dissipation. All the above combinations can be calculated from five basic DMOS output states as shown in figure 16.

Synchronous Fast Decay

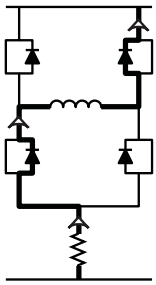


- Diagonally opposite DMOS output transistors are on
- Current flows from ground through load to positive supply

Dissipation is I^2R losses in the DMOS transistors:

$$P_{D(SF)} = I^2 \times (R_{DS(on)H}+R_{DS(on)L})$$

Non-Synchronous Fast Decay

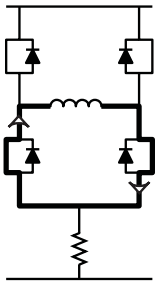


- Diagonally opposite body diodes conducting
- Current flows from ground through load to positive supply

Dissipation is IV losses in the diodes:

$$P_{D(NF)} = I \times (V_{FH} + V_{FL})$$

Synchronous Slow Decay

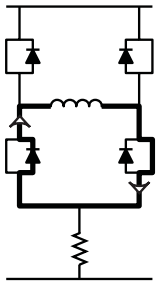


- Both low-side DMOS output transistors are on
- Current circulates through both transistors and the load

Dissipation is I^2R losses in the DMOS transistors:

$$P_{D(SS)} = I^2 \times (2 \times R_{DS(on)L})$$

Non-Synchronous Slow Decay

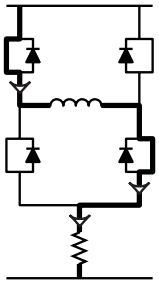


- One low-side DMOS output transistor and one body diode conducting
- Current circulates through the diode, the transistor and the load

Dissipation is I^2R losses in the DMOS transistors plus IV loss in the diode:

$$P_{D(NS)} = (I^2 \times R_{DS(on)L})/(I \times V_F)$$

Drive Current Ramp-up



(Used in all combinations)

- Diagonally opposite DMOS output transistors are on
- Current flows from positive supply through load to ground

Dissipation is I^2R losses in the DMOS transistors:

$$P_D = I^2 \times (R_{DS(on)H} + R_{DS(on)L})$$

Figure 16. Basic output states

The total power dissipation for each of the four decay modes, $P_{D(TOT)XX}$, is the average power for the drive current ramp portion, P_D, and the drive current decay portion, $P_{D(XX)}$ of the PWM cycle. For slow decay the current will be rising for approximately 20% of the cycle and decaying for approximately 80%. For fast decay the ratio will be approximately 50%. Note that these are approximate figures and will vary slightly depending on the motor characteristics and the use of synchronous rectification. The following formulas may be used to estimate total power dissipation:

- Synchronous slow decay mode

$$P_{D(TOT)SS} = 0.2 \times P_D + 0.8 \times P_{D(SS)}$$

$$P_{D(TOT)SS} = 0.2\,(I^2\,[R_{DS(on)H} + R_{DS(on)L}]) + 0.8\,(I^2 \times 2 \times R_{DS(on)L})$$

- Non-synchronous slow decay mode

$$P_{D(TOT)NS} = 0.2 \times P_D + 0.8 \times P_{D(NS)}$$

$$P_{D(TOT)NS} = 0.2\,(I^2\,[R_{DS(on)H} + R_{DS(on)L}]) + 0.8\,(I^2 \times R_{DS(on)L} + I \times V_F)$$

- Synchronous fast decay mode

$$P_{D(TOT)SF} = 0.5 \times P_D + 0.5 \times P_{D(SF)}$$

$$P_{D(TOT)SF} = I^2\,(R_{DS(on)H} + R_{DS(on)L})$$

- Non-synchronous fast decay mode

$$P_{D(TOT)NF} = 0.5 \times P_D + 0.5 \times P_{D(NF)}$$

$$P_{D(TOT)NF} = 0.5(I^2\,[R_{DS(on)H} + R_{DS(on)L}]) + 0.5(I \times [V_{FH} + V_{FL}])$$

An approximation of the total dissipation can be calculated by summing the total power dissipated in both bridges and adding the control circuit power due to $V_{BB} \times I_{BB}$ and $V_{DD} \times I_{DD}$.

The total power at the required ambient temperature can then be compared to the allowable power dissipation shown in figure 17. For critical applications, where the first order power estimate is close to the allowable dissipation, the power calculation should take several other parameters into account including: motor parameters, dead time, and switching losses in the controller.

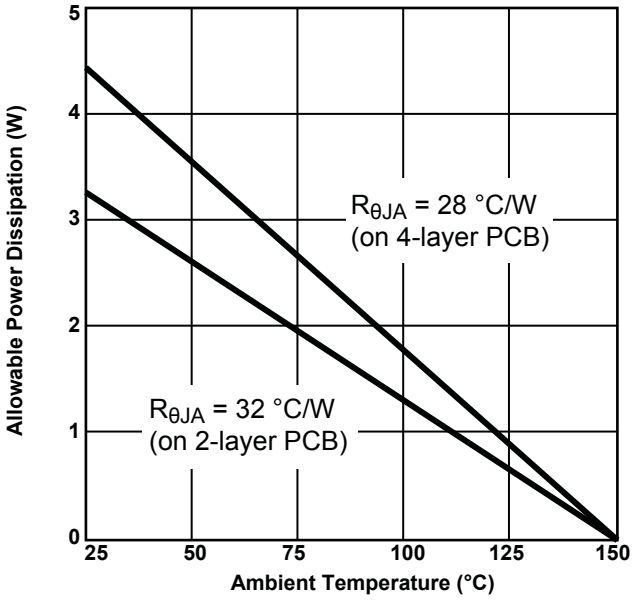


Figure 17. Allowable power dissipation, on typical PCBs

Layout

Traces

PCB The printed circuit board (PCB, or printed wiring board) should use a higher weight copper thickness than a standard small signal or digital circuit board. This helps to reduce the impedance of the printed traces when conducting high currents. PCB traces carrying switching currents should be as wide and short as possible to reduce the inductance of the trace. This will help reduce any voltage transients caused by current switching during PWM current control.

For optimum thermal performance, the exposed thermal pad on the underside of the A4980 should be soldered directly onto the board. A solid ground plane should be added to the opposite side of the board, and multiple vias through the board to the ground plane should be placed in the area under the thermal pad.

Decoupling

All supplies should be decoupled with an electrolytic capacitor in parallel with a ceramic capacitor. The ceramic capacitor should have a value of 100 nF and should be placed as close as possible to the associated supply and ground pins of the A4980. The electrolytic capacitor connected to VBB should be rated at least 1.5 times the maximum circuit voltage, and selected to support the maximum ripple current provided to the motor. The value of the capacitor is unimportant but should be the lowest value with the necessary ripple current capability.

The pump capacitor between CP1 and CP2, the pump storage capacitor between VCP and VBB, and the compensation capacitor between VREG and ground should be connected as close as possible to the respective pins of the A4980.

Grounding

A star ground system, with the common star point located close to the A4980, is recommended. The reference ground, AGND (pin 7), and the power ground, PGND (pin 21), must be connected together externally. The copper ground plane located under the exposed thermal pad is typically used as the star ground point.

Current Sense Resistor

In sensing the output current level, to minimize inaccuracies caused by ground-trace IR drops, the current sense resistor (R_S) should have an independent ground return to the star ground point. This path should be as short as possible. For low-value sense resistors, the IR drop in the PCB trace to the sense resistor can be significant and should be taken into account. Surface mount chip resistors are recommended to minimize contact resistance and parasitic inductance. The value, R_S, of the sense resistor is given by:

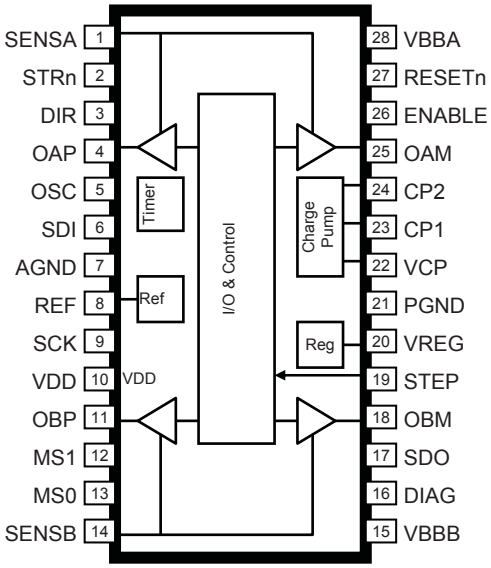
$$R_S = \frac{V_{REF}}{16 \times I_{SMAX}}$$

There is no restriction on the value of R_S or V_{REF}, other than the range of V_{REF} over which the output current precision is guaranteed. However, it is recommended that the value of V_{REF} be kept as high as possible to improve the current accuracy. The table below provides increasing values of I_{SMAX} for suggested values of V_{REF} and standard E96 values of R_S.

Suggested Values

I_{SMAX} (mA)	R_S (mΩ)	V_{REF} (V)
100	499	0.8
200	499	1.6
300	417	2.0
405	309	2.0
501	249	2.0
610	205	2.0
702	178	2.0
812	154	2.0
912	137	2.0
1008	124	2.0

Pin-out Diagram

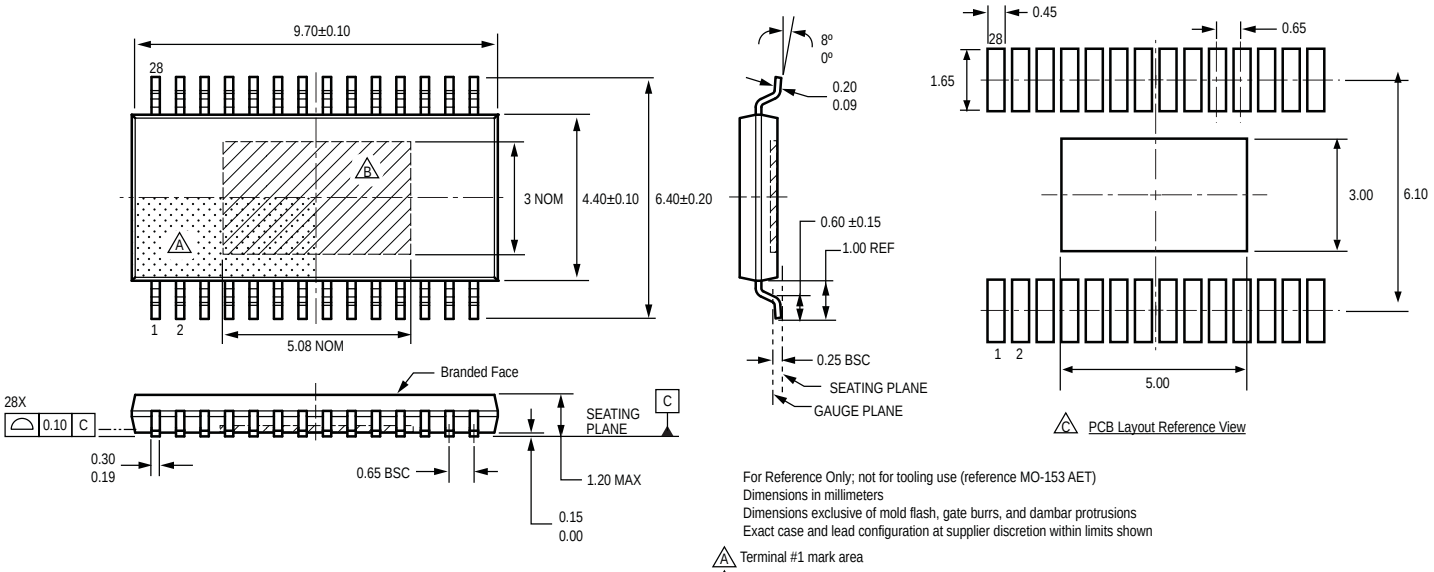


Terminal List Table

Name	Number	Description
AGND	7	Analog reference ground
CP1	24	Charge pump capacitor terminal
CP2	23	Charge pump capacitor terminal
DIAG	16	Diagnostic output
DIR	3	Direction select input
ENABLE	26	Bridge enable input
MS0	13	Microstep select input
MS1	12	Microstep select input
OAM	25	Bridge A negative output
OAP	4	Bridge A positive output
OBM	18	Bridge B negative output
OBP	11	Bridge B positive output
OSC	5	Oscillator input
PAD	–	Connect exposed tab to ground

Name	Number	Description
PGND	21	Power Ground
REF	8	Reference input voltage
RESETn	27	Chip reset
SCK	9	Serial data clock
SDI	6	Serial data input
SDO	17	Serial data output
SENSA	1	Current sense node – bridge A
SENSB	14	Current sense node – bridge B
STEP	19	Step input
STRn	2	Serial data strobe
VBBA	28	Motor supply – bridge A
VBBB	15	Motor supply – bridge B
VCP	22	Above supply voltage
VDD	10	Logic Supply
VREG	20	Regulated voltage

Package LP, 28-Pin TSSOP with Exposed Thermal Pad



For Reference Only; not for tooling use (reference MO-153 AET)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Appendix A. Driving a Stepper Motor

A stepper motor is a particular form of brushless DC motor. As for any electric motor, motion is created by magnetic interaction between the stationary part of the motor, known as the stator, and the moving part of the motor, known as the rotor. The information presented here concentrates on a specific type of motor known as a hybrid stepper motor. This is the most common type of small stepper motor. It uses permanent magnets in the rotor to produce one set of constant magnetic fields and electromagnets in the stator to produce another set of varying magnetic fields. The term hybrid relates to the use of both electromagnets and permanent magnets.

Comparing Bipolar and Unipolar Motors

There are two options in small hybrid stepper motor construction. In the first, known as a unipolar stepper motor, there are independent electromagnets to generate each magnetic polarity, so two electromagnets are required per phase. Each of these is energized with current in only one direction, producing a single magnetic field direction (unipolar). Because the current in each electromagnet only flows in a single fixed direction, the control circuit can be very simple. The drawback is that only one electromagnet per phase can be energized at any time so, at most, only half of the motor volume is ever used to create torque on the rotor.

A bipolar motor, in contrast, uses each electromagnet to produce two opposing fields (bipolar) at different times, by allowing the current to flow in both directions. This means that the motor volume required for a bipolar motor is half of the volume required for a unipolar motor for the same torque output. The minor drawback is that a bipolar motor requires a more complex drive circuit in order to reverse the forcing voltage across the coil of the electromagnet. However, if the drive circuit is integrated into a single IC then the drive becomes cost effective. This, along with the improvement in torque output makes the bipolar motor a better solution for applications where the volume available is restricted. For this reason the following information will relate only to bipolar motors.

In order to create continuous motion in one direction it is necessary to have two or more sets of electromagnets, that is, two or more phases. The simplest and most cost effective configuration for a stepper motor is to have two phases. For some applications that require an extremely low torque ripple, 3 phase, 5 phase, and even 9 phase stepper motors are sometimes used. However, the remainder of the information presented here relates specifically to 2-phase bipolar motors.

Moving a 2-Phase Bipolar Stepper Motor

Figure A1 shows the four possible current combinations in two phase windings, A and B, and the effect on a simplified representation of part of a stepper motor. In each case the stator with the electromagnets is shown at the top of the diagram and the rotor with the permanent magnets is shown at the bottom of the diagram.

In figure A1 the stator consists of alternate phase A and phase B electromagnets. The winding direction of the electromagnet changes for each sequential electromagnet in each phase as indicated by the overbar above the phase letter and identified below as *A-bar* and *B-bar*. The result is that the magnetic poles will alternate for each sequential electromagnet of each phase. That means, for example, when the A electromagnet produces a north (N) magnetic pole at the end nearest to the rotor, then the A-bar electromagnet will produce a south (S) magnetic pole at the end nearest to the rotor.

The windings for all the A and A-bar electromagnets are connected in series and driven by a single full bridge. Similarly the windings for all the B and B-bar electromagnets are connected in series and driven by another single full bridge. So a 2-phase bipolar stepper motor requires two full bridges for full control.

The rotor is much simpler than the stator, and consists of a solid base holding permanent magnets with alternating pole directions. There are no windings on the rotor, so there is no requirement to conduct current to the moving part of the motor. In addition the lack of current and windings means that there is no heat generated in the rotor, making cooling of the moving parts much simpler.

The diagrams in figure A1 provide a representation of a small section of the mechanics of the motor. In practice the motor structure is a little different from this, but the principle of operation is the same.

Starting at the top, panel (a) in figure A1, the current is flowing down through the phase A winding from top to bottom and there is no current in phase B. The result is an N magnetic pole on the A electromagnets and an S pole on the A-bar electromagnets. The rotor position is such that that the poles of the permanent magnets align with the poles of the electromagnets, N to S.

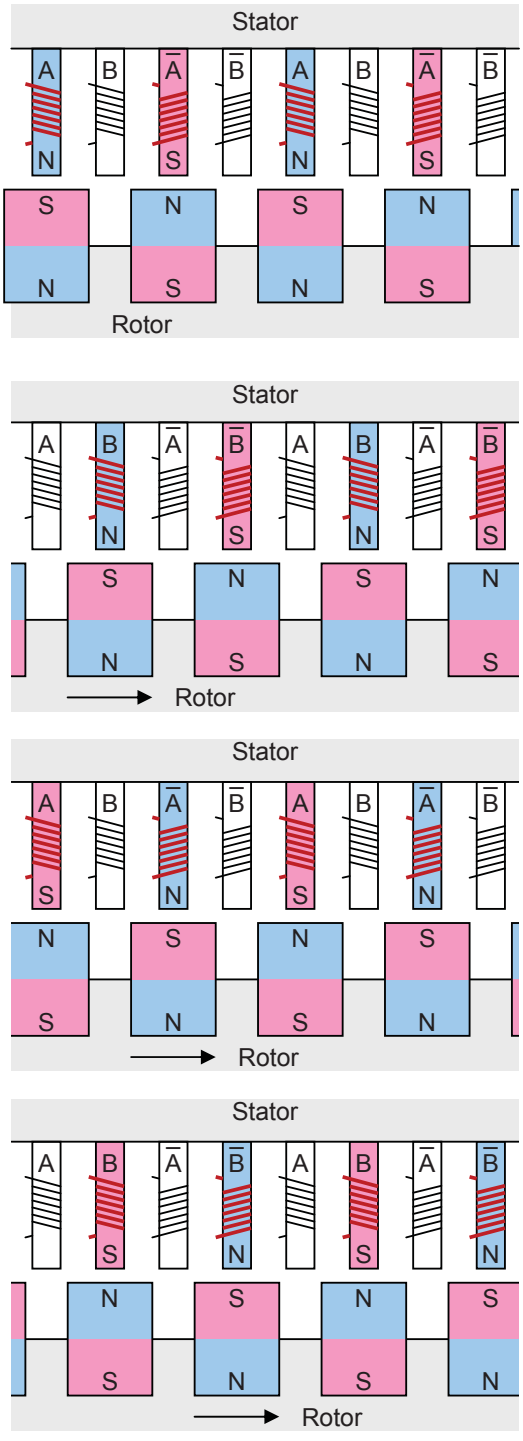


Figure A1. Basic principle of bipolar stepper motor operation

In the next panel, panel (b), the current is flowing down through the phase B winding from top to bottom and there is no current in phase A. The result is an N pole on the B electromagnets and an S pole on the B-bar electromagnets. These magnetic poles will attract and repel the permanent magnets on the rotor producing a force that moves the rotor from left to right in the diagram until the poles of the permanent magnets again align with the poles of the electromagnets.

In panel (c), the current is flowing up through the phase A winding from bottom to top and there is no current in phase B. This reverses the pole orientation from the top panel, such that there is an S pole on the A electromagnets and an N pole on the A-bar electromagnets. As before, these magnetic poles will attract and repel the permanent magnets on the rotor producing a force that moves the rotor from left to right in the diagram, until poles of the permanent magnets again align with the poles of the electromagnets.

The bottom panel, panel (d), shows the final combination with current flowing up through the phase B winding from bottom to top and there is no current in phase A. This produces an N pole on the B electromagnets and a S pole on the B-bar electromagnets. As before, these magnetic poles will attract and repel the permanent magnets on the rotor producing a force that moves the rotor from left to right until poles of the permanent magnets again align with the poles of the electromagnets.

Each of the four steps in figure A1 represents a single full mechanical step of the stepper motor. The four steps together represent a single electrical cycle.

The step resolution depends entirely on the mechanical construction of the motor and typically there will be 200 or more full steps per mechanical revolution of the motor. A 200-step motor will provide a resolution of 360 / 200 = 1.8° of rotation per step.

Stepping in the opposite direction to that described above is simply a case of changing the step sequence or inverting one of the phase current directions.

Microstepping

In many applications it is necessary to improve the resolution of the stepper motor, for more precise positioning control, or simply to increase the number of steps per revolution to reduce the torque ripple and therefore the vibration and noise of the motor. Fortunately this can be achieved by driving both phases at the same time in order to move the rotor to a position between two electromagnets. This is known generically as microstepping.

Figure A2 shows the basic principle of microstepping. Panels (a) and (c) of figure A2 correspond to panels (a) and (b) of figure A1. Panel (b) shows both phases energized such that there are now two adjacent N poles and two adjacent S poles. In this example the currents in each phase is the same, and so the S and N poles of the rotor now move to half way between the positions in diagrams (a) and (c). Figure A2 only shows a single mechanical step in total, which is one quarter of a full electrical cycle. This sequence is the lowest resolution form of microstepping, known as *half step*, and is the simplest method of driving a stepper motor in half-step mode.

The currents are switched-on in the correct direction in sequence and no current control is required. The current is simply defined,

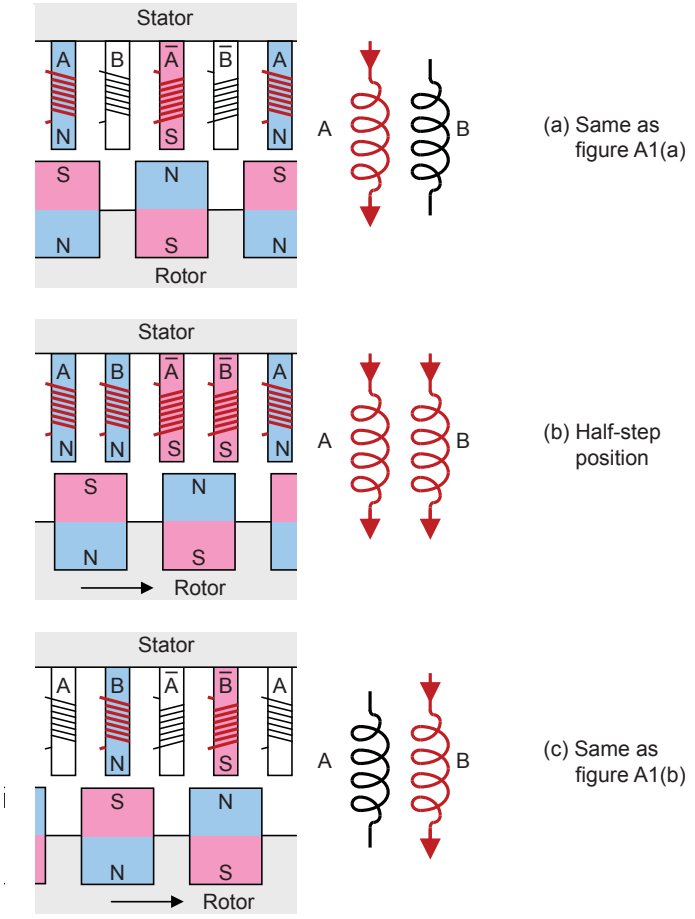


Figure A2. Half step operation

in the first instance, by the resistance of the winding and the applied voltage.

From figure A2(b) it is also apparent that varying the relative current in each phase will make it possible to move the rotor to any intermediate position between the four positions of figure A1, which occur when only a single phase is energized. When there is one intermediate position this is known as half step. When there are three intermediate positions this is known as *quarter step* and so on. Higher resolution microstepping is described in more detail below.

Phase Current-Sequence Diagrams

Figure A3 shows the full sequence of the two phase currents illustrated in figure A2. This shows two electrical cycles, equivalent to 4 full mechanical steps (8 half steps). The full-step positions are marked *F* and the half-step positions are marked *H*. Each half step in the electrical cycle is numbered, from 0 to 7, for reference later.

This figure shows that, when discussing stepper motor control, it is necessary to know the relative magnitude and direction of the current in each phase. So, rather than use physical representations of the motor, such as in figure A1 and A2, or simple time-based current waveforms, such as figure A3, it is simpler to use a phase diagram. For a 2-pole bipolar motor this diagram is created by plotting the current in the two phases as orthogonal vectors, that is, as vectors at 90° to each other as shown in figure A4.

Phase Current-Phase Diagrams

Figure A4 shows the currents of figure A3 plotted on a phase diagram where the phase A current is represented by the vertical line and the phase B current by the horizontal line. The half-step numbers correspond to the numbers in figure A3. For example, at step 1 in figure A3, the phase A current and the phase B current are both positive and with the same magnitude. These two currents are shown in figure A4 as the two solid arrows. Adding these two current vectors together gives the resultant motor current vector indicated. The resultant is the hypotenuse of a right-angled triangle with the two other sides equal. If the other two sides are assumed to be 1 then the magnitude of the hypotenuse will be:

$$\sqrt{1^2 + 1^2} = \sqrt{2} = 1.\mathbf{4}$$

So the resultant current vector will be 141% of the value of the current in phase A or B, positioned at 45°.

Torque Ripple

Now, the torque output of any electrical motor is directly proportional to the magnitude of the motor current, and the motor current is the resultant phase current. It is clear from figure A4 that the resultant phase current at the half-step position is higher than the current at the full-step position. This means that the motor torque will be changing as the motor rotates, resulting in what is known as *torque ripple*. Torque ripple in any rotating system will cause mechanical vibration and will result in increased audible noise and possible wear on other mechanical components. Torque ripple can be reduced by ensuring that the resultant current at the half-step point has the same magnitude as the full current in the single phase at the full-step positions.

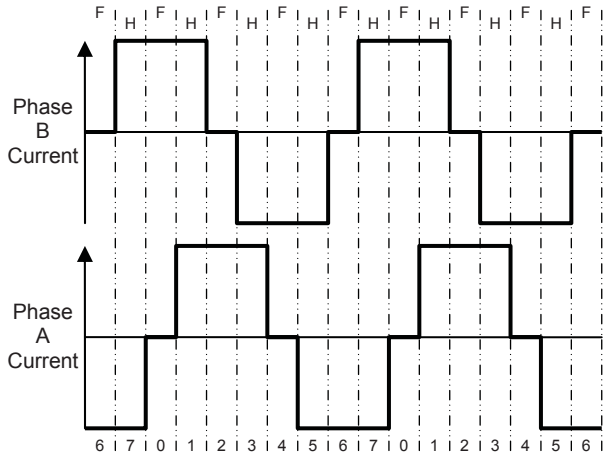


Figure A3. Phase current sequence for simple half step

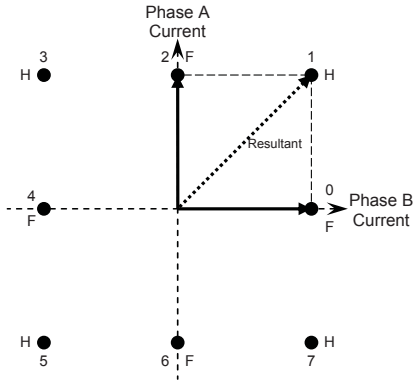


Figure A4. Phase diagram for simple half step

Improved Half Step

Figure A5 shows a circle superimposed on the phase diagram. This circle represents the required locus of the resultant phase current vectors to maintain 100% current magnitude. At the full-step positions, 0, 2, 4, and 6, only one phase is active and the magnitude of the phase current is at 100%. At the half-step positions, 1, 3, 5, and 7, both phases are active. To ensure that the magnitude of the resultant current is 100%, the magnitude of each phase current must be 70.7%. Calculating the value of the resultant current as before gives a resultant current of 100%.

$$\sqrt{0.707^2 + 0.707^2} = \sqrt{0.5 + 0.5} = \sqrt{1} = 1$$

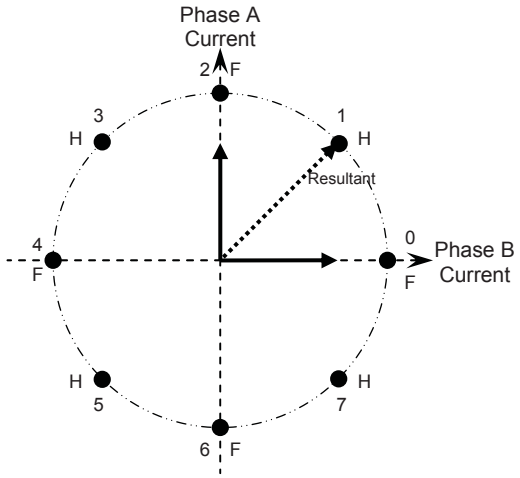


Figure A5. Phase diagram for improved half step

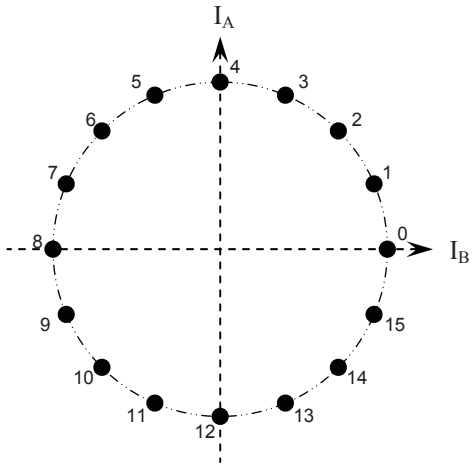


Figure A6. Phase diagram for quarter step

The current vectors at half-step position 1 are shown specifically to illustrate that the magnitude of the resultant sits on the 100% circle.

For a standard stepper motor to operate with minimum torque ripple, the resultant current must always lie on the constant torque circle irrespective of the number of microsteps. For higher resolution microstepping this then defines the relative phase currents at each microstep position.

Quarter Step

For example consider the next resolution in microstepping; quarter step. The locus of the required phase currents are shown in figure A6. The required current level in each phase can be calculated using simple trigonometry. For example, consider microstep position 7 in figure A6 as detailed in figure A7.

There are 4 quarter steps for each full step. A full step on the phase diagram is represented by 90°. So each quarter step increments the phase angle by 90° / 4 = 22.5°.

In figure A7 the resultant motor current at quarter-step position 8 is one quarter step from the horizontal, so it is at 22.5°. The magnitude of the current in phase A at quarter-step position 7, I_{A7}, is therefore sin 22.5°, which is equal to 0.383 or 38.3% of the maximum current.

Similarly, the magnitude of the current in phase B at quarter-step position 7, I_{B7}, is therefore cos 22.5°, which is equal to 0.924 or 92.4% of the maximum current.

At the 45° positions, 2, 6, 10 and 14, the magnitude of the current in phase A and phase B will be cos 45° = 0.707 or 70.7%, which is the same magnitude as in the half-step case shown in figure A5. Due to symmetry, the phase A current is the same at quarter-step positions 7 and 1. The phase A current at quarter-step positions 9 and 15 also has the same magnitude, but the current is in the

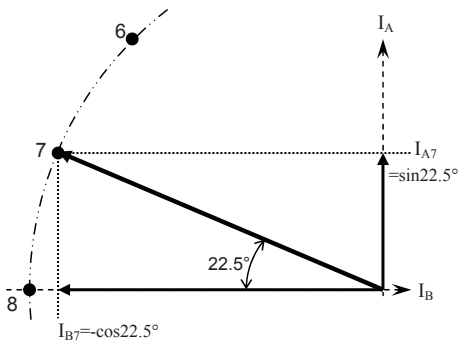


Figure A7. Calculating phase current magnitudes

opposite direction. In addition the phase B current at quarter-step positions 3, 5, 11, and 13 also have the same magnitude as that of phase A at quarter-step position 7, with a positive current direction for steps 3 and 13 and a negative direction for steps 5 and 11. Similar symmetry can be applied to the phase B current at quarter-step position 7, calculated above.

This means that only five discrete current magnitudes are required, including 0% and 100%, in order to drive the stepper motor to all 16 quarter-step positions. Using the same nomenclature as figure A7, that is, I_{Pn}, where P is the phase, A or B, and n is the quarter-step number from figure A6, table A1 shows where each of the five magnitude values are used.

Figure A8 shows these values plotted as a current sequence diagram. This figure is therefore the time-based equivalent of the phase diagram in figure A6.

Table A1. Quarter-Step Phase Current Magnitudes

Magnitude (%)	Phase B				Phase A			
0	I_{A0}	–	I_{A8}	–	–	I_{B4}	–	I_{B12}
38.3	I_{A1}	I_{A7}	I_{A9}	I_{A15}	I_{B3}	I_{B5}	I_{B11}	I_{B13}
70.7	I_{A2}	I_{A6}	I_{A10}	I_{A14}	I_{B2}	I_{B6}	I_{B10}	I_{B14}
92.4	I_{A3}	I_{A5}	I_{A11}	I_{A13}	I_{B1}	I_{B7}	I_{B9}	I_{B15}
100	–	I_{A4}	–	I_{A12}	I_{B0}	–	I_{B8}	–

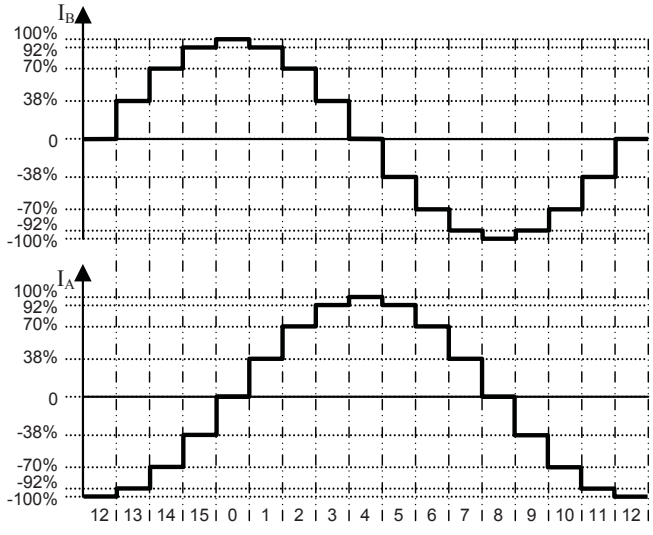


Figure A8. Phase current sequence for quarter step

Higher Microstep Resolution

The principles described above can easily be extended to higher microstep resolutions. As the microstep resolution increases, it becomes more apparent that the phase current sequences approximate ever closer to a sin and cosine function. Figure A9 shows the measured phase current sequence of the A4980 running in sixteenth-step mode. The phase current sequences for eighth-step and sixteenth-step resolutions are shown in figures A10 and A11.

Most applications using small motors are limited to sixteenth-step mode due to the mechanical precision of the motor. Larger, high-precision stepper motors are sometimes driven at 32, 64, or even up to 256 microsteps in some extreme cases.

Practical Implementation

A system to drive a stepper motor with microstep capability requires sequencers, current reference generators, and current controllers. Developing such a system from discrete components, or even using a fast microcontroller, is a complex task. The A4980 is one of several fully integrated stepper drivers that are available with microstep resolutions, from simple half step to sixteenth step and higher, using programmable current tables. All aspects of the stepper control system are included in these single chip solutions and many of them can be controlled by a simple Step and Direction interface.

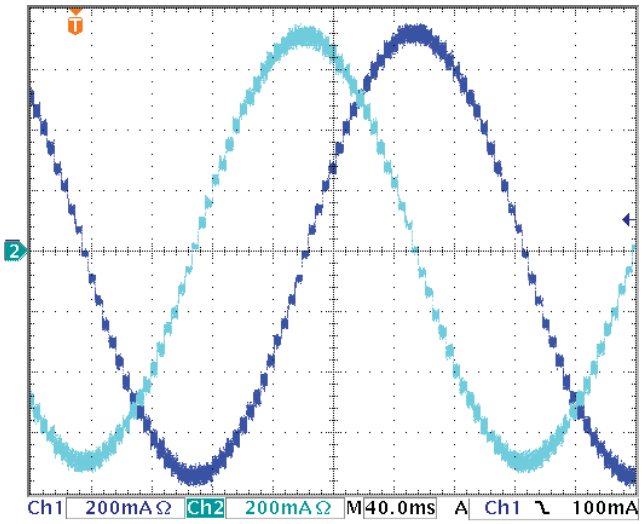


Figure A9. Measured sixteenth-step phase current sequence

Practical limitations

The information presented here assumes ideal stepper motors being stepped slowly, with accurate, efficient current control circuits. In practice the stepper motor phase windings are represented by two non-ideal inductors and the motor may be driven at a high stepping rate.

A high stepping rate will produce a back EMF, like any other motor, that will act against any current control circuits. The current control circuits must also be able to work with inductive loads. In general the current control circuit will be a PWM current control scheme to make the driver as efficient as possible and reduce the dissipation in the driver.

Like any other motor, the back EMF will also limit the maximum stepping rate of the motor. As the motor speed increases the back EMF will increase. When it reaches a value close to the supply voltage the resulting voltage difference will be insufficient to drive the phase current required to produce the necessary output torque. When this occurs the motor will stall and slip out of synchronization with the driving circuit.

The mechanical precision of the motor will also have an effect on the overall performance of the system. If the effect of the motor windings on the rotor are non-linear then the relationship between current and torque may not be linear. The magnitude of the currents at each microstep may then require a relationship other than sinusoidal. The A4980 and a few other integrated drivers are able to accommodate this by allowing the phase current values for each microstep position to be reprogrammed. In most systems this effect will be very small and can be ignored but in some cases some improvement in torque ripple and audible noise can be achieved.

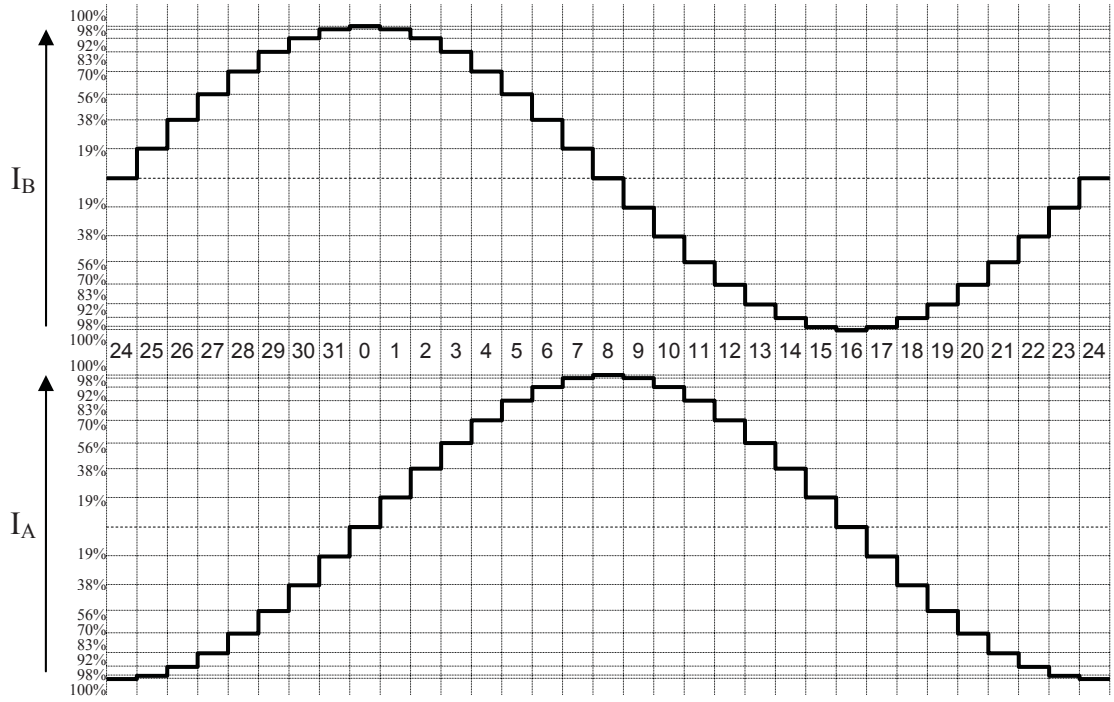


Figure A10. Phase current sequence for eighth step

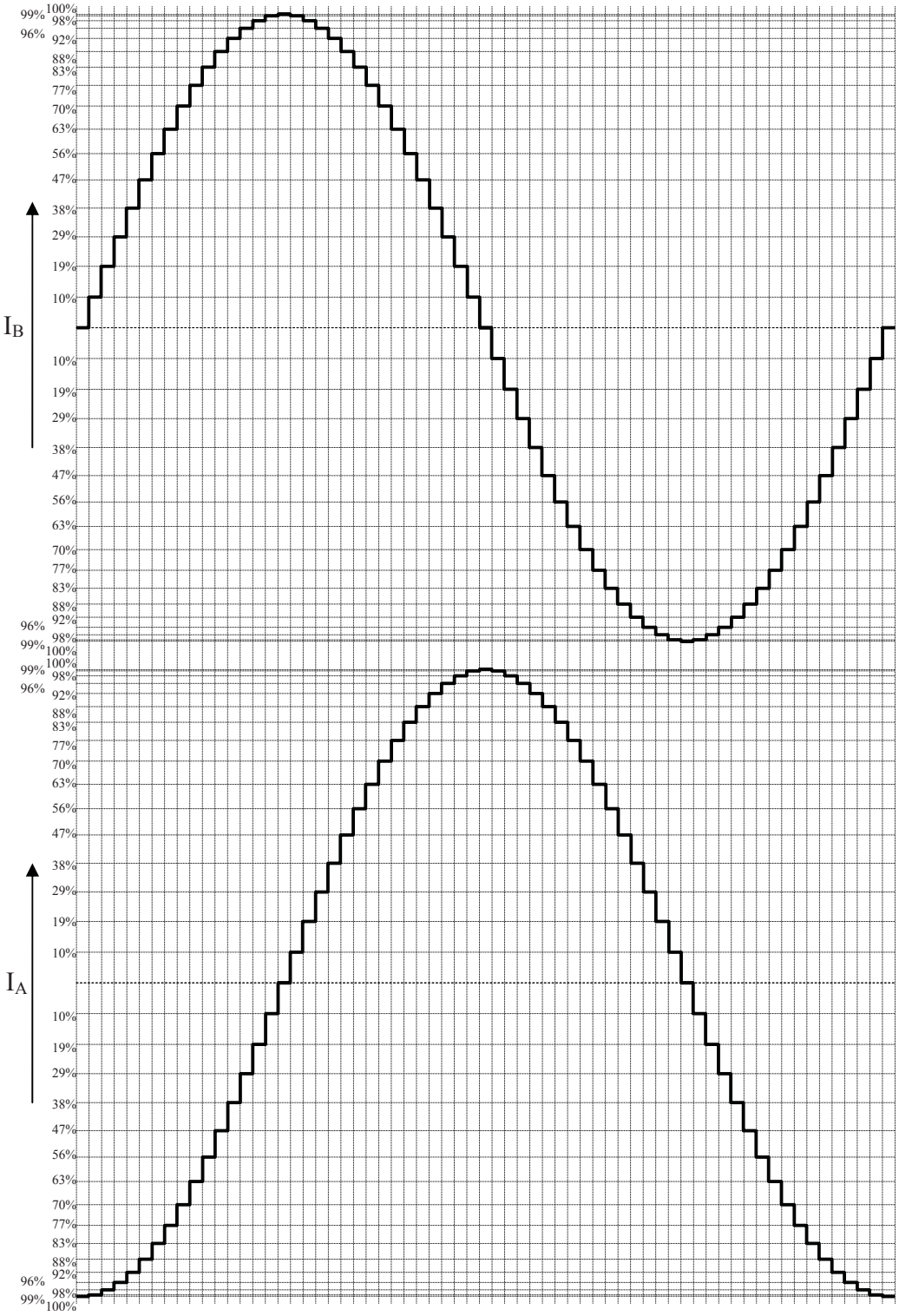


Figure A11. Phase current sequence for sixteenth step

Revision History

Revision	Revision Date	Description of Revision
Rev. 2	September 19, 2011	Update features list

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