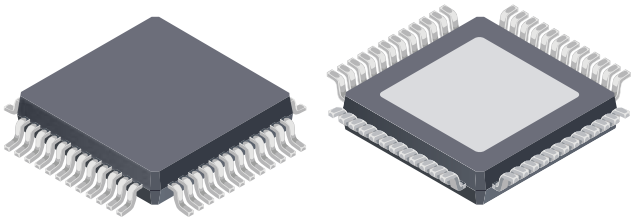
Automotive 3-Phase MOSFET Driver

Features and Benefits

- High current 3-phase gate drive for large N-channel MOSFETs
- Pin compatible with Allegro® A4935KJP
- Cross-conduction protection with adjustable dead time
- Top-off charge pump for 100% PWM
- Charge pump for low supply voltage operation
- Uncommitted current sense amplifier
- 5.5 to 50 V supply voltage range
- Compatible with 3.3 V and 5 V logic
- Extensive diagnostic outputs
- Low-current sleep mode

Package: 48-pin LQFP with exposed thermal pad (suffix JP)



Not to scale

Description

The A4933 is a 3-phase controller for use with N-channel external power MOSFETs and is specifically designed for automotive applications.

A unique charge pump regulator provides full (>10 V) gate drive for battery voltages down to 7 V and allows the A4933 to operate with a reduced gate drive, down to 5.5 V.

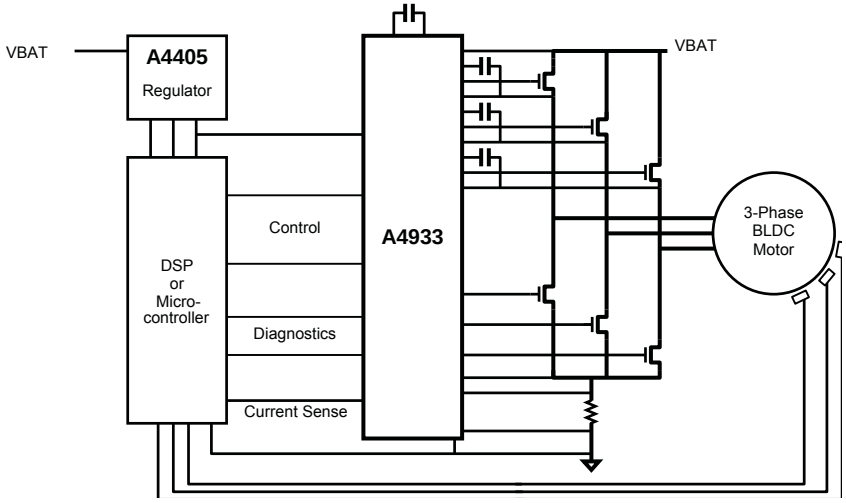
A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs. An internal charge pump for the high-side drive allows DC (100% duty cycle) operation.

Full control over all six power FETs in the 3-phase bridge is provided, allowing motors to be driven with block commutation or sinusoidal excitation. The power FETs are protected from shoot-through by integrated crossover control and resistor-adjustable dead time.

Bridge current can be measured using an integrated current sense amplifier. This is an uncommitted differential amplifier with a below-ground common mode range allowing it to be used in low-side current sense applications. Gain and offset are defined by external resistors.

Continued on the next page…

Typical Application



Description (continued)

Integrated diagnostics provide indication of undervoltage, overtemperature, and power bridge faults. They can be configured to protect the power FETs under most short circuit conditions. Detailed diagnostics are available as a serial data word.

The A4933 is supplied in a 48-pin LQFP with exposed thermal pad, (suffix JP). This is a small footprint (81 mm^2) power package. It is lead (Pb) free with 100% matte tin leadframe plating.

Selection Guide

Part Number	Packing
A4933KJPTR-T	1500 pieces per reel

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		–0.3 to 50	V
Logic Supply Voltage	V_{DD}		–0.3 to 7	V
VREG			–0.3 to 16	V
CP1 and CP2			–0.3 to 16	V
Logic Inputs and Outputs			–0.3 to 6.5	V
CSP and CSN			–4 to 6.5	V
LSS			–4 to 6.5	V
CSO and VDSTH			–0.3 to 6.5	V
SA, SB, and SC			–5 to 55	V
RDEAD			–0.3 to 6.5	V
VDRAIN			–5 to 55	V
GHA, GHB, and GHC			Sx to Sx+15	V
GLA, GLB, and GLC			–5 to 16	V
CA, CB, and CC			–0.3 to Sx+15	V
Operating Temperature Range	T_A	Range K	–40 to 150	ºC
Junction Temperature	T_J(max)		150	ºC
Transient Junction Temperature	T_{tJ}	Overtemperature event not exceeding 10 s, lifetime duration not exceeding 10 h, guaranteed by design characterization	175	ºC
Storage Temperature Range	T_{stg}		–55 to 150	ºC
ESD Rating, Human Body Model		AEC-Q100-002, all pins	2000	V
ESD Rating, Charged Device Model		AEC-Q100-011, all pins	1050	V

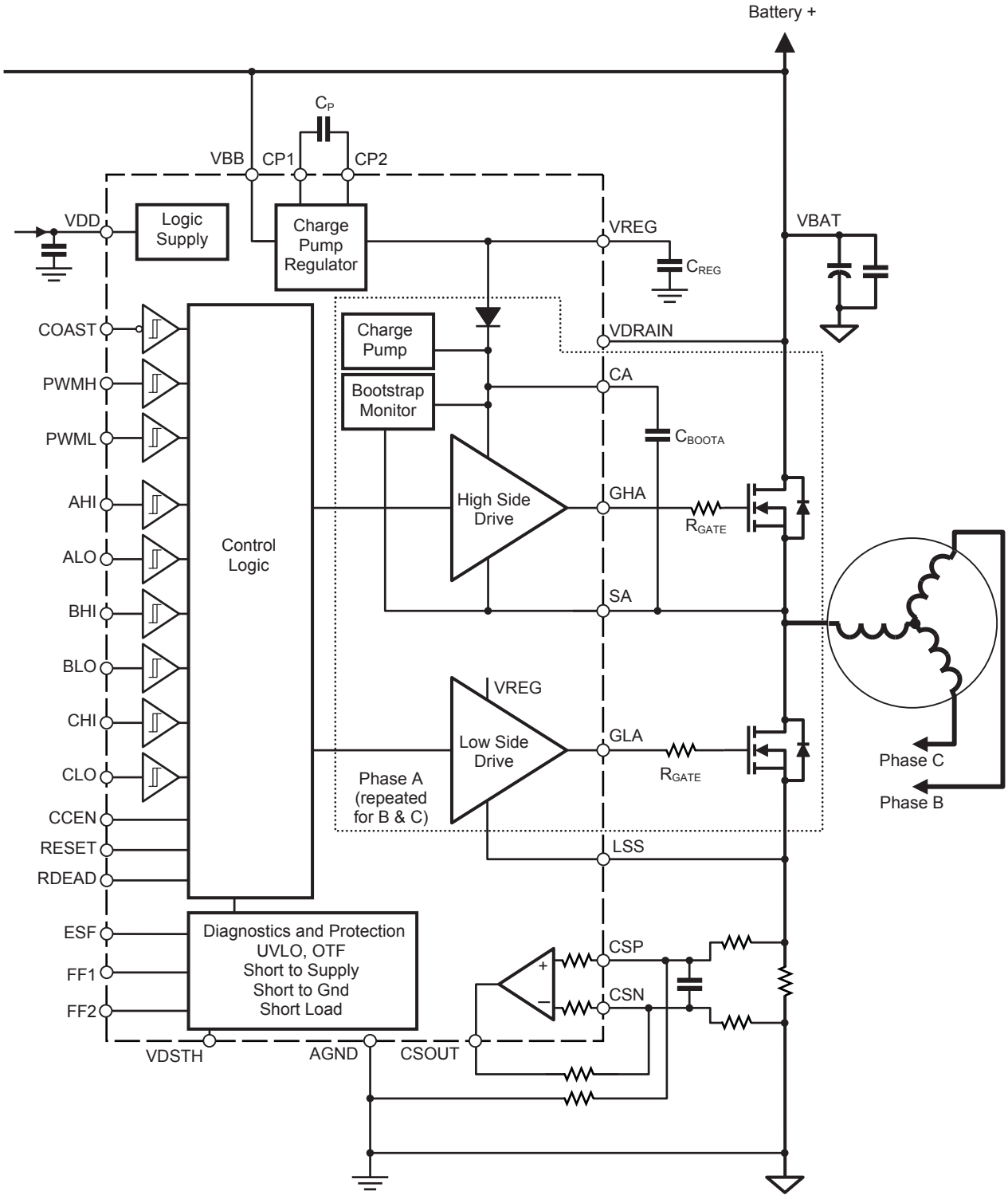
*With respect to AGND.

THERMAL CHARACTERISTICS may require derating at maximum conditions

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	23	ºC/W
		2-layer PCB with 3 $in.^2$ of copper area each side	44	ºC/W
	$R_{\theta JP}$		2	ºC/W

*Additional thermal information available on Allegro website.

Functional Block Diagram



ELECTRICAL CHARACTERISTICS valid at T_J = –40°C to 150°C, V_{DD} = 3 to 5.5 V, V_{BB} = 7 to 50 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply and Reference						
Load Supply Voltage Functional Operating Range[1]	V_{BB}		5.5	–	50	V
Load Supply Quiescent Current	I_{BBQ}	RESET = high, outputs = low, V_{BB} = 12 V	–	10	14	mA
	I_{BBS}	RESET = low, Sleep mode, V_{BB} = 12 V	–	–	10	µA
Logic Supply Voltage	V_{DD}		3.0	–	5.5	V
Logic Supply Quiescent Current	I_{DDQ}	RESET = high, outputs = low	–	4	6	mA
	I_{DDS}	RESET = low	–	–	10	µA
VREG Output Voltage	V_{REG}	V_{BB} > 9 V, I_{REG} = 0 to 50 mA	9	13	13.80	V
		7.5 V < V_{BB} ≤ 9 V, I_{REG} = 0 to 30 mA	9	13	13.80	V
		6 V < V_{BB} ≤ 7.5 V, I_{REG} = 0 to 17 mA	8.5	–	–	V
		5.5 V < V_{BB} ≤ 6 V, I_{REG} < 13 mA	7.5	9.5	–	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA	0.4	0.7	1.0	V
		I_D = 100 mA	0.6	1.0	1.2	V
Bootstrap Diode Resistance	r_D	$r_{D(100mA)}$ = ($V_{fBOOT(150mA)}$ – $V_{fBOOT(50mA)}$) / 100 mA	2	4	8	Ω
Bootstrap Diode Current Limit	I_{DBOOT}		500	1000	1500	mA
Top-off Charge Pump Current Limit	I_{TOCPM}		–	400	–	µA
High-Side Gate Drive Static Load Resistance	R_{GSH}		250	–	–	kΩ
Gate Output Drive						
Turn-On Time	t_r	C_{LOAD} = 10 nF, 20% to 80%	–	175	–	ns
Turn-Off Time	t_f	C_{LOAD} = 10 nF, 80% to 20%	–	100	–	ns
Pullup On Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GHx} = –300 mA	3	4	6	Ω
		T_J = 150°C, I_{GHx} = –300 mA	5	6.5	8	Ω
Pulldown On Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GLx} = 300 mA	1	1.5	2	Ω
		T_J = 150°C, I_{GLx} = 300 mA	1.5	2	3	Ω
GHx Output Voltage	V_{GHX}	Bootstrap capacitor fully charged	V_{Cx} – 0.2	–	–	V
GLx Output Voltage	V_{GLX}		V_{REG} – 0.2	–	–	V
Turn-Off Propagation Delay[2]	$t_{P(off)}$	Input change to unloaded gate output change	60	90	130	ns
Turn-On Propagation Delay[2]	$t_{P(on)}$	Input change to unloaded gate output change	60	90	130	ns
Propagation Delay Matching, Phase-to-Phase	Δt_{PP}	Measured between corresponding transition points on two sequential phases	–	10	–	ns
Propagation Delay Matching, On-to-Off	Δt_{OO}	Measured across one phase	–	10	–	ns

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ELECTRICAL CHARACTERISTICS (continued) valid at T_J = –40°C to 150°C, V_{DD} = 3 to 5.5 V, V_{BB} = 7 to 50 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Dead Time[2]	t_{DEAD}	RDEAD tied to GND	–	0	–	ns
		R_{DEAD} = 3 kΩ	–	180	–	ns
		R_{DEAD} = 30 kΩ	815	960	1110	ns
		R_{DEAD} = 240 kΩ	–	3.5	–	µs
		RDEAD tied to VDD	–	6	–	µs
Logic Inputs and Outputs						
FF1 and FF2 Fault Output	$V_{FF(L)}$	I_{FF} = 1 mA, fault not present	–	–	0.4	V
FF1 and FF2 Fault Output Leakage Current[3]	$I_{FF(H)}$	V_{FF} = 5 V, fault present	–1	–	1	µA
RDEAD Input Low Voltage	$V_{DEAD(L)}$		–	–	0.2	V
RDEAD Current[3]	I_{DEAD}	RDEAD = GND	–200	–	–70	µA
Input Low Voltage	$V_{IN(L)}$		–	–	0.3 × V_{DD}	V
Input High Voltage	$V_{IN(H)}$		0.7 × V_{DD}	–	–	V
Input Hysteresis	V_{INhys}		300	500	–	mV
Input Current (Except RESET and CCEN)[3]	I_{IN}	0 V < V_{IN} < V_{DD}	–1	–	1	µA
Input Pulldown Resistor (RESET and CCEN)	R_{PD}		–	50	–	kΩ
RESET Pulse Time[4]	t_{RES}		0.1	–	3.5	µs
RESET Delay[4]	t_{DR}		–	–	200	ns
FF2 Clock Input High Voltage	V_{ILC}		–	–	0.3 × V_{DD}	V
FF2 Clock Input Low Voltage	V_{IHC}		0.7 × V_{DD}	–	–	V
FF2 Clock Input Hysteresis	V_{IChys}		300	500	–	mV
FF2 Clock Low to Valid Data Delay[4]	t_{DF}		–	–	100	ns
FF2 Clock Low to Fault Reset Delay[4]	t_{RF}		–	–	100	ns
FF2 Clock High Time[4]	t_{HF}		500	–	–	ns
FF2 Clock Low Time[4]	t_{LF}		500	–	–	ns
Current Sense Differential Amplifier						
Differential Input Voltage	V_{ID}	V_{ID} = CSP – CSN, –1.3 V < V_{CM} < 4 V	$–V_{DD}$	–	V_{DD}	mV
Input Bias Current[3]	I_{BIAS}	CSP = CSN = 0 V	–100	0	100	nA
Input Offset Current[3]	I_{OS}	CSP = CSN = 0 V	–100	0	100	nA
Input Offset Voltage	V_{IOS}	CSP = CSN = 0 V	–10	–	+10	mV
Input Offset Voltage Drift	ΔV_{IOS}	CSP = CSN = 0 V	–	10	–	µV/°C
Input Common Mode Range	CMR	CSP = CSN	–1.5	–	4	V
Open Loop Gain	A_{Vopn}	40 mV< V_{ID} < 175 mV, V_{CM} in range	100	–	–	dB
Closed Loop Gain	A_{Vclos}	40 mV< V_{ID} < 175 mV, V_{CM} in range	5	–	–	V/V

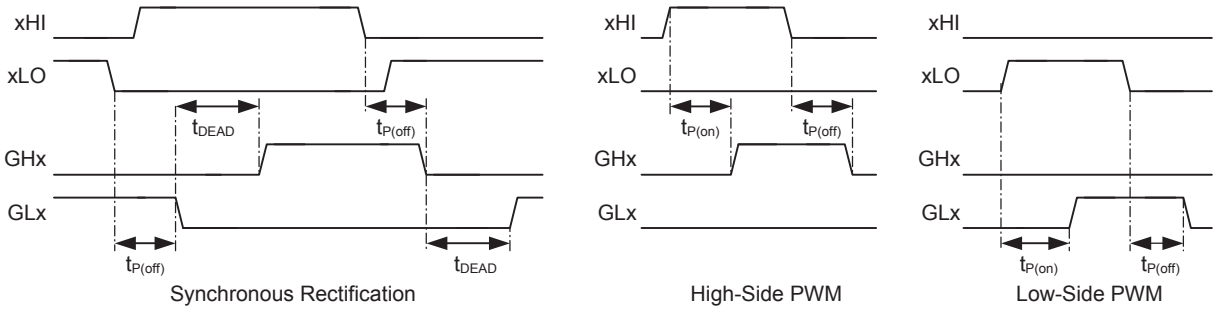
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ELECTRICAL CHARACTERISTICS (continued) valid at T_J = –40°C to 150°C, V_{DD} = 3 to 5.5 V, V_{BB} = 7 to 50 V, unless noted otherwise

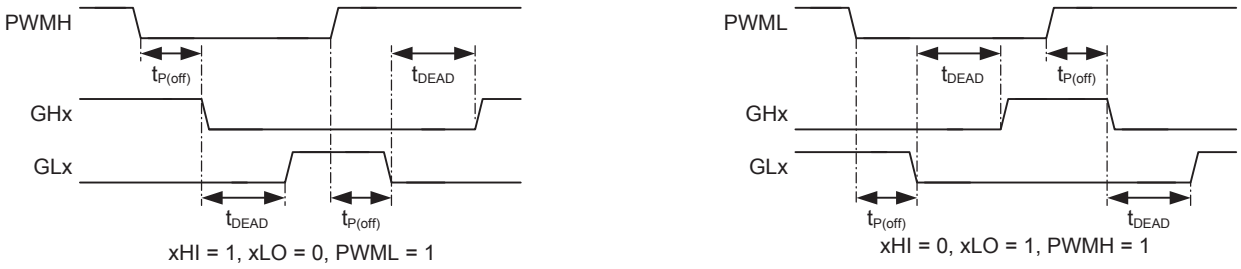
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Small Signal –3 dB Frequency Bandwidth	BW_G	V_{ID} = 10 mV_{pp}, G = 5 V/V	–	1.6	–	MHz
Settling Time	t_{SETTLE}	To within 10% of steady state, V_{CSOUT} = 1 Vpp square wave	–	400	–	ns
Output Dynamic Range	V_{CSOUT}	–100 µA < I_{CSOUT} < 100 µA	0.1	–	V_{DD} – 0.3	V
Output Current Sink	I_{CSsink}	V_{ID} = –400 mV, V_{CSOUT} = 1.5 V	1	–	–	mA
Output Current Source	$I_{CSsource}$	V_{ID} = 400 mV, V_{CSOUT} = 1.5 V	–	–	–1	mA
VREG Supply Ripple Rejection	PSRR	CSP = CSN = AGND, 0 to 300 kHz	–	45	–	dB
DC Common Mode Rejection	CMRR	CSP = CSN = 0 to 200 mV step	–	38	–	dB
AC Common Mode Rejection	CMRR	V_{CM} = 200 mVpp, 0 to 1 MHz	–	28	–	dB
Common Mode Recovery Time	t_{CMrec}	To within 100 mV of steady state, V_{CM} = +4 V step within CMR	–	1	–	µs
Output Slew Rate	SR	10% to 90%, V_{ID} = 0 to 175 mV step	–	20	–	V/µs
Input Overload Recovery	t_{IDrec}	To within 10% of steady state, V_{ID} = 250 mV to 0 V step	–	500	–	ns
Protection						
VREG Undervoltage Lockout Threshold	$V_{REGUVon}$	V_{REG} rising	7.5	8	8.5	V
	$V_{REGUVoff}$	V_{REG} falling	6.75	7.25	7.75	V
Bootstrap Undervoltage Threshold	V_{BOOTUV}	Cx with respect to Sx	59	–	69	$\%V_{REG}$
Bootstrap Undervoltage Hysteresis	$V_{BOOTUVhys}$		–	13	–	$\%V_{REG}$
VDD Undervoltage Turn-Off Threshold	V_{DDUV}	V_{DD} falling	2.45	2.7	2.85	V
VDD Undervoltage Hysteresis	$V_{DDUVhys}$		50	100	150	mV
VDSTH Input Range	V_{DSTH}		0.1	–	2	V
VDSTH Input Current	I_{DSTH}	0 V < V_{DSTH} < 2 V	–	10	30	µA
VDRAIN Input Voltage	V_{DRAIN}		7	V_{BB}	50	V
VDRAIN Input Current	I_{DRAIN}	V_{DSTH} = 2 V, V_{BB} = 12 V, 0 V < V_{DRAIN} < V_{BB}	–	–	250	µA
Short-to-Ground Threshold Offset[5]	V_{STGO}	High-side on, V_{DSTH} ≥ 1 V	–	±100	–	mV
		High-side on, V_{DSTH} < 1 V	–150	±50	150	mV
Short-to-Battery Threshold Offset[6]	V_{STBO}	Low-side on, V_{DSTH} ≥ 1 V	–	±100	–	mV
		Low-side on, V_{DSTH} < 1 V	–150	±50	150	mV
Overtemperature Fault Flag Threshold	T_{JF}	Temperature increasing	150	170	–	ºC
Overtemperature Fault Hysteresis	T_{JFhys}	Recovery = T_{JF} – T_{JFhys}	–	15	–	ºC

[1]Functions correctly, but parameters are not guaranteed, below the general limits (7 V).
[2]See Gate Drive Timing diagrams.
[3]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[4]See Fault Output Timing diagram.
[5]As V_{Sx} decreases, fault occurs if $V_{BAT} - V_{Sx} > V_{STG}$. STG threshold, $V_{STG} = V_{DSTH} + V_{STGO}$.
[6]As V_{Sx} increases, fault occurs if $V_{Sx} - V_{LSS} > V_{STB}$. STB threshold, $V_{STB} = V_{DSTH} + V_{STBO}$.

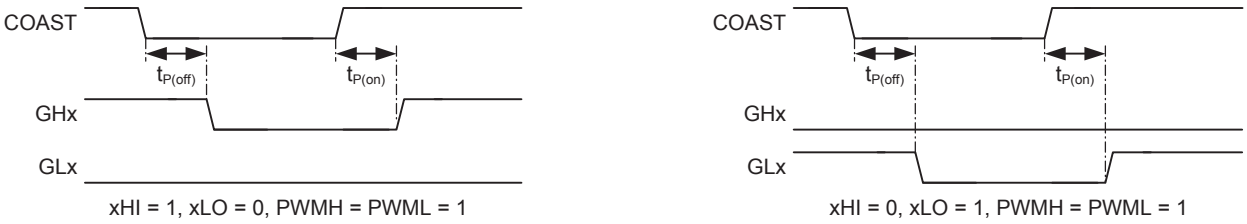
Timing Diagrams



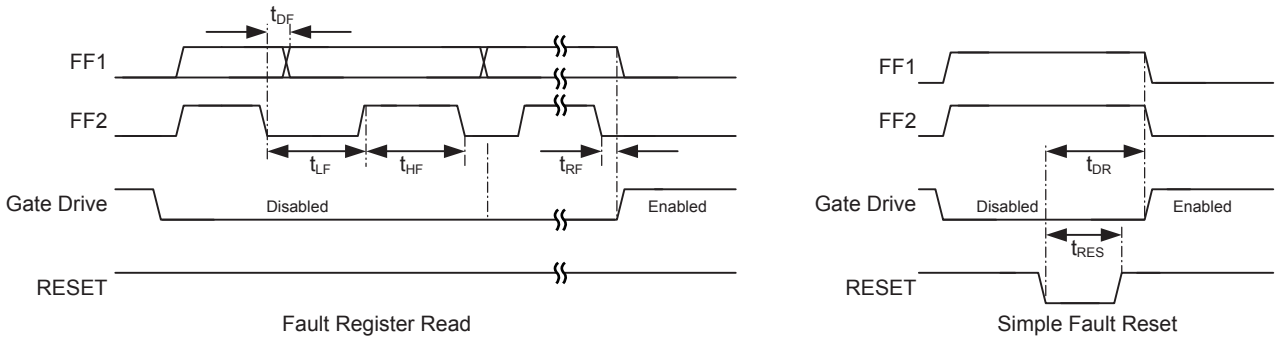
(A) Gate Drive Timing, Phase Control Inputs



(B) Gate Drive Timing, PWM Inputs



(C) Gate Drive Timing, COAST Inputs



(D) Fault Output Timing

Functional Description

The A4933 is a three-phase MOSFET driver (pre-driver) with separate supplies for the logic, and for the analog and drive sections. This permits operation with a regulated logic supply from 3 to 5.5 V and with an unregulated main supply of 7 to 50 V.

The six high current gate drives are capable of driving a wide range of N-channel power MOSFETs, and are configured as three high-side drives and three low-side drives. Each drive can be controlled with a logic level input compatible with 3.3 or 5 V logic. The A4933 provides all the necessary circuits to ensure that the gate-source voltage of both high-side and low-side external FETs are above 10 V, at supply voltages down to 7 V. For extreme battery voltage drop conditions, correct functional operation is guaranteed at supply voltages down to 5.5 V, but with a reduced gate drive voltage.

The control inputs to the A4933 provide a very flexible solution for many motor control applications. For full sinusoidal excitation, each phase can be driven with an independent PWM signal. For less complex drive solutions, the two PWM inputs, PWML and PWMH, allow simple high-side, low-side, or fast-decay control with a single PWM signal.

A current sense amplifier allows motor current to be sensed by a low-value sense resistor in the ground connection to the power bridge.

The A4933 includes a number of protection features against undervoltage, overtemperature, and power bridge faults. Fault states enable responses by the device or by the external controller, depending on the fault condition and logic settings. Two fault flag outputs, FF1 and FF2, are provided to signal detected faults to an external controller. Diagnostics include an internal fault register, which can be accessed by serial read out using the fault flag pins.

Power Supplies

Two power supply voltages are required, one for the logic interface and one for the analog and output drive sections. Both supplies should be decoupled with ceramic capacitors connected close to the supply and ground pins.

The logic supply, connected to VDD, allows the flexibility of a 3.3 or 5 V logic interface. The main power supply should be connected to VBB through a reverse voltage protection circuit. The A4933 operates within specified parameters with a VBB supply from 7 to 50 V and functions correctly with a supply down to 5.5 V. This provides a very rugged solution for use in the harsh automotive environment.

Gate Drives

The A4933 is designed to drive external, low on-resistance, power N-channel MOSFETs. It supplies the large transient currents necessary to quickly charge and discharge the external FET gate capacitance in order to reduce dissipation in the external FET during switching. The charge and discharge rate can be controlled using an external resistor in series with the connection to the gate of the FET.

Gate Drive Voltage Regulation The gate drives are powered by an internal regulator which limits the supply to the drives and therefore the maximum gate voltage. When the V_{BB} supply greater than about 16 V, the regulator is a simple linear regulator. Below 16 V, the regulated supply is maintained by a charge pump boost converter, which requires a pump capacitor connected between the CP1 and CP2 pins. This capacitor must have a minimum value of 470 nF, and is typically 680 nF.

The regulated voltage, nominally 13 V, is available on the VREG pin. A sufficiently large storage capacitor must be connected to this pin to provide the transient charging current to the low-side drives and the bootstrap capacitors.

Top-off Charge Pump An additional top-off charge pump is provided for each phase. The charge pumps allow the high-side drives to maintain the gate voltage on the external FETs indefinitely, ensuring so-called 100% PWM if required. This is a low current trickle charge pump, and is operated only after a high-side FET has been signaled to turn on. The floating high-side gate drive requires a small bias current (<20 µA) to maintain the high-level output. Without the top-off charge pump, this bias current would be drawn from the bootstrap capacitor through the Cx pin. The charge pump provides sufficient current to ensure that the bootstrap voltage and thereby the gate-source voltage is maintained at the necessary level.

Note that the charge required for initial turn-on of the high-side gate is always supplied by the bootstrap capacitor. If the bootstrap capacitor becomes discharged, the top-off charge pump will not provide sufficient current to allow the FET to turn on.

In some applications a safety resistor is added between the gate and source of each FET in the bridge. When a high-side FET is held in the on-state, the current through the associated high-side gate-source resistor (R_{GSH}) is provided by the high-side drive and therefore appears as a static resistive load on the top-off charge pump. The minimum value of R_{GSH} for which the top-off charge pump can provide current is shown in the Electrical Characteristics table.

GLA, GLB, and GLC Pins These are the low-side gate drive outputs for the external N-channel MOSFETs. External resistors between the gate drive output and the gate connection to the FET (as close as possible to the FET) can be used to control the slew rate seen at the gate, thereby providing some control of the di/dt and dv/dt of the SA, SB, and SC outputs. GLx going high turns on the upper half of the drive, sourcing current to the gate of the low-side FET in the external power bridge, turning it on. GLx going low turns on the lower half of the drive, sinking current from the external FET gate circuit to the LSS pin, turning off the FET.

SA, SB, and SC Pins Directly connected to the motor, these terminals sense the voltages switched across the load. These terminals are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drives. The discharge current from the high-side FET gate capacitance flows through these connections, which should have low impedance circuit connections to the FET bridge.

GHA, GHB, and GHC Pins These terminals are the high-side gate drive outputs for the external N-channel FETs. External resistors between the gate drive output and the gate connection to the FET (as close as possible to the FET) can be used to control the slew rate seen at the gate, thereby controlling the di/dt and dv/dt of the SA, SB, and SC outputs. GHx going high turns on the upper half of the drive, sourcing current to the gate of the high-side FET in the external motor-driving bridge, turning it on. GHx going low turns on the lower half of the drive, sinking current from the external FET gate circuit to the corresponding Sx pin, turning off the FET.

CA, CB, and CC Pins These are the high-side connections for the bootstrap capacitors and are the positive supply for the high-side gate drives. The bootstrap capacitors are charged to approximately V_{REG} when the associated output Sx terminal is low. When the Sx output swings high, the charge on the bootstrap capacitor causes the voltage at the corresponding Cx terminal to rise with the output to provide the boosted gate voltage needed for the high-side FETs.

LSS Pin This is the low-side return path for discharge of the capacitance on the FET gates. It should be tied directly to the common sources of the low-side external FETs through an independent low impedance connection.

RDEAD Pin This pin controls internal generation of dead time during FET switching.

- When a resistor greater than 3 kΩ is connected between RDEAD and AGND, cross-conduction is prevented by the gate drive circuits, which introduce a dead time, t_{DEAD}, between switching one FET off and the complementary FET on. The dead time is derived from the resistor value connected between the RDEAD and AGND pins.
- When RDEAD is connected directly to VDD, cross-conduction is prevented by the gate drive circuits. In this case, t_{DEAD} defaults to a value of 6 µs typical.
- When RDEAD is connected directly to AGND, internal dead time generation is disabled. This allows dead times of any duration to be determined by the external controller through the relative timing of the phase logic control inputs, xHI and xLO. Note that when using an external controller to determine the dead time, care must be taken to ensure that unintentional shorts across the supply are avoided.

Logic Control Inputs

Low voltage-level digital inputs provide control for the gate drives. The input logic is shown in table 1.

These logic inputs can be driven from either 3.3 or 5 V logic. All have a nominal hysteresis of 500 mV to improve noise performance.

AHI, BHI, CHI, ALO, BLO, and CLO Pins These are the phase control inputs. The xHI inputs control the high-side drives and the xLO inputs control the low-side drives. Internal lockout logic ensures that the high-side output drive and low-side output drive cannot be active simultaneously, except when RDEAD is connected to AGND and at the same time CCEN is set high, as described in the CCEN pin section.

PWMH and PWML Pins These inputs can be used to externally control motor torque and speed.

- Setting PWMH low turns off active high-side drives and turns on the complementary low-side drives. This provides high-side–chopped slow-decay PWM with synchronous rectification.

- Setting PWML low turns off active low-side drives and turns on the complementary high-side drives. This provides low-side–chopped slow-decay PWM with synchronous rectification.
- PWMH and PWML may also be connected together and driven with a single PWM signal. This provides fast-decay PWM with synchronous rectification.

COAST Pin An active-low input, which forces low all gate drive outputs, GHx and GLx, and turns off all external FETs. This can be used to protect the FETs and the motor in the case of a short circuit. Using COAST does not clear any faults, so the fault flags can still be decoded and the fault register data word can be read. Because COAST turns off all the external FETs, it can also be used to provide fast-decay PWM without synchronous rectification.

RESET Pin This is an active-low input, and when active it allows the A4933 to enter sleep mode. When RESET is held low for longer than the reset pulse time, t_{RES}, the regulator and all internal circuitry are disabled and the A4933 enters sleep mode. During sleep mode, current consumption from the VBB and VDD supplies is reduced to a minimal level. In addition, latched faults and the corresponding fault flags are cleared. When the A4933 is coming out of sleep mode, the protection logic ensures that the gate drive outputs are off until the charge pump reaches its correct operating condition. The charge pump stabilizes in approximately 3 ms under nominal conditions.

RESET can be used also to clear latched fault flags without entering sleep mode. To do so, hold RESET low for less then the reset pulse time, t_{RES}. This clears any latched fault that disables the outputs, such as short circuit detection or bootstrap capacitor undervoltage, and also clears the fault register.

Note that the A4933 can be configured to start without any external logic input. To do so, pull up the RESET pin to V_{BB} by means of an external resistor. The resistor value should be between 20 and 33 kΩ.

CCEN Pin This input provides an override to allow both the high-side and the low-side external FETs of any phase to be active at the same time, enabling cross-conduction. As an extra level of safety, cross-conduction can only occur when RDEAD is tied to AGND and CCEN is set high. If the CCEN input is inadvertently disconnected from the controller, an internal pull-down resistor ensures that the outputs revert to a safe condition.

ESF Pin This is the Enable Stop on Fault input. It determines the action that is taken when certain faults are detected. See the Fault Protection and Diagnostics section for details.

Table 1. Phase Control Truth Table

Inputs								Outputs			Comment
RDEAD	RESET	CCEN	COAST	PWMH	PWML	xHI	xLO	GHx	GLx	Sx	
x	1	x	x	x	x	0	0	L	L	Z	Phase disabled
x	1	x	1	1	1	0	1	L	H	LS	Phase sinking
x	1	x	1	1	1	1	0	H	L	HS	Phase sourcing
>0.2 V	1	x	x	x	x	1	1	L	L	Z	Phase disabled
x	1	x	1	0	1	0	1	L	H	LS	Sink; high-side PWM on other phases
x	1	x	1	0	1	1	0	L	H	LS	Slow decay, SR; low-side recirculation
x	1	x	1	1	0	0	1	H	L	HS	Slow decay, SR; high-side recirculation
x	1	x	1	1	0	1	0	H	L	HS	Source; low-side PWM on other phases
x	1	x	1	0	0	0	1	H	L	HS	Fast decay, SR
x	1	x	1	0	0	1	0	L	H	LS	Fast decay, SR
AGND	1	x	1	1	0	1	1	H	L	HS	Slow decay, SR; high-side recirculation
AGND	1	x	1	0	1	1	1	L	H	LS	Slow decay, SR; low-side recirculation
x	0	x	x	x	x	x	x	Z	Z	Z	Low power shutdown
x	1	x	0	x	x	x	x	L	L	Z	Coast
AGND	1	0	1	1	1	1	1	L	L	Z	Phase disabled
AGND	1	1	1	1	1	1	1	H	H	U	Cross-conduction

x = don't care, HS = high-side FET active, LS = low-side FET active, Z = high impedance, both FETs off, U = undefined, SR = synchronous rectification

Current Sense Amplifier

An uncommitted differential sense amplifier is provided to allow the use of either low value sense resistors or a current shunt as the current sensing element. The input common mode range, CMR, allows the below-ground current sensing typically required in PWM motor control during switching transients.

Input is on the CSN and CSP pins. The output of the sense amplifier is available at CSOUT and can be used in a peak current control system.

The gain of the sense amplifier is set using external input and feedback resistors. The gain must be set to be greater than the specified minimum to ensure stability. Typically the gain will be set between 5 and 50 V/V. Output offset can also be added using external resistors. Examples of setting the sense amplifier gain and offset are provided in the Applications Information section.

Diagnostics

Several diagnostic features are integrated into the A4933 to provide indication of fault conditions and, if required, take action to prevent permanent damage. In addition to system wide faults such as undervoltage and overtemperature, the A4933 integrates individual drain-source monitors for each external FET, to provide short circuit detection. When a short or undervoltage fault is being reported, detailed fault information can be read from the fault outputs as a serial data word.

Diagnostic Management Pins

ESF Pin This pin (Enable Stop on Fault) determines the action taken when a short circuit or overtemperature fault is detected. It does not affect undervoltage fault condition actions.

When ESF is set to logic high, any short circuit or overtemperature fault condition will pull all the gate drive outputs low and coast the motor. For short faults, this disabled state will be latched until RESET goes low or a serial read is completed.

When ESF is set to logic low, under most conditions the A4933 will not disrupt normal operation and therefore will not protect the drive circuit or motor from damage. This is the case even though the fault flags are set. This allows the actions taken to be controlled externally by the system control circuits. To prevent damage to components, the external controller can take low the COAST input or all of the xHi and xLO phase control inputs.

VDSTH Pin Faults on the external FETs are determined by measuring the drain-source voltage, V_{DS}, of each active FET and comparing it to the threshold voltage applied to the VDSTH input, V_{DSTH}. To avoid false fault detection during switching transients, the comparison is delayed by an internal blanking timer.

VDRAIN This is a low-current sense input from the top of the external FET bridge. This input allows accurate measurement of the voltage at the drain of the high-side FETs. It should be connected directly to the common connection point for the drains of the power bridge FETs at the positive supply connection point. The input current to the VDRAIN pin is proportional to the voltage on the VDSTH pin and can be approximated by:

$$I_{VDRAIN} = 72 \times V_{DSTH} + 52 \ ,$$

where I_{VDRAIN} is the current into the VDRAIN pin, in µA, and V_{DSTH} is the voltage on the VDSTH pin, in V.

FF1 and FF2 Pins are open drain output fault flags, which indicate fault conditions by their state, as shown in table 2. In the event that two or more faults are detected simultaneously, the state of the fault flags will be determined by a logical OR of the flag states for all detected faults.

Table 2. Fault Definitions

Flag State		Fault Description	Disable Outputs*		Flag Latched
FF1	FF2		ESF Low	ESF High	
0	0	No fault	No	No	–
0	1	Short-to-ground	No	Yes	If ESF high
0	1	Short-to-supply	No	Yes	If ESF high
0	1	Shorted load	No	Yes	If ESF high
1	0	Overtemperature	No	Yes	No
1	1	VDD undervoltage	Yes	Yes	No
1	1	VREG undervoltage	Yes	Yes	No
1	1	Bootstrap undervoltage	Yes	Yes	Yes

**Yes* indicates all gate drives low, and all FETs off.

When ESF is high, short faults will always cause the fault flags to be latched. When ESF is low, a short fault will only be flagged when the fault is present, and the flag state will not be latched. This provides additional diagnostics flexibility during FET

switching. Any short faults detected will always be latched in the fault register.

When a short or undervoltage fault is present, a clock can be applied to FF2 and detailed fault information can be read from FF1 as a serial word. This can be used to determine on which of the six external FETs a short is being detected, or which of the monitored voltages have gone below their undervoltage threshold level. Fault register serial access operation is detailed in the Fault Register Serial Access section.

Fault States

Overtemperature If the junction temperature exceeds the overtemperature threshold, typically 165°C, the A4933 will enter the overtemperature fault state and FF1 will go high. The overtemperature fault state, and FF1, will only be cleared when the temperature drops below the recovery level defined by $T_{JF} - T_{JFhys}$. Note that an overtemperature fault does not permit access to the fault register because FF2 is pulled low.

If ESF is set high when an overtemperature is detected, the outputs will be disabled automatically while the fault state is present. If ESF is set low, then no circuitry will be disabled. In this case external control circuits must take action to limit the power dissipation in some way so as to prevent overtemperature damage to the chip and unpredictable device operation.

VREG Undervoltage VREG supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the voltages are sufficiently high before enabling any of the outputs. If the voltage at VREG, V_{REG}, drops below the falling VREG undervoltage lockout threshold, $V_{REGUVoff}$, then the A4933 will enter the VREG undervoltage fault state. In this fault state, both FF1 and FF2 will be high, and the outputs will be disabled. The VREG undervoltage fault state and the fault flags will be cleared when V_{REG} rises above the rising VREG undervoltage lockout threshold, $V_{REGUVon}$.

The VREG undervoltage monitor circuit is active during power-up, and the A4933 remains in the VREG undervoltage fault state until V_{REG} is greater than the rising VREG undervoltage lockout threshold, $V_{REGUVon}$.

Any time the A4933 enters the VREG undervoltage fault state, bit 7 in the fault register will be set and will remain set until cleared by a register reset (see the Fault Register Serial Access section).

Bootstrap Capacitor Undervoltage The A4933 monitors the voltage across the individual bootstrap capacitors to ensure they have sufficient charge to supply the current pulse for the high-side drive. Before a high-side drive can be turned on, the voltage across the associated bootstrap capacitor must be higher than the turn-on voltage limit. If this is not the case, then the A4933 will start a bootstrap charge cycle by activating the complementary low-side drive. Under normal circumstances, this will charge the bootstrap capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled.

The bootstrap voltage monitor remains active while the high-side drive is active and if the voltage drops below the turn-off voltage a charge cycle is initiated.

In either case, if there is a fault that prevents the bootstrap capacitor charging, then the charge cycle will timeout, the fault flags (indicating an undervoltage) will be set, and the outputs will be disabled. In addition, the appropriate bit in the fault register will be set. This allows the specific phase giving the bootstrap undervoltage to be determined by reading the serial data word.

The bootstrap undervoltage fault state remains latched until RESET is set low or a serial read of the fault register is completed.

VDD Undervoltage The logic supply voltage at VDD is monitored to ensure correct logical operation. If an undervoltage on VDD is detected, the outputs will be disabled. In addition, because the state of other reported faults cannot be guaranteed, all fault states, fault flags, and the fault register are reset and replaced by the fault flags corresponding to a VDD undervoltage fault state. For example, a VDD undervoltage will reset an existing short circuit fault condition and replace it with a VDD undervoltage fault. When the VDD undervoltage condition is removed, all flags will be cleared and the outputs enabled.

Short Fault Operation Shorts in the power bridge are determined by monitoring the drain-souce voltage, V_{DS}, of each active FET and comparing it to the fault threshold voltage at the VDSTH pin. Because power MOSFETs take a finite time to reach the rated on-resistance, the measured drain-source voltages will show a fault as the phase switches. To avoid such false short fault detections,

the output from the comparators are ignored under two conditions:

- while the external FET is off, and
- until the end of the period, referred to as the *fault blank time*, after the FET is turned on.

When the FET is turned on, if the drain-source voltage exceeds the voltage at the VDSTH pin at any time after the fault blank time, then a short fault will be detected. If also ESF is set high, then this fault will be latched and the FET disabled until reset.

In some applications, the fault blank time may be insufficient to avoid detecting false faults during the switching time of the external FET. In these cases, the external controller driving the A4933 may be used to determine the correct fault condition by setting ESF low. This will prevent latching of the fault flag when a short fault is detected, and will not disable the FET. With ESF low, FF2 will remain high only while the measured V_{DS} exceeds the fault threshold. The external controller can then monitor the fault flags and use its own timers to validate a fault condition.

Note that any fault thus detected by the A4933 will still be latched in the fault register and remain there until cleared.

When ESF is set low, the external FETs are not disabled by the A4933 when a short fault is detected. To avoid permanent damage to the external FETs or to the motor under this condition, the A4933 can either be fully disabled by the RESET input or all FETs can be switched off by pulling low the COAST input or all the phase control inputs.

Short to Supply A short from any of the motor phase connections to the battery or VBB connection is detected by monitoring the voltage across the low-side FETs in each phase, using the appropriate Sx pin and the LSS pin. This drain-source voltage, V_{DS}, is continuously compared to the voltage on the VDSTH pin. The result of this comparison is ignored if the FET is not active. It is ignored also for one fault blank time interval after the FET is turned on. If, when the comparator is not being ignored, its output indicates that V_{DS} exceeds the voltage at the VDSTH pin, then FF2 will be high. If also ESF is set high, then FF2 will be latched high and the outputs will be disabled. Alternatively, if also ESF is set low, then the outputs will not be disabled and FF2 will only be high while the output of the comparator indicates that V_{DS} exceeds the voltage at the VDSTH pin.

Short to Ground A short from any of the motor phase connections to ground is detected by monitoring the voltage across the high-side FETs in each phase, using the appropriate Sx pin and the voltage at VDRAIN. This drain-source voltage, V_{DS}, is continuously compared to the voltage on the VDSTH pin. The result of this comparison is ignored if the FET is not active. It is ignored also for one fault blank time interval after the FET is turned on. If, when the comparator is not being ignored, its output indicates that V_{DS} exceeds the voltage at the VDSTH pin, FF2 will be high. If also ESF is set high, FF2 will be latched high and the outputs will be disabled. Alternatively, if also ESF is set low, the outputs will not be disabled and FF2 will only be high while the output of the comparator indicates that V_{DS} exceeds the voltage at the VDSTH pin.

Shorted Load The short-to-ground and short-to-supply monitor circuits will also detect a short across a motor phase winding. In most cases, a shorted winding will be indicated by a high-side and low-side fault being detected at the same time. In some cases the relative impedances may permit only one of the shorts to be detected.

Differentiating Short Fault Conditions

The distinction between short-to-ground, short-to-supply, and shorted load can only be made by examining the contents of the fault register. It is not possible to determine where a short fault has occurred when using the state of the fault flags, FF1 and FF2, alone. The flag combination FF1 low and FF2 high simply indicates the presence of a probable short circuit.

As described above, shorts are detected by monitoring the drain-source voltage, V_{DS}, of each of the six FETs in the power bridge. The different short fault conditions are defined as follows:

- A short-to-ground is likely to be present if the V_{DS} of any active high-side FET is greater than the threshold defined by VDSTH (fault bits AH, BH, or CH = 1)
- A short-to-supply is likely to be present if the V_{DS} of any active low-side FET is greater than the threshold defined by VDSTH (fault bits AL, BL, or CL = 1)
- A shorted load or phase is likely to be present if, at the same time, the V_{DS} of an active high-side and an active low-side are both greater than the threshold defined by VDSTH.

Fault Register

All undervoltage and short faults are recorded in a 10-bit fault register as defined in table 3. The fault register accumulates all detected faults until cleared by setting RESET low, by cycling the power off and on, or by reading the contents. The contents will also be cleared if a VDD undervoltage fault is detected. During a VDD undervoltage fault condition, both fault flags will be high but all the bits in the fault register will be reset.

Table 3. Fault Register Bit Definitions

Bit	Position	Function
AH	First	V_{DS} exceeded on A phase high-side FET
BH	2	V_{DS} exceeded on B phase high-side FET
CH	3	V_{DS} exceeded on C phase high-side FET
AL	4	V_{DS} exceeded on A phase low-side FET
BL	5	V_{DS} exceeded on B phase low-side FET
CL	6	V_{DS} exceeded on C phase low-side FET
VR	7	Undervoltage detected on VREG
VA	8	Bootstrap undervoltage detected on phase A
VB	9	Bootstrap undervoltage detected on phase B
VC	Last	Bootstrap undervoltage detected on phase C

The contents of the fault register can be read serially from the FF1 pin by applying a clock signal to the FF2 pin during an undervoltage or short fault state.

The fault flag pins, FF1 and FF2, are open drain outputs and passively pulled high when a fault is present. This makes it possible to drive one or both of these fault pins from an external source during a fault condition, when the A4933 is not pulling the pin low. FF2 can thus be used as a clock input to shift out the fault status register, bit-by-bit, on the other fault flag, FF1.

When FF2 is being pulled low by the A4933, either when no fault is present or when an overtemperature fault is present, then no serial access is possible. The fault status register can be accessed only when FF2 goes high. This occurs when either a short or an undervoltage fault has been detected.

Faut Register Serial Access

To access the fault register, FF1 and FF2 must be monitored by an external controller. If FF2 goes high and FF1 remains low, then a short has been detected. If FF1 and FF2 go high together, then an under voltage has been detected. In either case, the sequence for reading the contents of the fault register is:

1. The external controller takes any necessary additional action to protect the FETs.
2. The external controller pulls FF2 low.
3. The A4933 outputs on FF1 the fault register first bit, AH.
4. The external controller reads the fault bit, and then cycles FF2 high then low for the next bit, BH.
5. Steps 3 and 4 alternate until all of the 10 bits in the fault register have been read out.
6. After the final bit, VC, is output, the external controller cycles FF2 high then low.
7. The A4933 resets the fault register and pulls FF1 and FF2 low to indicate no fault present.
8. The external controller releases FF2.

The basic sequence for the three possible states of FF1 and FF2 are shown in figure 1.

At the end of the serial transfer, on the last high-to-low transition input to FF2, the fault register and the fault flags are reset. However, it is possible that one of the three unlatched fault conditions, VREG undervoltage, VDD undervoltage, or overtemperature, is still present. In this case the fault flags will immediately show the fault status.

Resetting the VR Bit

At power-up, on coming out of reset, or after a VDD or VREG undervoltage fault, it is possible that the fault flags and fault register will have cleared but the VR bit in the fault register remains set. This would happen if, when a power-on-reset occurred, V_{REG} had not yet risen beyond the undervoltage threshold level, $V_{REGUVon}$. Although VREG undervoltage fault state is not latched and the fault flags are cleared when the fault is removed, the VR bit in the fault register is latched and may remain set after the power-on-reset. For this reason it is recommended, when the serial fault register is to be used, to perform a reset by taking the RESET pin low for less than the reset pulse time, t_{RES}, after the A4933 is powered-up and all fault flags are clear (FF1 and FF2 are low).

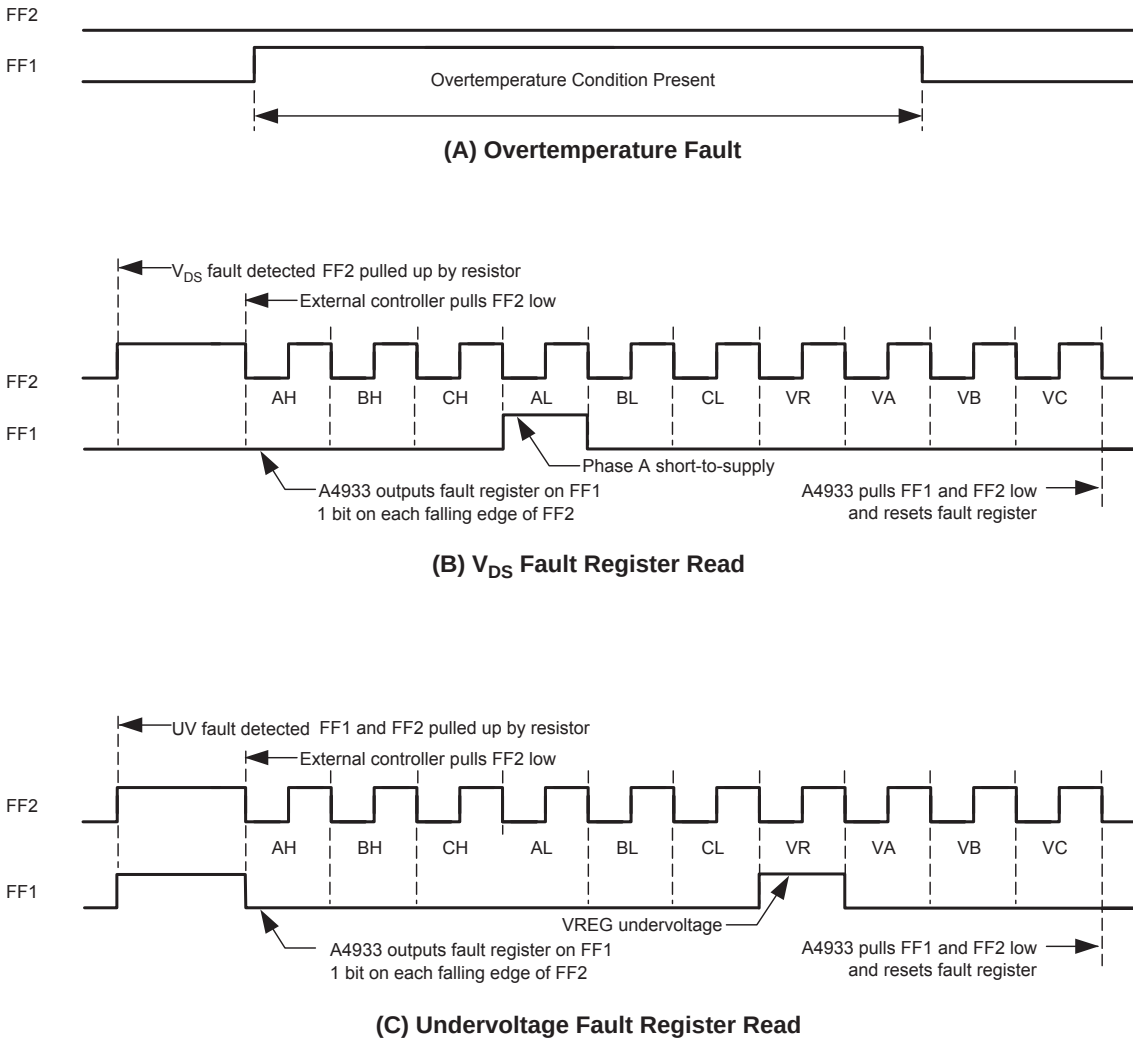


Figure 1. Fault flag sequence diagrams

Applications Information

Power Bridge Management Using PWM Control

The A4933 provides individual high-side and low-side controls for each phase, plus two PWM control signals and a coast control. This allows a wide variety of 3-phase bridge control schemes to be implemented.

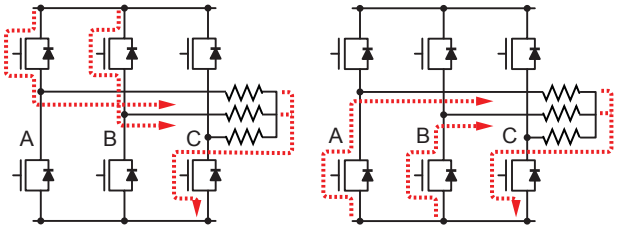
For advanced schemes using sinusoidal current control, each FET in the 3-phase bridge can be controlled individually without using the PWM and COAST inputs. This requires a higher performance external controller, with a PWM output for each phase. If full external control over dead time is required, then six PWM outputs will be required, one for each FET in the bridge. In this type of system, the external controller has full control over the current-decay method, load current recirculation paths, braking, and coasting.

Figure 2A shows an example of the paths of the bridge and load currents when each phase is controlled directly. The PWM inputs PWMH and PWML are both tied high and COAST is tied low. In this case the high-side FETs are switched off during the current decay time (PWM off-time) and load current recirculates through the low-side FETs. This is commonly referred to as high-side chopping or high-side PWM. During the PWM off-time, the complementary FETs are turned on, to short the body diode and provide synchronous rectification.

Figure 2A shows one combination of phase states, and the same principal applies to any of the possible phase states. This principal also applies when the low-side FETs are turned off during the PWM off-time and the load current recirculates through the high side FETs, as shown in figure 2B.

For less complex control schemes, for example where simple block commutation is used, it is possible to control the bridge with three logic signals (one for each phase) and a single PWM signal. Figure 2C shows an example of 2-phase excitation with high-side PWM, as commonly used in a block commutation scheme. The PWMH input is used to modulate the phase currents and PWML is held high. During the PWM off-time, the active high-side FET is turned off and the complementary low-side FET is turned on. Note that the phase control signals in this case do not change and all PWM switching, for any phase combination, is managed by a single PWM signal. For low-side PWM, PWMH is held high and the PWM signal is applied to PWML.

By tying PWMH and PWML together and applying a PWM signal to them, the load current can be controlled using fast decay by effectively reversing the supply polarity. This feature operates



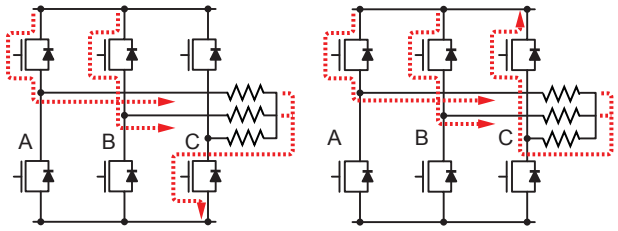
Drive

Phase	A	B	C
xHI	1	1	0
xLO	0	0	1
GHx	H	H	L
GLx	L	L	H

Recirculate

Phase	A	B	C
xHI	0	0	0
xLO	1	1	1
GHx	L	L	L
GLx	H	H	H

(A) Slow decay, synchronous rectification, high-side PWM using phase inputs



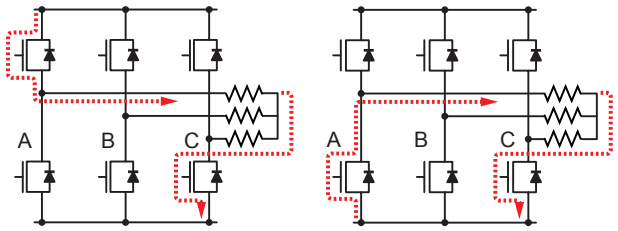
Drive

Phase	A	B	C
xHI	1	1	0
xLO	0	0	1
GHx	H	H	L
GLx	L	L	H

Recirculate

Phase	A	B	C
xHI	1	1	1
xLO	0	0	0
GHx	H	H	H
GLx	L	L	L

(B) Slow decay, synchronous rectification, low-side PWM using phase inputs



Drive

Phase	A	B	C
xHI	1	0	0
xLO	0	0	1
GHx	H	L	L
GLx	L	L	H
PWMH		1	
PWML		1	

Recirculate

Phase	A	B	C
xHI	1	0	0
xLO	0	0	1
GHx	L	L	L
GLx	H	L	H
PWMH		0	
PWML		1	

(C) Slow decay, synchronous rectification, high-side PWM using PWMx inputs

Figure 2. Power bridge current paths

with either 2-phase or 3-phase excitation. When using fast decay, a PWM duty cycle of 50% results in zero effective motor torque. A duty cycle of less than 50% causes negative effective torque, and greater than 50% causes positive effective torque.

To reduce power dissipation in the external FETs, the A4933 can be instructed to turn on the appropriate low-side and high-side drives during the load current recirculation PWM off-cycle. This synchronous rectification allows current to flow through the selected FETs, rather than the source-drain body diode, during the decay time. The body diodes of the recirculating power FETs conduct only during the dead time that occurs at each PWM transition.

Dead Time

To prevent cross-conduction (shoot through) in any phase of the power FET bridge, it is necessary to have a dead time delay, t_{DEAD}, between a high- or low-side turn-off and the next complementary turn-on event. The potential for cross-conduction occurs when any complementary high-side and low-side pair of FETs are switched at the same time; for example, when using synchronous rectification or after a bootstrap capacitor charging cycle. In the A4933, the dead time for all three phases is set by a single dead-time resistor (R_{DEAD}) between the RDEAD and AGND pins.

For R_{DEAD} values between 3 kΩ and 240 kΩ, at 25°C the nominal value of t_{DEAD} in ns can be approximated by:

$$t_{DEAD}(\text{nom}) = 50 + \frac{7200}{1.2 + (200 / R_{DEAD})} \quad , \quad (1)$$

where R_{DEAD} is in kΩ. Greatest accuracy is obtained for values of R_{DEAD} between 6 and 60 kΩ, which are shown in figure 3.

The I_{DEAD} current can be estimated by:

$$I_{DEAD} = \frac{1.2}{R_{DEAD}} \quad . \quad (2)$$

If the dead time is to be generated externally, for example by the PWM output of a microcontroller, then connect the RDEAD pin to the AGND pin to set the internally-generated dead time to zero. Note that this configuration can allow cross-conduction, and appropriate care should be taken, as described in the Cross-Conduction section. The maximum internally-generated dead time, 6 µs typical, can be set by connecting the RDEAD and VDD pins.

The choice of power FET and external series gate resistance determine the selection of the dead-time resistor, R_{DEAD}. The dead time should be long enough to ensure that one FET in a phase has stopped conducting before the complementary FET starts conducting. This should also take into account the tolerance and variation of the FET gate capacitance, the series gate resistance, and the on-resistance of the A4933 internal drives.

Internally-generated dead time will be present only if the on-command for one FET occurs within t_{DEAD} after the off-command for its complementary FET. In the case where one side of a phase drive is permanently off, for example when using diode rectification with slow decay, then the dead time will not occur. In this case the gate drive will turn on within the specified propagation delay after the corresponding phase input goes high. (Refer to the Gate Drive Timing diagrams.)

Fault Blank Time

To avoid false short fault detection, the output from the VDS monitor for any FET is ignored when that FET is off and for a period of time after it is turned on. This period of time is the fault blank time. Its length is the dead time, t_{DEAD}, plus an additional period of time that compensates for the delay in the V_{DS} monitors. This additional delay is typically 300 to 600 ns. When t_{DEAD}

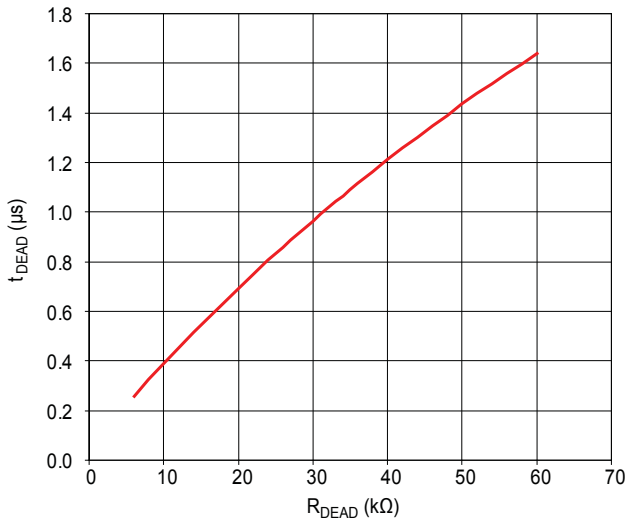


Figure 3. Dead time versus R_{DEAD}

is set to zero by connecting RDEAD to AGND, the fault blank time typically defaults to 2 µs.

Cross-Conduction

In some circumstances it is desirable to allow activation of both high-side and low-side FETs in a single phase of the power bridge. This can be used, with care, to reduce diode conduction during synchronous rectification, which improves overall efficiency and reduces electromagnetic emissions.

This mode of operation is also useful for independently controlling each phase of a VR motor or to turn on all high-side and low-side FETs together, to cause a supply short circuit for blowing a safety fuse.

Cross-conduction can occur only when the internally-generated dead time is set to zero by connecting RDEAD to AGND and, at the same time, CCEN is high. If zero internally-generated dead time is required, but cross-conduction is to be prevented, then CCEN can be tied to AGND. When the dead time is set to zero it is still possible for some overlap to be present at the switching instants due to the relative switching time of the FETs.

Bootstrap Capacitor Selection

The bootstrap capacitors, C_{BOOTx}, must be correctly selected to ensure proper operation of the A4933. If the capacitances are too high, time will be wasted charging the capacitor, resulting in a limit on the maximum duty cycle and the PWM frequency. If the capacitances are too low, there can be a large voltage drop at the time the charge is transferred from C_{BOOTx} to the FET gate, due to charge sharing.

To keep this voltage drop small, the charge in the bootstrap capacitor, Q_{BOOT}, should be much larger than the charge required by the gate of the FET, Q_{GATE}. A factor of 20 is a reasonable value, and the following formula can be used to calculate the value for C_{BOOT}:

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20 \quad ,$$

therefore:

$$C_{BOOT} = \frac{Q_{GATE} \times 20}{V_{BOOT}} \quad , \qquad (3)$$

where V_{BOOT} is the voltage across the bootstrap capacitor.

The voltage drop across the bootstrap capacitor as the FET is being turned on, ΔV, can be approximated by:

$$\Delta V \approx \frac{Q_{GATE}}{C_{BOOT}} \quad . \qquad (4)$$

So, for a factor of 20, ΔV would be approximately 5% of V_{BOOT}.

The maximum voltage across the bootstrap capacitor under normal operating conditions is V_{REG}(max). However, in some circumstances the voltage may transiently reach 18 V, the clamp voltage of the Zener diodes between the Cx and Sx pins. In most applications, with a good ceramic capacitor the working voltage can be limited to 16 V.

Bootstrap Charging

It is good practice to ensure the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested. The time required to charge the capacitor, t_{CHARGE} (µs), is approximated by:

$$t_{CHARGE} = \frac{C_{BOOT} \times \Delta V}{500} \quad , \qquad (5)$$

where C_{BOOT} is the value of the bootstrap capacitor, in nF, and ΔV is the required voltage of the bootstrap capacitor.

At power-up and when the drives have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case ΔV can be considered to be the full high-side drive voltage, 12 V. Otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the Sx pin is pulled low and current flows from VREG through the internal bootstrap diode circuit to C_{BOOT}.

Bootstrap Charge Management

The A4933 provides automatic bootstrap capacitor charge management. The bootstrap capacitor voltage for each phase is continuously checked to ensure that it is above the bootstrap under-voltage threshold, V_{BOOTUV}. If the bootstrap capacitor voltage drops below this threshold, the A4933 will turn on the necessary low-side FET, and continue charging until the bootstrap capacitor exceeds the undervoltage threshold plus the hysteresis, $V_{BOOTUV} + V_{BOOTUVhys}$. The minimum charge time is typically 7 µs, but may be longer for very large values of bootstrap capaci-

tor (>1000 nF). If the bootstrap capacitor voltage does not reach the threshold within approximately 200 µs, an undervoltage fault will be flagged.

VREG Capacitor Selection

The internal reference, VREG, supplies current for the low-side gate drive circuits and the charging current for the bootstrap capacitors. When a low-side FET is turned on, the gate-drive circuit will provide the high transient current to the gate that is necessary to turn on the FET quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator, and must be supplied by an external capacitor connected to VREG.

The turn-on current for the high-side FET is similar in value to that for the low-side FET, but is mainly supplied by the bootstrap capacitor. However the bootstrap capacitor must then be recharged from the VREG regulator output. Unfortunately the bootstrap recharge can occur a very short time after the low-side turn-on occurs. This requires that the value of the capacitor connected between VREG and AGND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side FET turn-on and a bootstrap capacitor recharge. A value of 20 × C_{BOOT} is a reasonable value. The maximum working voltage will never exceed V_{REG}, so the capacitor can be rated as low as 15 V. This capacitor should be placed as close as possible to the VREG pin.

Supply Decoupling

Because this is a switching circuit, there are current spikes from all supplies at the switching points. As with all such circuits, the power supply connections should be decoupled with a ceramic capacitor, typically 100 nF, between the supply pin and ground. These capacitors should be connected as close as possible to the device supply pins VBB and VDD, and the power ground pin, PGND.

Power Dissipation

In applications where a high ambient temperature is expected, the on-chip power dissipation may become a critical factor. Careful attention should be paid to ensure the operating conditions allow the A4933 to remain in a safe range of junction temperature.

The power consumed by the A4933, P_D, can be estimated by:

$$P_D = P_{BIAS} + P_{CPUMP} + P_{SWITCHING} \quad , \tag{6}$$

given:

$$P_{BIAS} = V_{BB} \times I_{BB} \quad ; \tag{7}$$

$$P_{CPUMP} = [(2 \times V_{BB}) - V_{REG}] \times I_{AV} \quad , \text{for } V_{BB} < 15 \text{ V},$$
$$\text{or}$$
$$= [V_{BB} - V_{REG}] \times I_{AV} \quad , \text{for } V_{BB} \geq 15 \text{ V}, \tag{8}$$

$$P_{SWITCHING} = Q_{GATE} \times V_{REG} \times N \times f_{PWM} \times \text{Ratio} \quad ; \tag{9}$$

where:

$$I_{AV} = Q_{GATE} \times N \times f_{PWM} \quad ,$$

N is the number of FETs switching during a PWM cycle, and

$$\text{Ratio} = \frac{10}{R_{GATE} + 10} \quad .$$

Braking

The A4933 can be used to perform dynamic braking by either forcing all low-side FETs on and all high-side FETs off or, conversely, by forcing all low-side FETs off and all high-side FETs on. This will effectively short-circuit the back EMF of the motor, creating a breaking torque.

During braking, the load current can be approximated by:

$$I_{BRAKE} = \frac{V_{BEMF}}{R_L} \quad , \tag{10}$$

where V_{BEMF} is the voltage generated by the motor and R_L is the resistance of the phase winding.

Care must be taken during braking to ensure that the maximum ratings of the power FETs are not exceeded. Dynamic braking is equivalent to slow decay with synchronous rectification and all phases enabled.

The A4933 can also be used to perform regenerative braking. This is equivalent to reversing the motor commutation sequence or using fast decay with synchronous rectification. Note that phase commutation must continue for regenerative braking to operate and the supply must be capable of managing the reverse current, such as by connecting a resistive load or dumping the current to a battery or capacitor.

Current Sense Amplifier

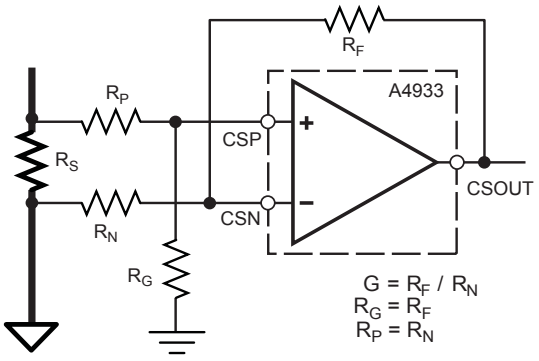
The gain of the current sense amplifier is set using external input and feedback resistors. Output offset can also be added using external resistors. Care must be taken to ensure that the input impedances seen from either end of the sense resistor match.

For the basic configuration shown in figure 4A, the two input resistors, RN and RP, have matched values. The feedback resistor, RF, between CSN and CSOUT, and the ground reference resistor, RG, between CSP and AGND also have matched values. The gain of the sense amplfier, G, is determined by the relative values of RF and RN, and is approximately:

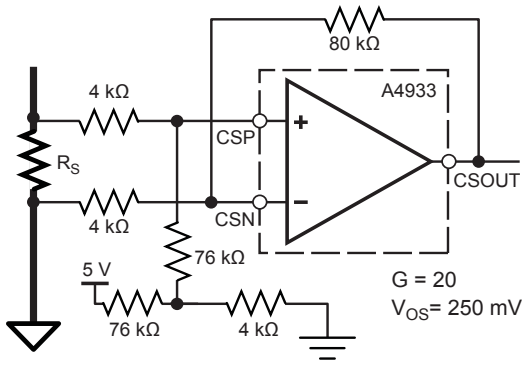
$$G = \frac{R_F}{R_N} \quad , \tag{11}$$

If an output offset is required, for example to allow reverse current measurement, then this can be generated by adding offset to the CSP input through the RG resistor. Because the amplifier is operating in a closed loop, any offset added to CSP will be mirrored at the output.

Figure 4B shows suitable resistor values for a gain, G, of 20 and an output offset, V_{OS}, of 250 mV.



(A) Basic configuration



(B) Typical Configuration

Figure 4. Current sense amplifier configurations

Layout Recommendations

Careful consideration must be given to PCB layout when designing high frequency, fast switching, high current circuits. The following are recommendations regarding some of these considerations:

- The A4933 analog ground, AGND, and power ground, PGND, should be connected together at the package pins. This common point, and the high-current return of the external FETs, should return separately to the negative side of the motor supply filtering capacitor. This will minimize the effect of switching noise on the device logic and analog reference.
- The exposed thermal pad and all NC pins of the package should be connected to the common point of AGND and PGND.
- Minimize stray inductance by using short, wide copper traces at the drain and source terminals of all power FETs. This includes motor lead connections, the input power bus, and the common source of the low-side power FETs. This will minimize voltages induced by fast switching of large load currents.
- Consider the use of small (100 nF) ceramic decoupling capacitors across the sources and drains of the power FETs to limit fast transient voltage spikes caused by the inductance of the circuit trace.
- Keep the gate discharge return connections Sx and LSS as short as possible. Any inductance on these traces will cause negative transitions on the corresponding A4933 pins, which may exceed the absolute maximum ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these pins with respect to AGND.

- Sensitive connections such as RDEAD and VDSTH, which have very little ground current, should be connected to the Quiet ground (refer to figure 5), which is connected independently, closest to the AGND pin. These sensitive components should never be connected directly to the supply common or to a common ground plane. They must be referenced directly to the AGND pin.
- The supply decoupling for VBB, VREG, and VDD should be connected to the Controller Supply ground, which is connected independently, close to the PGND pin. The decoupling capacitors should also be connected as close as practicable to the relevant supply pin.
- If layout space is limited, then the Quiet ground and the Controller Supply ground may be combined. In this case, ensure that the ground return of the dead time resistor is close to the AGND pin.
- Check the peak voltage excursion of the transients on the LSS pin with reference to the AGND pin, using a close grounded (tip and barrel) probe. If the voltage at LSS exceeds the absolute maximum shown in this datasheet, add additional clamping and capacitance between the LSS pin and the AGND pin as shown in figure 5.
- Gate charge drive paths and gate discharge return paths may carry a large transient current pulse. Therefore, the traces from GHx, GLx, Sx, and LSS should be as short as possible to reduce the circuit trace inductance.
- Provide an independent connection from LSS to the common point of the power bridge. It is not recommended to connect LSS directly to an xGND pin, as this may inject noise into sensitive functions such as the timer for dead time. The LSS connection should not be used for the CSP connection.
- The inputs to the sense amplifier, CSP and CSN, should have independent circuit traces. For best results, they should be matched in length and route.
- A low-cost diode can be placed in the connection to VBB to provide reverse battery protection. In reverse battery conditions, it is possible to use the body diodes of the power FETs to clamp the reverse voltage to approximately 4 V. In this case, the additional diode in the VBB connection will prevent damage to the A4933 and the VDRAIN input will survive the reverse voltage.

Note that the above are only recommendations. Each application is different and may encounter different sensitivities. A driver running a few amps will be less susceptible than one running with 150 A, and each design should be tested at the maximum current to ensure any parasitic effects are eliminated.

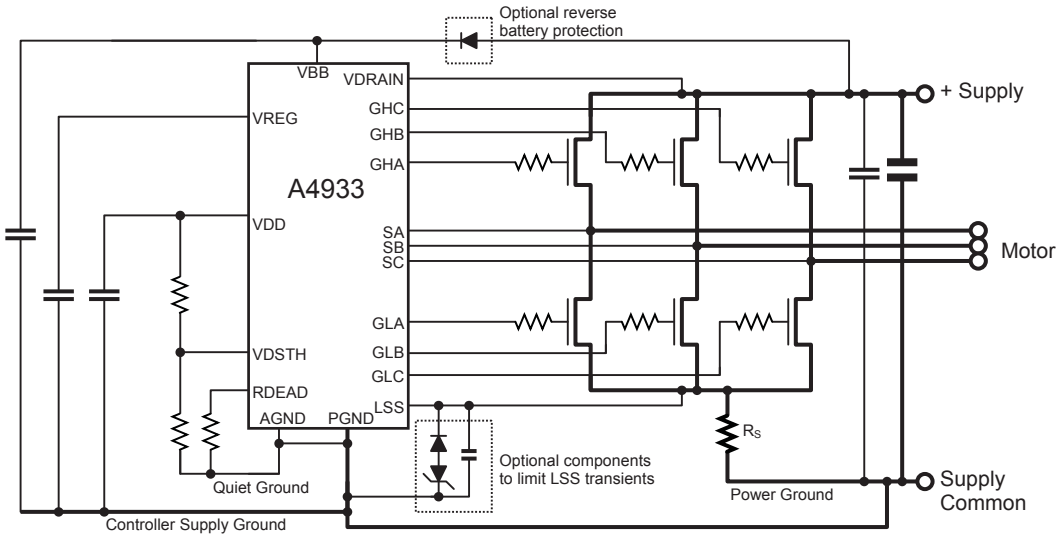
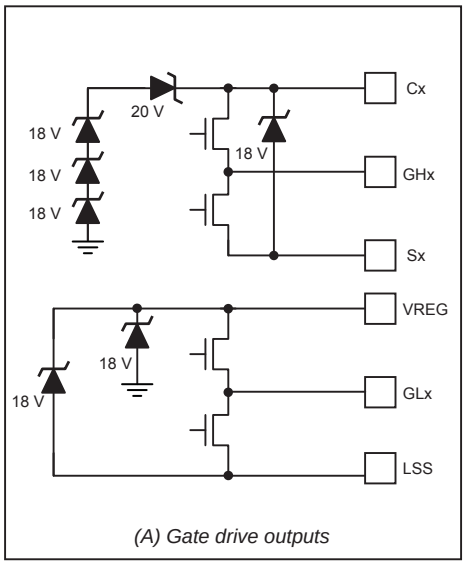
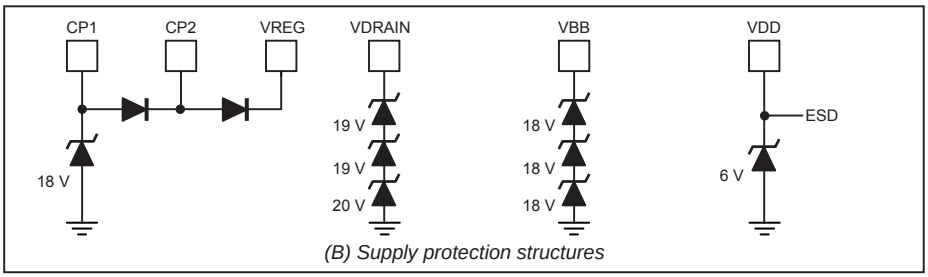


Figure 5. Supply routing suggestions

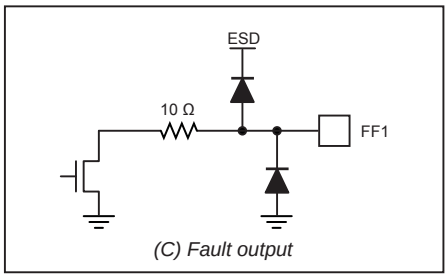
Input and Output Structures



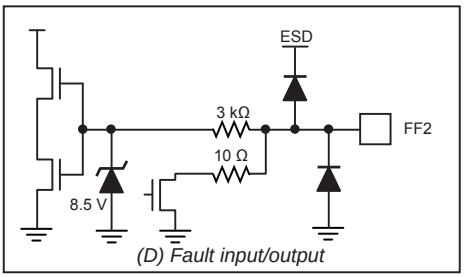
(A) Gate drive outputs



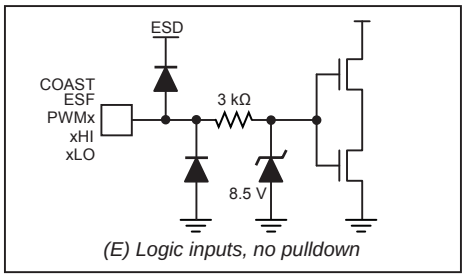
(B) Supply protection structures



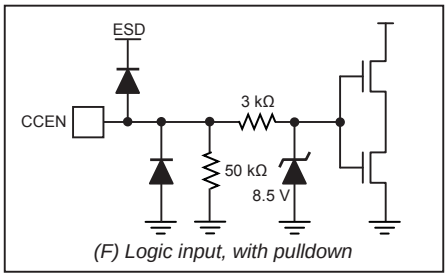
(C) Fault output



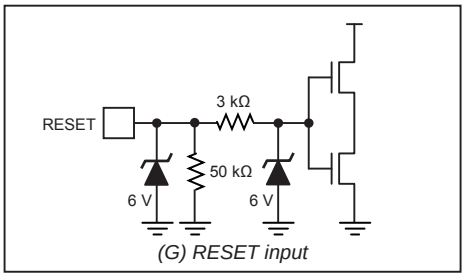
(D) Fault input/output



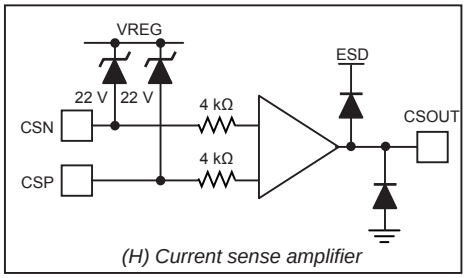
(E) Logic inputs, no pulldown



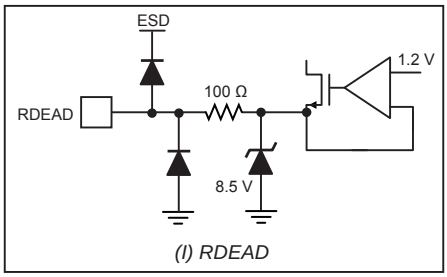
(F) Logic input, with pulldown



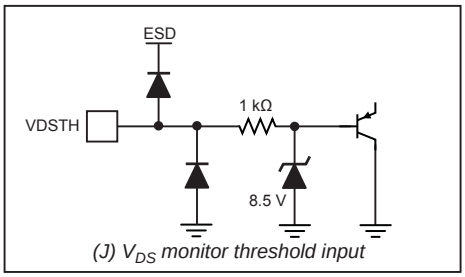
(G) RESET input



(H) Current sense amplifier

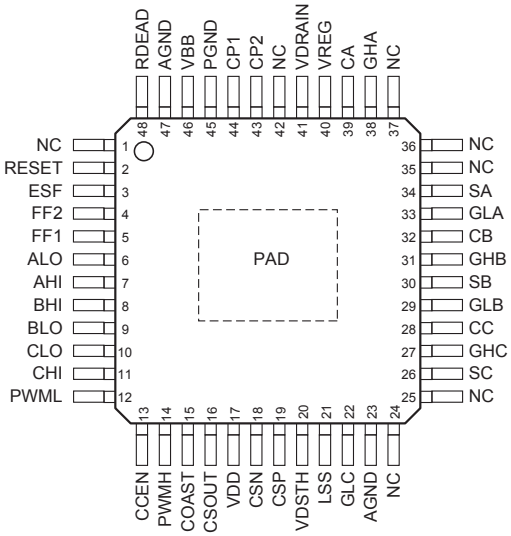


(I) RDEAD



(J) V_{DS} monitor threshold input

Pin-out Diagram

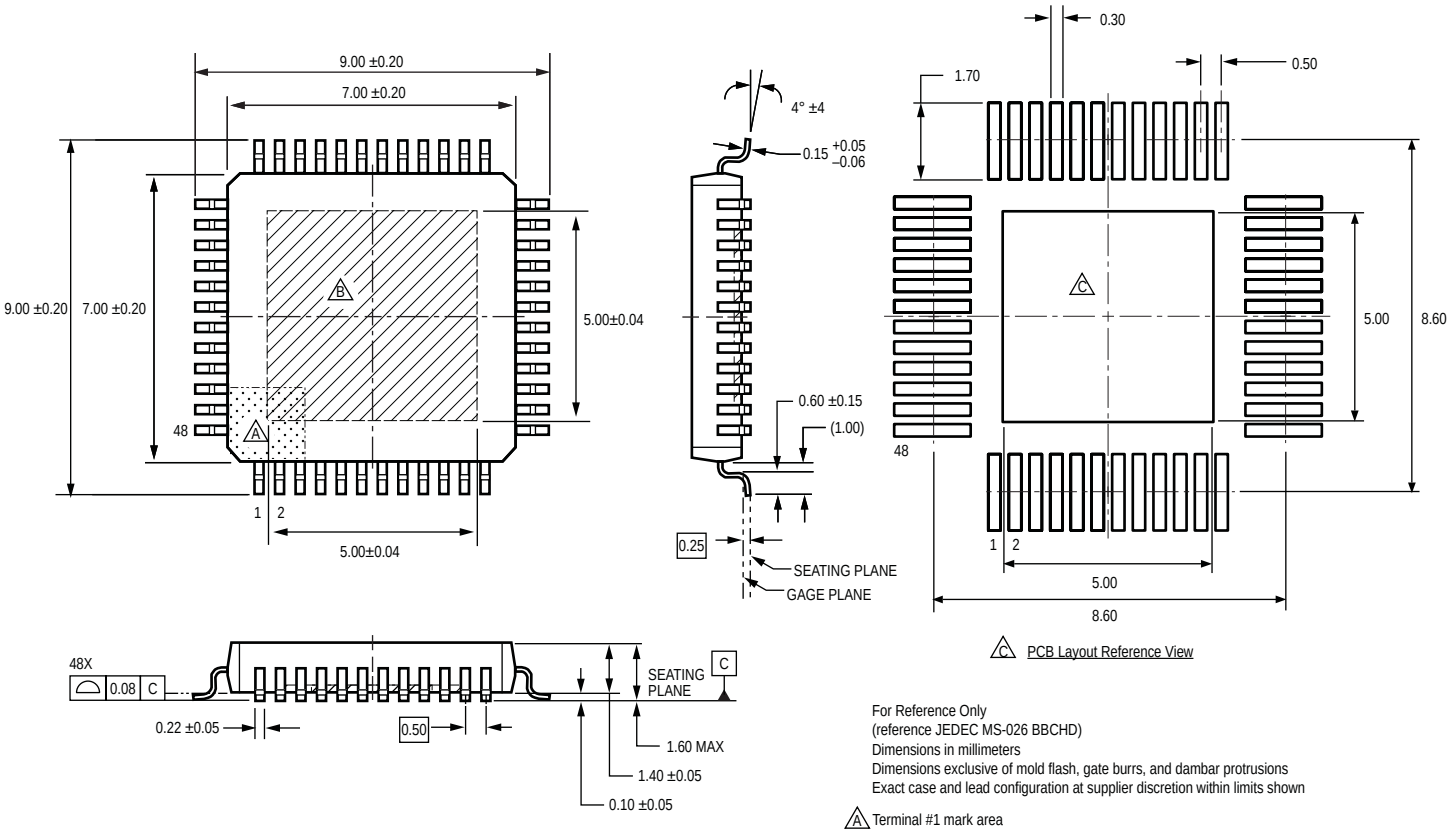


Terminal List

Pin	Pin Name	Pin Description
1, 24, 25, 35, 36, 37, 42	NC	No internal connection; connect to AGND
2	RESET	Standby mode control
3	ESF	Enable Stop on Fault input
4	FF2	Fault Flag 2 and serial clock input
5	FF1	Fault Flag 1 and serial data output
6	ALO	Control input phase A low-side
7	AHI	Control input phase A high-side
8	BHI	Control input phase B high-side
9	BLO	Control input phase B low-side
10	CLO	Control input phase C low-side
11	CHI	Control input phase C high-side
12	PWML	Low-side PWM input
13	CCEN	Cross-conduction enable
14	PWMH	High-side PWM input
15	COAST	Coast input
16	CSOUT	Current sense output
17	VDD	Logic supply
18	CSN	Current sense negative input
19	CSP	Current sense positive input
20	VDSTH	Fault threshold voltage
21	LSS	Low-side source

Pin	Pin Name	Pin Description
22	GLC	Low-side gate drive phase C
23	AGND	Analog ground
26	SC	Motor connection phase C
27	GHC	High-side gate drive phase C
28	CC	Bootstrap capacitor phase C
29	GLB	Low-side gate drive phase B
30	SB	Motor connection phase B
31	GHB	High-side gate drive phase B
32	CB	Bootstrap capacitor phase B
33	GLA	Low-side gate drive phase A
34	SA	Motor connection phase A
38	GHA	High-side gate drive phase A
39	CA	Bootstrap capacitor phase A
40	VREG	Gate drive supply output
41	VDRAIN	High-side drain voltage sense
43	CP2	Pump capacitor
44	CP1	Pump capacitor
45	PGND	Power ground
46	VBB	Main power supply
47	AGND	Analog ground
48	RDEAD	Dead time setting
–	PAD	Exposed thermal pad; connect to AGND

Package JP 48-Pin LQFP with Exposed Thermal Pad



For Reference Only
(reference JEDEC MS-026 BBCHD)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 QFP50P900X900X160-48M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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