Document Title

512K X 32 Bit X 4 Banks Synchronous DRAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	December 28, 2004	Preliminary

Preliminary — *512K X 32 Bit X 4 Banks Synchronous DRAM*

Features

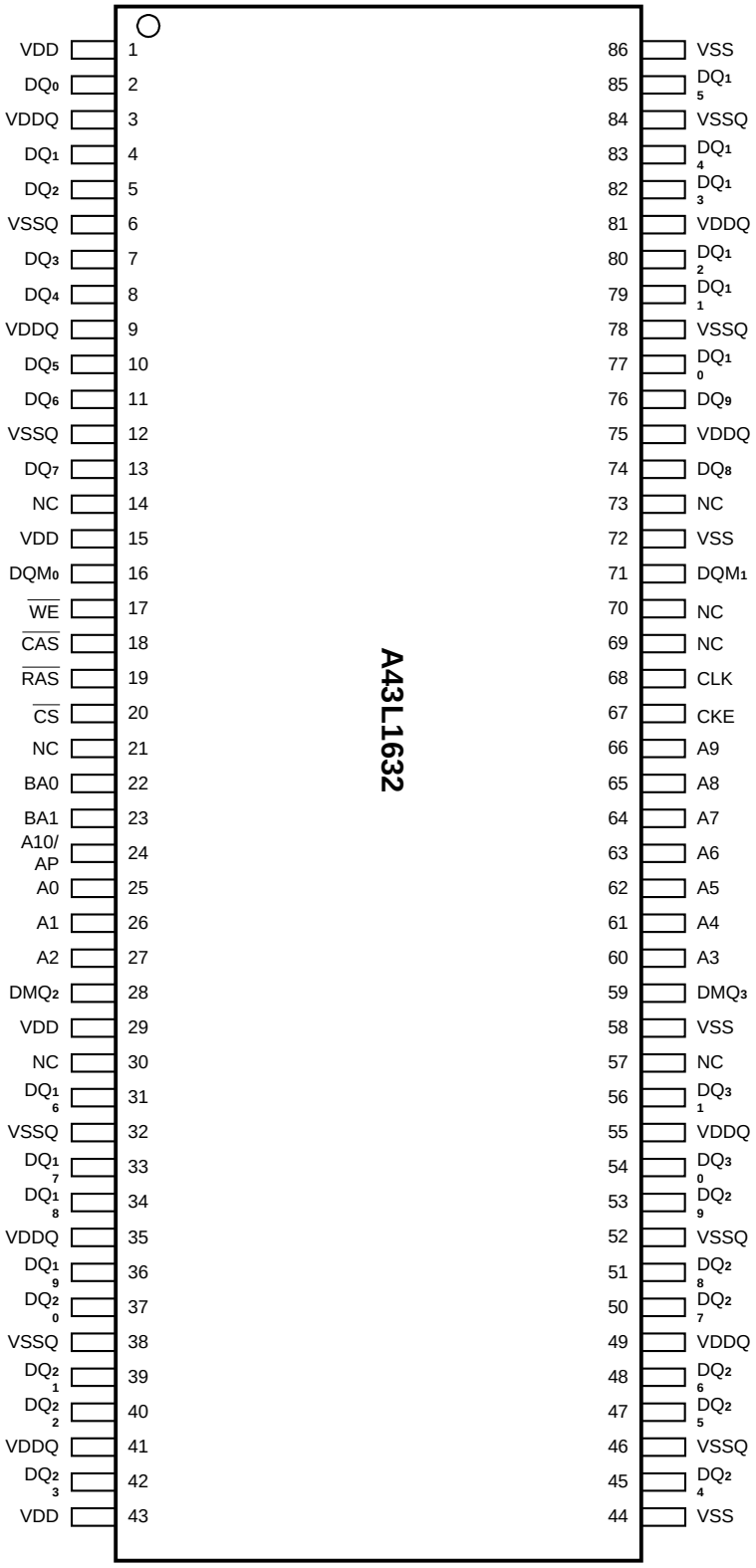
- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks / Pulse $\overline{RAS}$
- MRS cycle with address key programs
  - CAS Latency (2,3)
  - Burst Length (1,2,4,8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Deep Power Down Mode
- Burst Read Single-bit Write operation
- Clock Frequency (max) : 166MHz @ CL=3 (-6)
  143MHz @ CL=3 (-7)
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)
- Self refresh with programmable refresh period through EMRS cycle
- Programmable Power Reduction Feature by partial array activation during Self-refresh through EMRS cycle
- 86 Pin TSOP (II)
- operating temperature range: 0ºC to + 70ºC

General Description

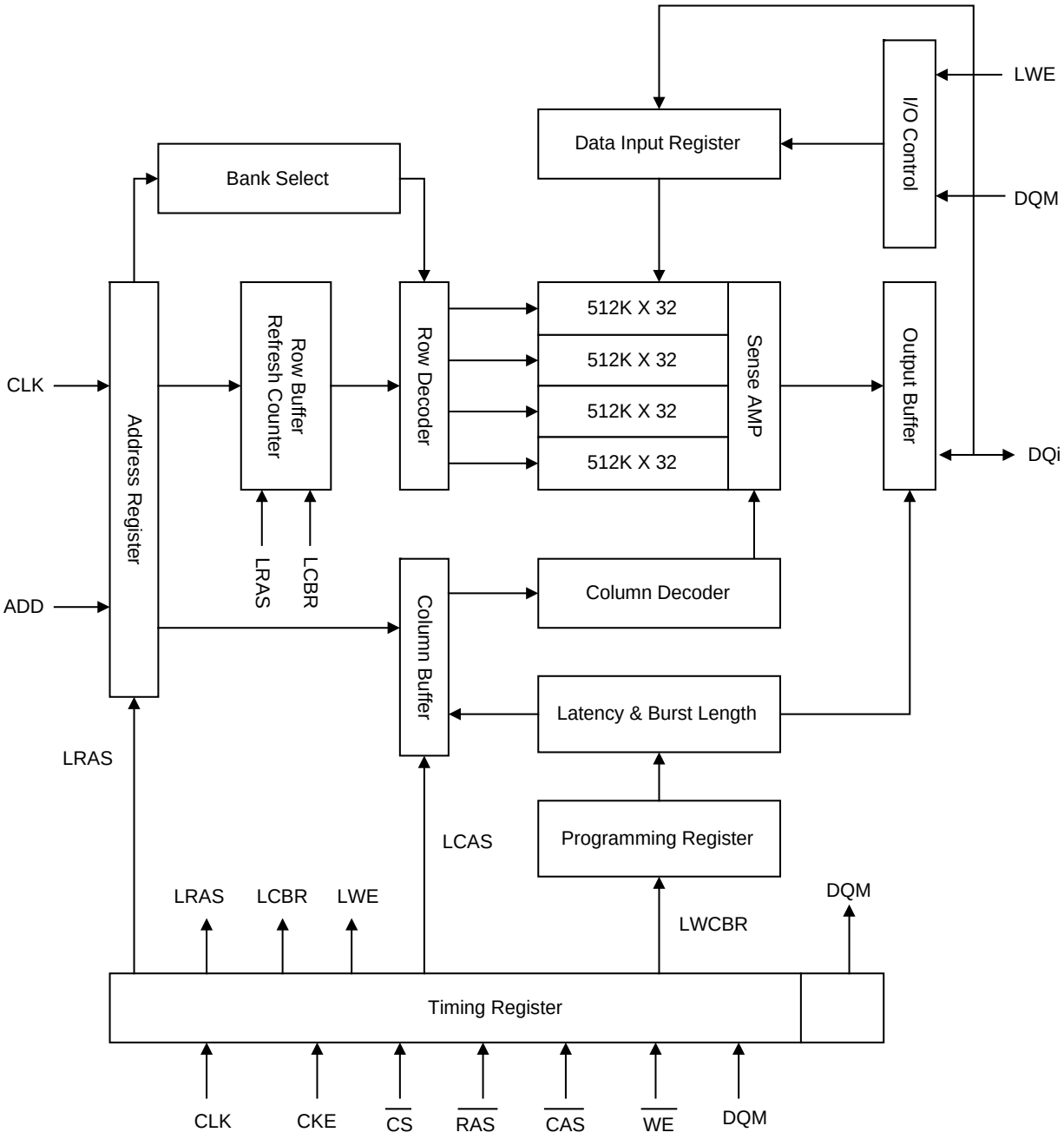
The A43L1632 is 67,108,864 bits Low Power synchronous high data rate Dynamic RAM organized as 2 X 1,048,576 words by 32 bits, fabricated with AMIC's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Pin Configuration

■ **TSOP (II)**



Block Diagram



Pin Descriptions

Symbol	Name	Description
CLK	System Clock	Active on the positive going edge to sample all inputs.
$\overline{CS}$	Chip Select	Disables or Enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock + tss prior to new command. Disable input buffers for power down in standby.
A0~A10	Address	Row / Column addresses are multiplexed on the same pins. Row address : RA0~RA10, Column address: CA0~CA7
BS0, BS1	Bank Select Address	Selects bank to be activated during row address latch time. Selects band for read/write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and Row precharge.
DQM_{0-3}	Data Input/Output Mask	Makes data output Hi-Z, t SHZ after the clock and masks the output. Blocks data input when DQM_{0-3} active.
DQ_{0-31}	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power Supply/Ground	Power Supply: +2.5V±0.125V/Ground
VDDQ/VSSQ	Data Output Power/Ground	Provide isolated Power/Ground to DQs for improved noise immunity.
NC/RFU	No Connection	

Absolute Maximum Ratings*

Voltage on any pin relative to VSS (Vin, Vout) . . . . . .
. . . . . .

Decoupling Capacitance Guide Line

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between VDD and VSS	C_{DC1}	0.1 + 0.01	μF
Decoupling Capacitance between VDDQ and VSSQ	C_{DC2}	0.1 + 0.01	μF

Note: 1. VDD and VDDQ pins are separated each other.
All VDD pins are connected in chip. All VDDQ pins are connected in chip.
2. VSS and VSSQ pins are separated each other
All VSS pins are connected in chip. All VSSQ pins are connected in chip.

DC Electrical Characteristics

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C or T_A = -40ºC to +85ºC)

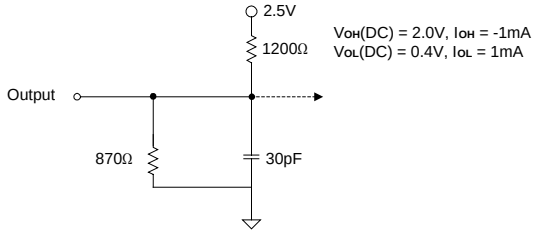
Symbol	Parameter	Test Conditions	Speed		Unit	Notes
			-6	-7		
I_{CC1}	Operating Current (One Bank Active)	Burst Length = 1 $t_{RC} \geq t_{RC}$(min), tcc ≥ tcc(min), I_{OL} = 0mA	90	80	mA	1
I_{CC2} P	Precharge Standby Current in power-down mode	CKE ≤ V_{IL}(max), tcc = 15ns	35	30	mA	
I_{CC2} PS		CKL ≤ VIL(max), tcc = ∞	1	1		
I_{CC2}N	Precharge Standby Current in non power-down mode	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns	8		mA	
I_{CC2}NS		CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable.	1			
I_{CC3}N	Active Standby current in non power-down mode (One Bank Active)	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns	60	55	mA	
I_{CC4}	Operating Current (Burst Mode)	I_{OL} = 0mA, Page Burst All bank Activated, t_{CCD} = t_{CCD} (min)	165	145	mA	1
I_{CC5}	Refresh Current	$t_{RC} \geq t_{RC}$ (min)	120	110	mA	2
I_{CC6}	Self Refresh Current	CKE = 0.2V	1	1	mA	

Note: 1. Measured with outputs open. Addresses are changed only one time during tcc(min).
2. Refresh period is 64ms. Addresses are changed only one time during tcc(min).

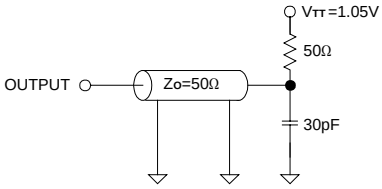
AC Operating Test Conditions

(VDD = 3.3V ±0.3V, T_A = 0°C to +70°C or T_A = -40ºC to +85ºC)

Parameter	Value
AC input levels	V_{IH}/V_{IL} = 2.4V/0.4V
Input timing measurement reference level	1.4V
Input rise and all time (See note3)	tr/tf = 1ns/1ns
Output timing measurement reference level	1.4V
Output load condition	See Fig.2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

AC Characteristics

(AC operating conditions unless otherwise noted)

Symbol	Parameter		-6		-7		Unit	Note
			Min	Max	Min	Max		
tCC	CLK cycle time	CL=3	6	1000	7	1000	ns	1
		CL=2	10		10			
		CL=1	25		25			
tSAC	CLK to valid Output delay	CL=3	-	5.5	-	5.5	ns	1,2
		CL=2	-	6	-	6		
		CL=1	-	22	-	22		
tOH	Output data hold time		2	-	2	-	ns	2
tCH	CLK high pulse width	CL=3	2.5	-	3	-	ns	3
		CL=2	3	-	3	-		

CL=CAS Latency.

AC Characteristics (continued)

(AC operating conditions unless otherwise noted)

Symbol	Parameter		-6		-7		Unit	Note
			Min	Max	Min	Max		
t_{CL}	CLK low pulse width	CL=3	2.5	-	3	-	ns	3
		CL=2	3	-	3	-		
t_{SS}	Input setup time	CL=3	1.5	-	1.75	-	ns	3
		CL=2	2.5	-	2.5	-		
t_{SH}	Input hold time		1	-	1	-	ns	3
t_{SLZ}	CLK to output in Low-Z		1	-	1	-	ns	2
t_{SHZ}	CLK to output in Hi-Z	CL=3	-	5.5	-	5.5	ns	
		CL=2	-	6	-	6		

CL=CAS Latency. *All AC parameters are measured from half to half.

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

Operating AC Parameter

(AC operating conditions unless otherwise noted)

Symbol	Parameter	Version		Unit	Note
		-6	-7		
$t_{RRD(min)}$	Row active to row active delay	12	14	ns	1
$t_{RCD(min)}$	$\overline{RAS}$ to $\overline{CAS}$ delay	18	20	ns	1
$t_{RP(min)}$	Row precharge time	18	20	ns	1
$t_{RAS(min)}$	Row active time	42	48	ns	1
$t_{RAS(max)}$		100		µs	
$t_{RC(min)}$	Row cycle time	60	70	ns	1
$t_{CDL(min)}$	Last data in new col. Address delay	6	7	ns	2
$t_{RDL(min)}$	Last data in row precharge	12	14	ns	2
$t_{BDL(min)}$	Last data in to burst stop	6	7	ns	2
$t_{CCD(min)}$	Col. Address to col. Address delay	6	7	ns	

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.

Simplified Truth Table

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BS0 BS1	A10 /AP	A9~A0,	Notes
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Addr.		4
Read & Column Addr.	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Addr.	4
	Auto Precharge Enable										H		4,5
Write & Column Addr.	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Addr.	4
	Auto Precharge Enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	L	H	H	H	X	X			
					H	X	X	X					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	L	H	H	H	X	X			
					H	X	X	X					
		Exit	L	H	L	V	V	V	X				
					H	X	X	X					
DQM			H	X					V	X			6
No Operation Command			H	X	L	H	H	H	X	X			
					H	X	X	X					
Deep Power Down Entry			H	L	L	H	H	L	X	X			
Deep Power Down Exit			L	H	X	X	X	X	X	X			7

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

Note : 1. OP Code: Operand Code
A0~A10, BS0, BS1: Program keys. (@MRS)
2. MRS can be issued only when all banks are at precharge state.
A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions is same as CBR refresh of DRAM.
The automatical precharge without Row precharge command is meant by "Auto".
Auto/Self refresh can be issued only when all banks are at precharge state.
4. BS0, BS1 : Bank select address.
If both BS1 and BS0 are "Low" at read, write, row active and precharge, bank A is selected.
If both BS1 is "Low" and BS0 is "High" at read, write, row active and precharge, bank B is selected.
If both BS1 is "High" and BS0 is "Low" at read, write, row active and precharge, bank C is selected.
If both BS1 and BS0 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BS1 and BS0 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command cannot be issued.
Another bank read/write command can be issued at every burst length.
6. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0)
but masks the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2)
7. After Deep Power Down mode exit, a full new initialization of the memory device is mandatory.

Mode Register Filed Table to Program Modes

Register Programmed with MRS

Address	BS1	BS0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	0	0	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		
	(Note 3)		(Note 2)	(Note 1)									

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Vendor	0	0	1	1	1	Interleave	0	0	1	2	2
1	0	Use	0	1	0	2			0	1	0	4	4
1	1	Only	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	256(Full)	Reserved

Note : 1. RFU(Reserved for Future Use) should stay “0” during MRS cycle.
2. If A9 is high during MRS cycle, “Burst Read Single Bit Write” function will be enabled.
3. BS0,BS1 must be 0,0 to select the Mode Register (vs. the Extended Mode Register).

Power Up Sequence

1. Apply power and start clock, Attempt to maintain CKE = “H”, DQM = “H” and the other pins are NOP condition at inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200μs.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 may be changed.

The device is now ready for normal operation.

Burst Sequence (Burst Length = 4)

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

Burst Sequence (Burst Length = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

Device Operations

Clock (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between VIL and VIH. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of set up and hold time around positive edge of the clock for proper functionality and ICC specifications.

Clock Enable (CLK)

The clock enable (CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "tSS + 1 CLOCK" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

Bank Select (BS0, BS1)

This SDRAM is organized as 4 independent banks of 524,288 words X 32 bits memory arrays. The BS0, BS1 inputs is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank select BS0, BS1 is latched at bank activate, read, write mode register set and precharge operations.

Address Input (A0 ~ A10)

The 19 address bits required to decode the 524,288 word locations are multiplexed into 11 address input pins (A0~A10). The 11 bit row address is latched along with $\overline{RAS}$, BS0 and BS1 during bank activate command. The 8 bit column address is latched along with $\overline{CAS}$, $\overline{WE}$, BS0 and BS1during read or write command.

NOP and Device Deselect

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$, and all the address inputs are ignored.

Power-Up

The following sequence is recommended for POWER UP

1. Power must be applied to either CKE and DQM inputs to pull them high and other pins are NOP condition at the inputs before or along with VDD (and VDDQ) supply.
   The clock signal must also be asserted at the same time.
2. After VDD reaches the desired voltage, a minimum pause of 200 microseconds is required with inputs in NOP condition.
3. All banks must be precharged now.
4. Perform a minimum of 2 Auto refresh cycles to stabilize the internal circuitry.
5. Perform a MODE REGISTER SET cycle to program the CAS latency, burst length and burst type as the default value of mode register is undefined.
   At the end of one clock cycle from the mode register set cycle, the device is ready for operation.
   When the above sequence is used for Power-up, all the out-puts will be in high impedance state. The high impedance of outputs is not guaranteed in any other power-up sequence.
   cf.) Sequence of 4 & 5 may be changed.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operation modes of SDRAM. It programs the CAS latency, addressing mode, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A10, BS0 and BS1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ going low is the data written in the mode register. One clock cycle is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length field uses A0~A2, burst type uses A3, addressing mode uses A4~A6, A7~A8, A10, BS0 and BS1 are used for vendor specific options or test mode. And the write burst length is programmed using A9. A7~A8, A10, BS0 and BS1 must be set to low for normal SDRAM operation.
Refer to table for specific codes for various burst length, addressing modes and CAS latencies. BS0 and BS1 have to be set to "0" to enter the Mode Register.

Device Operations (continued)

Bank Activate

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank addresses, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation. t_{RCD}(min) is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has 4 internal banks on the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of all banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before the other bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different banks. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

Burst Read

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{CAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

Burst Write

The burst write command is similar to burst read command, and is used to write data into the SDRAM consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing may not have been completed yet. The burst write can be terminated by issuing a burst read and DQM for blocking data inputs or burst write in the same or the other active bank. The burst stop command is valid only at full page burst length where the writing continues at the end of burst and the burst is wrap around. The write burst can also be terminated by using DQM for blocking data and precharging the bank "t_{RDL}" after the last data input to be written into the active row. See DQM OPERATION also.

DQM Operation

The DQM is used to mask input and output operation. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in the read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock, therefore the masking occurs for a complete cycle. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required.

Precharge

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A10/AP with valid BA of the bank to be precharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank activate command in the desired bank. "t_{RP}" is defined as the minimum time required to precharge a bank.

The minimum number of clock cycles required to complete row precharge is calculated by dividing "t_{RP}" with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank has to be precharged within t_{RAS}(max) from the bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again.

Entry to Power Down, Auto refresh, Self refresh and Mode register Set etc, is possible only when all banks are in idle state.

Auto Precharge

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A10/AP. If burst read or burst write command is issued with low on A10/AP, the bank is left active until a new command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

All Banks Precharge

All banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ with high on A10/AP after both banks have satisfied t_{RAS}(min) requirement, performs precharge on all banks. At the end of tRP after performing precharge all, all banks are in idle state.

Auto Refresh

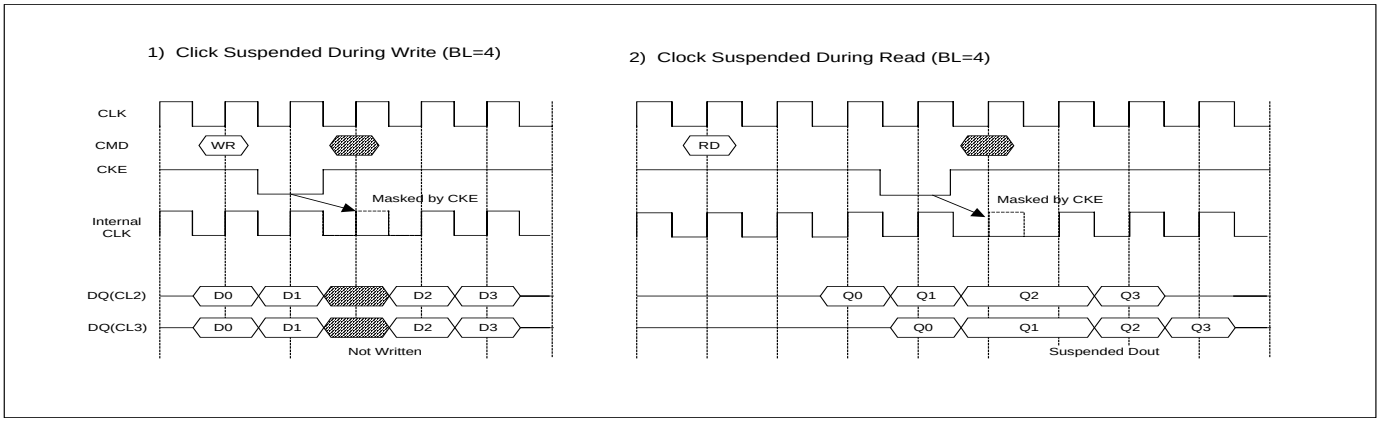
The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with all banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by "t_{RC}(min)". The minimum number of clock cycles required can be calculated by dividing "t_{RC}" with clock cycle time and then rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. All banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or a burst of 4096 auto refresh cycles once in 64ms.

Self Refresh

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.
The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the self refresh.
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of "t_{RC}" before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to used burst 4096 auto refresh cycles immediately after exiting self refresh.

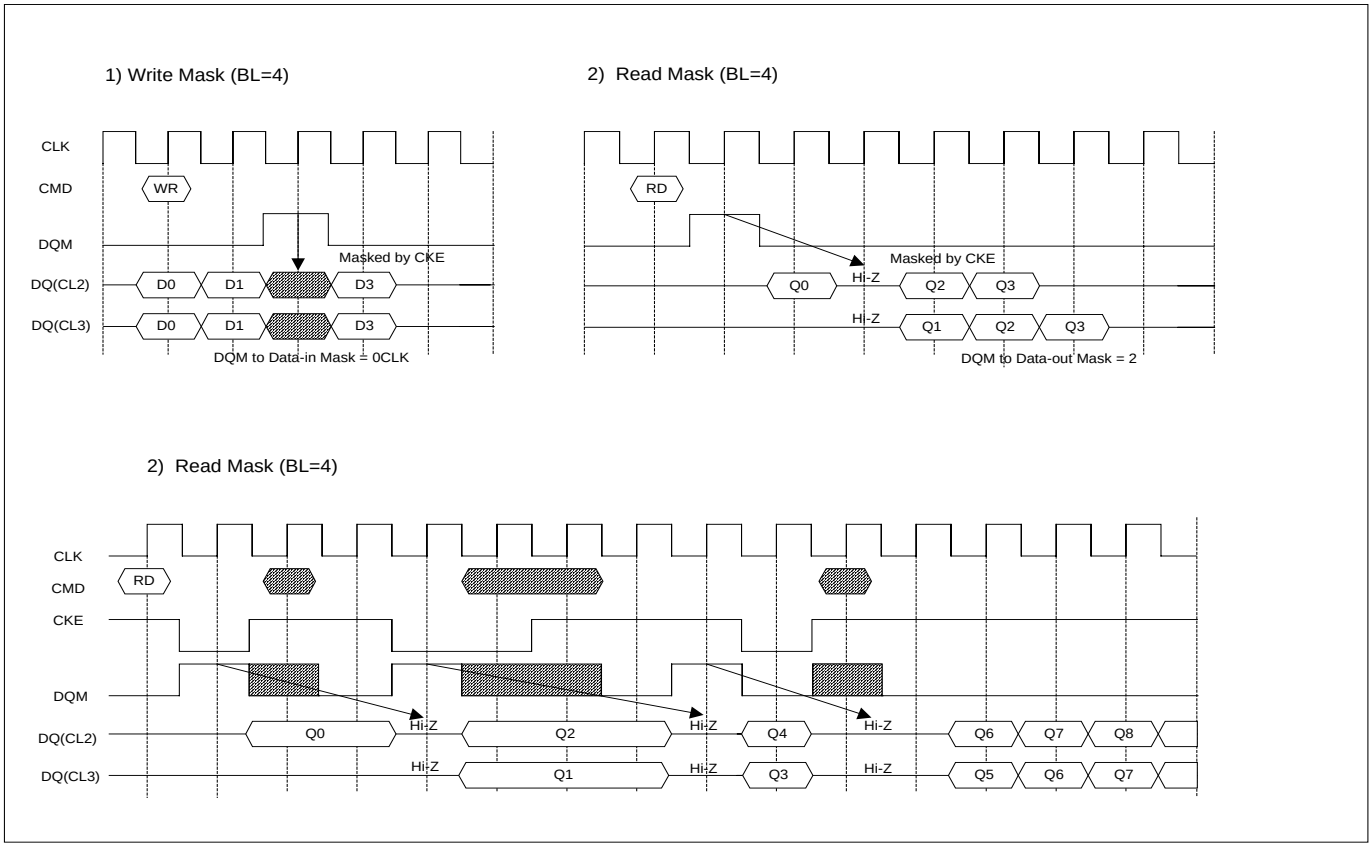
Basic feature And Function Descriptions

1. CLOCK Suspend



Note: CLK to CLK disable/enable=1 clock

2. DQM Operation

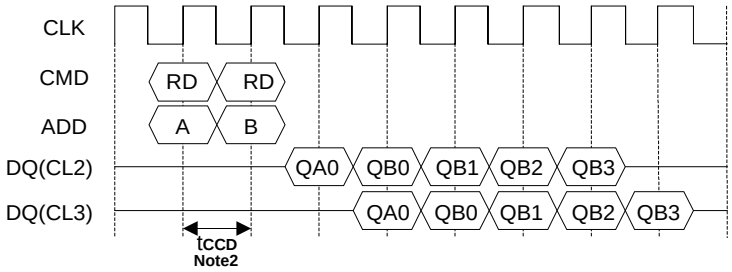


*** Note :** 1. DQM makes data out Hi-Z after 2 clocks which should masked by CKE "L".

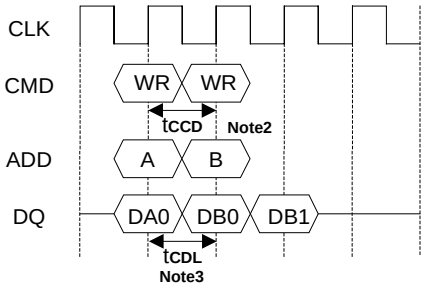
2. DQM masks both data-in and data-out.

3. CAS Interrupt (I)

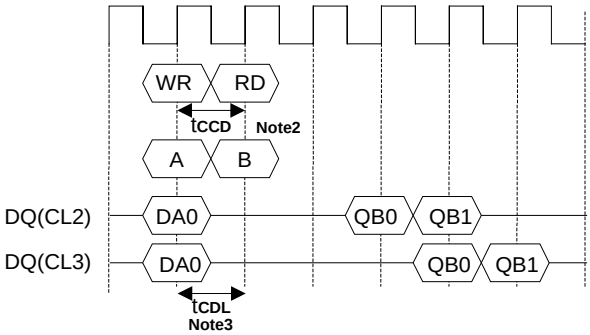
1) Read interrupted by Read (BL=4) Note 1



2) Write interrupted by Write (BL =2)

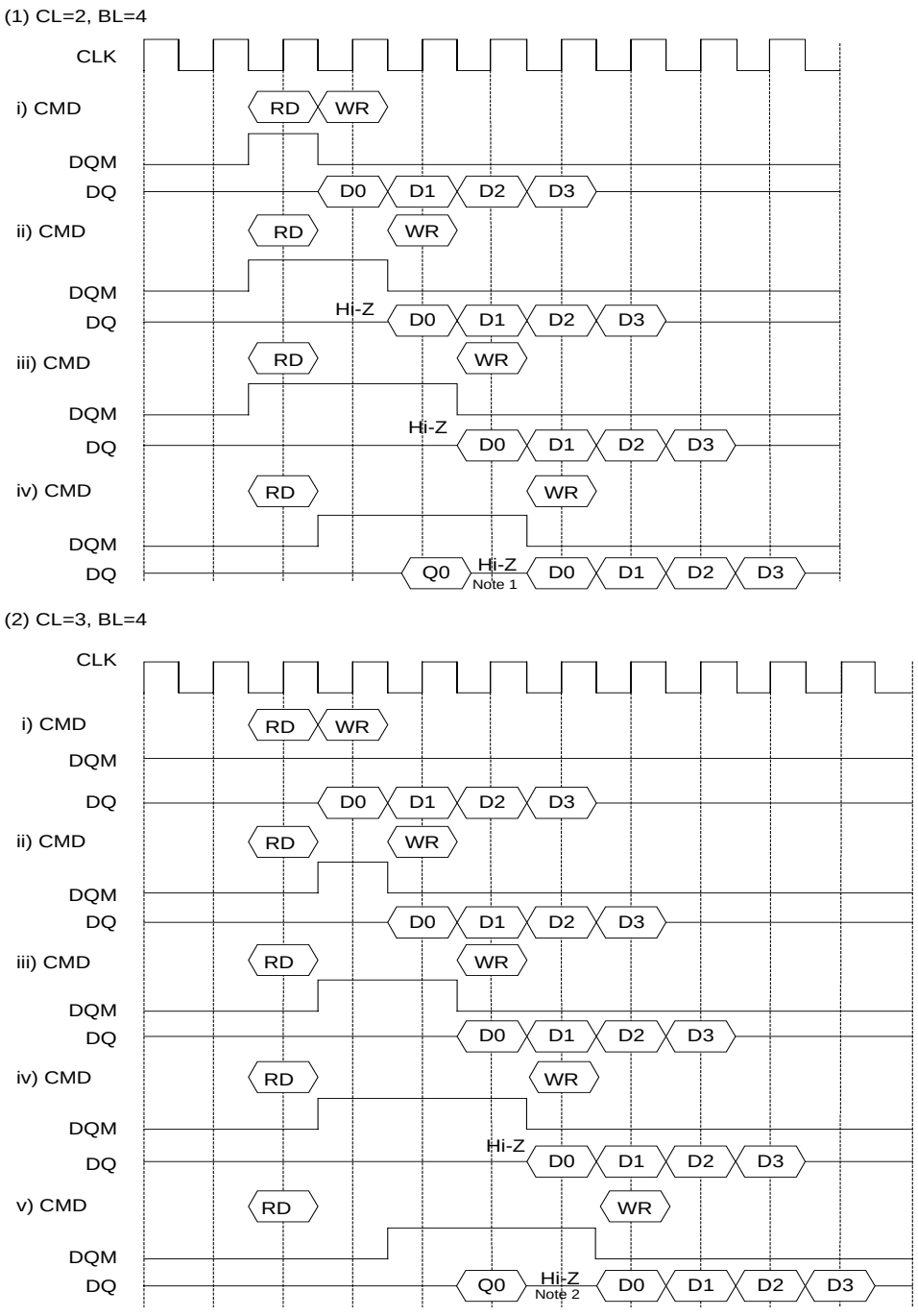


3) Write interrupted by Read (BL =2)



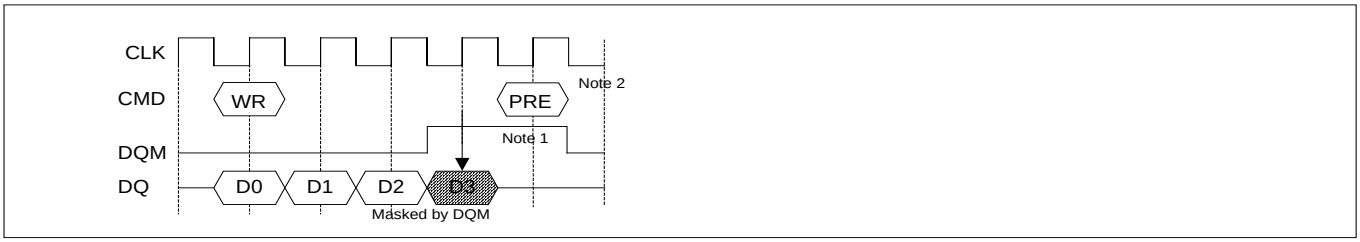
Note : 1. By "Interrupt", It is possible to stop burst read/write by external command before the end of burst.
By "$\overline{CAS}$ Interrupt", to stop burst read/write by $\overline{CAS}$ access; read, write and block write.
2. t_{CCD} : $\overline{CAS}$ to $\overline{CAS}$ delay. (=1CLK)
3. t_{CDL} : Last data in to new column address delay. (= 1CLK).

4. CAS Interrupt (II) : Read Interrupted Write & DQM



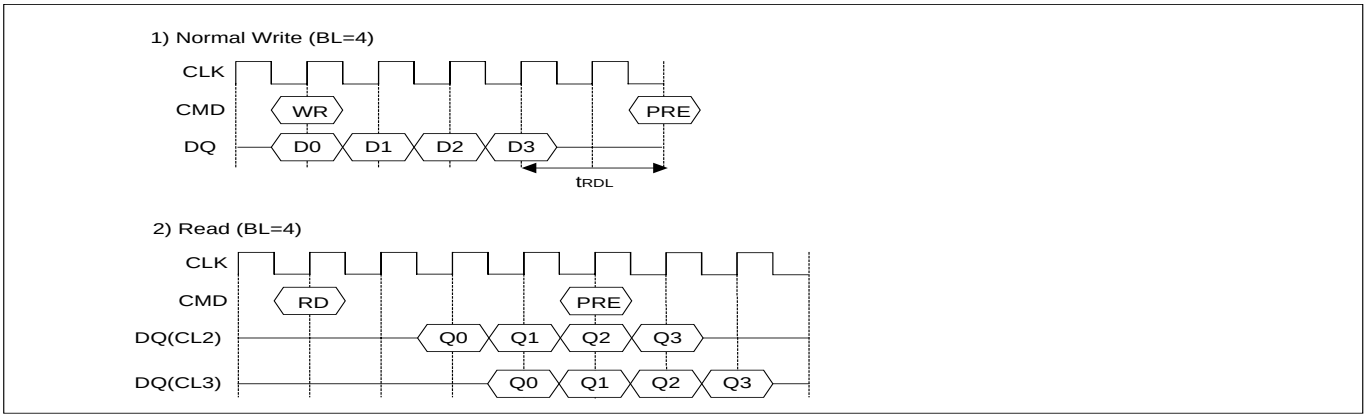
* Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.
2. To prevent bus contention, DQM should be issued which makes a least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM

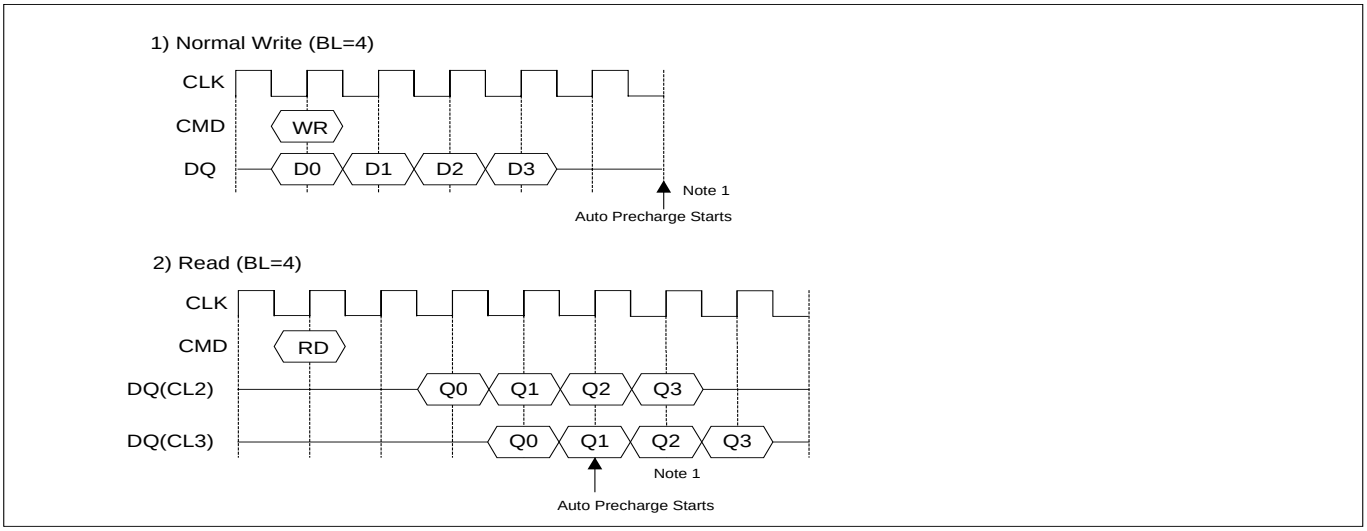


Note : 1. To inhibit invalid write, DQM should be issued.
2. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of dual banks operation.

6. Precharge

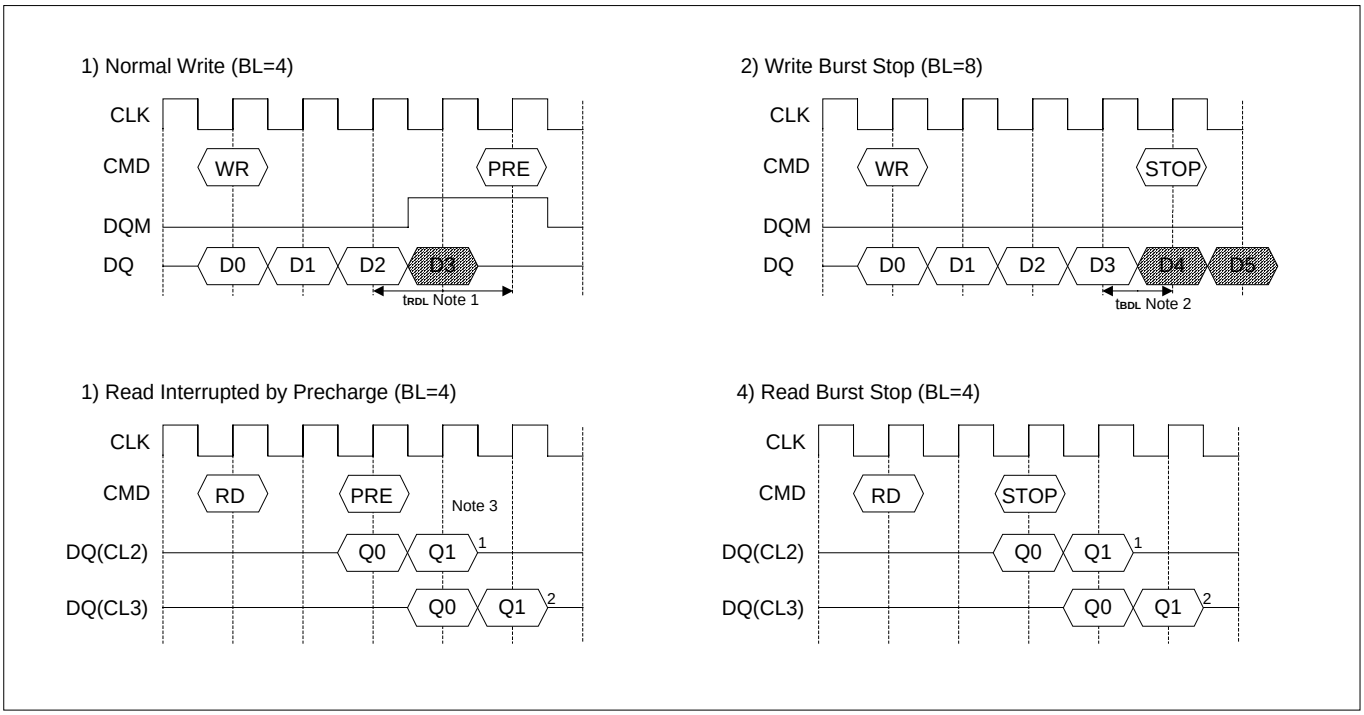


7. Auto Precharge

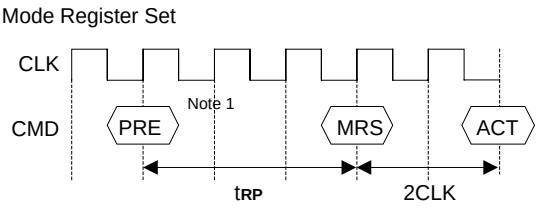


* Note : 1. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of other active bank can be issued from this point.
At burst read/write with auto precharge, $\overline{CAS}$ interrupt of the same/another bank is illegal.

8. Burst Stop & Interrupted by Precharge

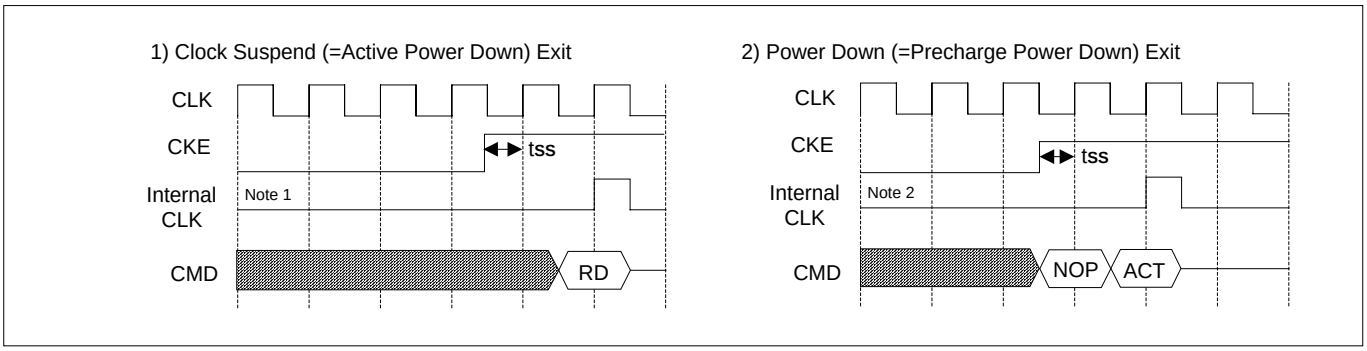


9. MRS

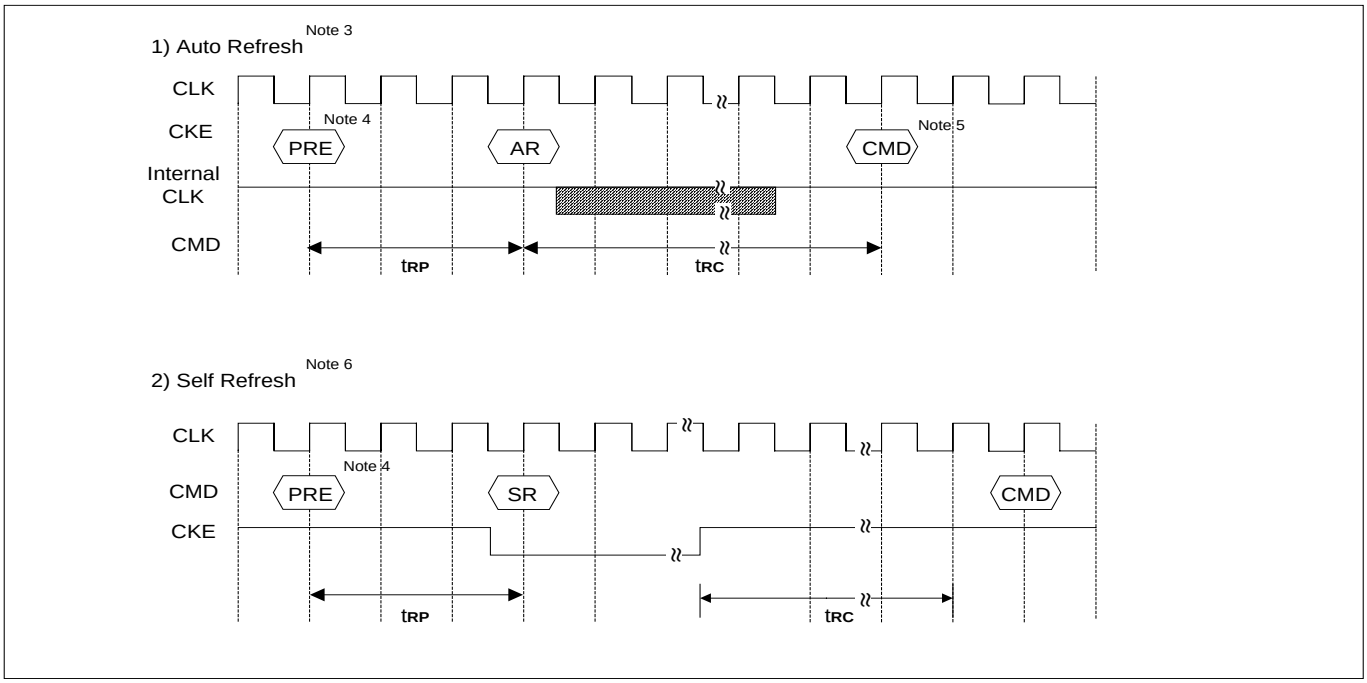


Note : 1. t_{RDL}: 1CLK
2. t_{BDL}: 1CLK; Last data in to burst stop delay.
Read or write burst stop command is valid at every burst length.
3. Number of valid output data after row precharge or burst stop: 1,2 for CAS latency = 2, 3 respectively.
4. PRE: All banks precharge if necessary.
MRS can be issued only when all banks are in precharged state.

10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



* Note : 1. Active power down : one or more bank active state.
2. Precharge power down : both bank precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
No precharge commands are required after Auto Refresh command.
During t_{RC} from auto refresh command, other command can not be accepted.
4. Before executing auto/self refresh command, both banks must be idle state.
5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refresh mode, refresh interval and refresh operation are performed internally.
After self refresh entry, self refresh mode is kept while CKE is LOW.
During self refresh mode, all inputs expect CKE will be don't cared, and outputs will be in Hi-Z state.
During t_{RC} from self refresh exit command, any other command can not be accepted.
Before/After self refresh mode, burst auto refresh cycle (4K cycles) is recommended.

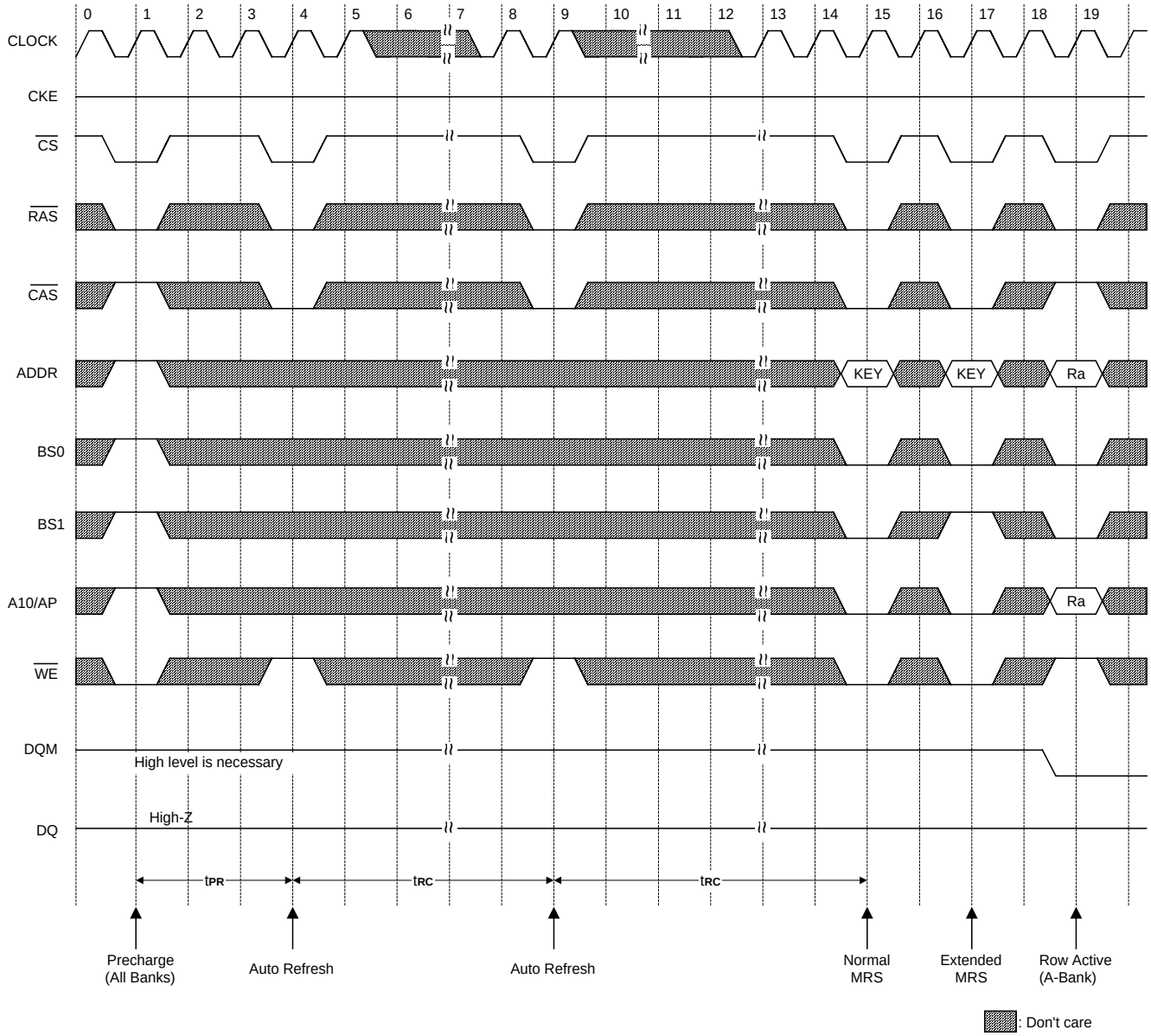
12. About Burst Type Control

Basic MODE	Sequential counting	At MRS A3="0". See the BURST SEQUENCE TABE.(BL=4,8) BL=1,2,4,8 and full page wrap around.
	Interleave counting	At MRS A3=" 1". See the BURST SEQUENCE TABE.(BL=4,8) BL=4,8 At BL=1,2 Interleave Counting = Sequential Counting
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of convention DRAM.

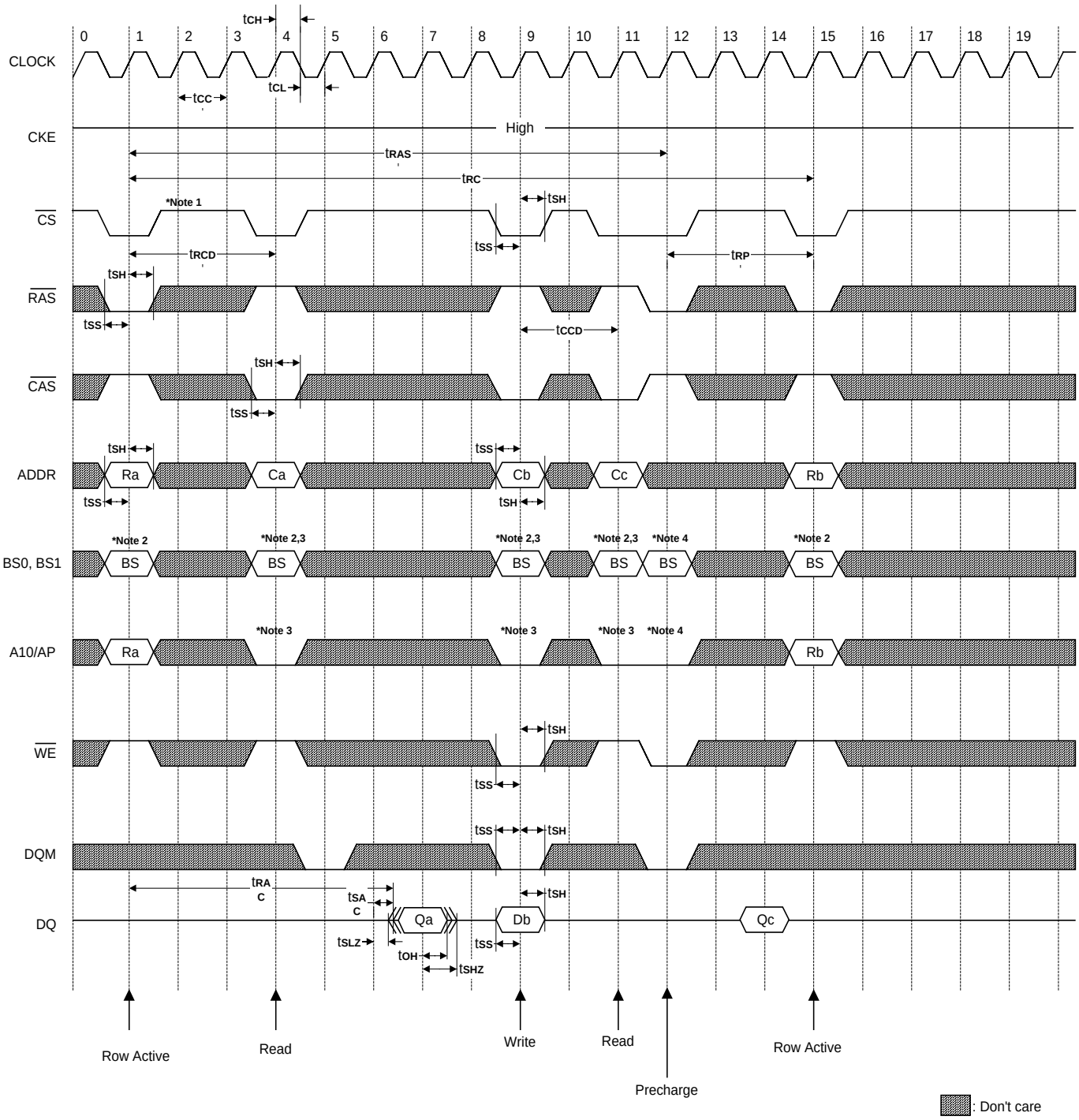
13. About Burst Length Control

Basic MODE	1	At MRS A2,1,0 = "000". At auto precharge, tRAS should not be violated.
	2	At MRS A2,1,0 = "001". At auto precharge, tRAS should not be violated.
	4	At MRS A2,1,0 = "010"
	8	At MRS A2,1,0 = "011".
Special MODE	BRSW	At MRS A9="1". Read burst = 1,2,4,8, full page/write Burst =1 At auto precharge of write, tRAS should not be violated.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank Stops read/write burst with Row precharge. t_{RDL}= 2 with DQM, valid DQ after burst stop is 1,2 for CL=2,3 respectively During read/write burst with auto precharge, $\overline{RAS}$ interrupt cannot be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst or block write. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

Power On Sequence for Low Power SDRAM



Single Bit Read-Write-Read Cycles (Same Page) @CAS Latency=3, Burst Length=1



* Note : 1. All inputs can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by BS0, BS1.

BS1	BS0	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

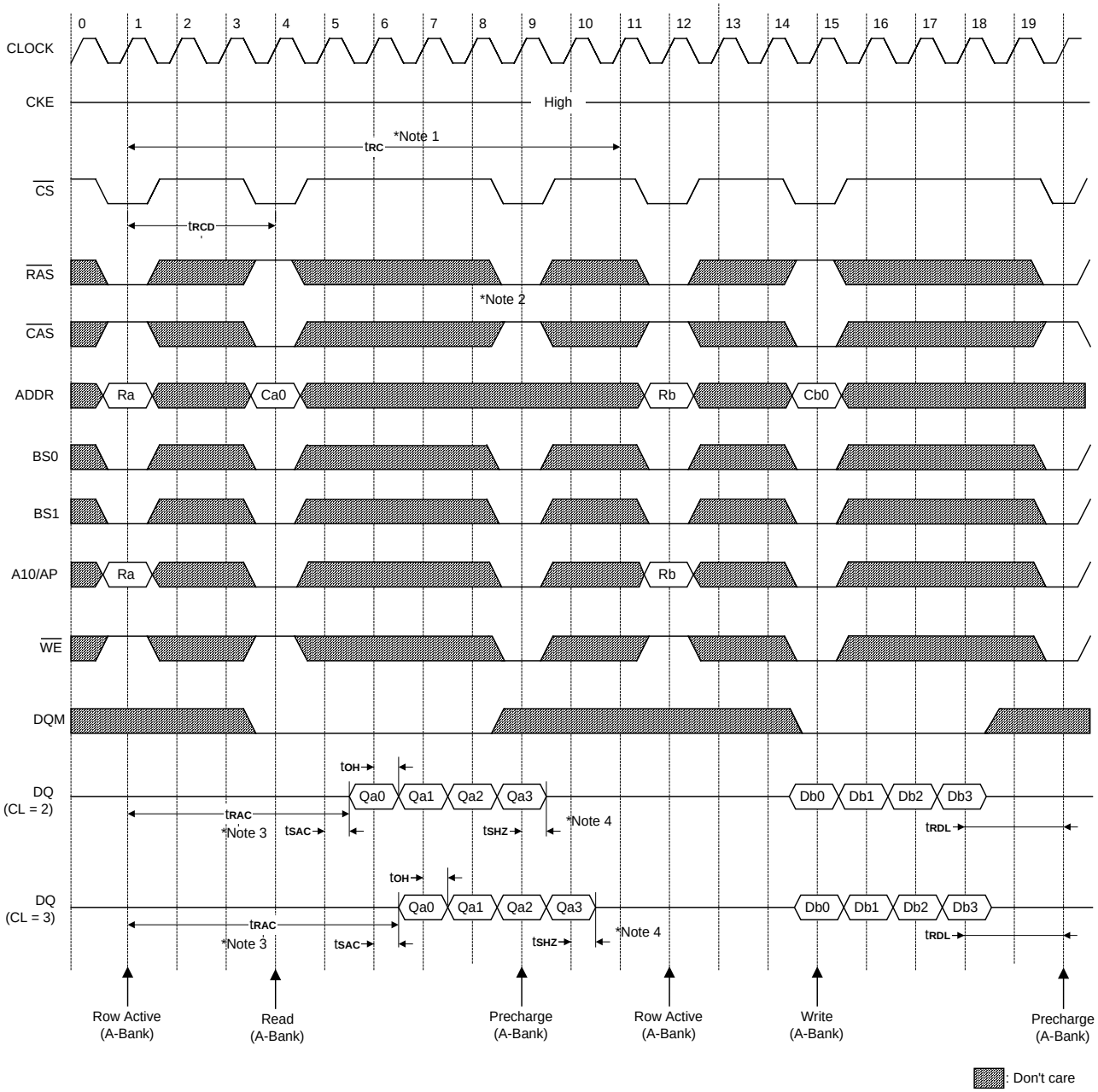
3. Enable and disable auto precharge function are controlled by A10/AP in read/write command.

A10/AP	BS1	BS0	Operation
0	0	0	Disable auto precharge, leave bank A active at end of burst.
	0	1	Disable auto precharge, leave bank B active at end of burst.
	1	0	Disable auto precharge, leave bank C active at end of burst.
	1	1	Disable auto precharge, leave bank D active at end of burst.
1	0	0	Enable auto precharge, precharge bank A at end of burst.
	0	1	Enable auto precharge, precharge bank B at end of burst.
	1	0	Enable auto precharge, precharge bank C at end of burst.
	1	1	Enable auto precharge, precharge bank D at end of burst.

4. A10/AP and BS0, BS1 control bank precharge when precharge command is asserted.

A10/AP	BS1	BS0	Precharge
0	0	0	Bank A
0	0	1	Bank B
0	1	0	Bank C
0	1	1	Bank D
1	X	X	All Banks

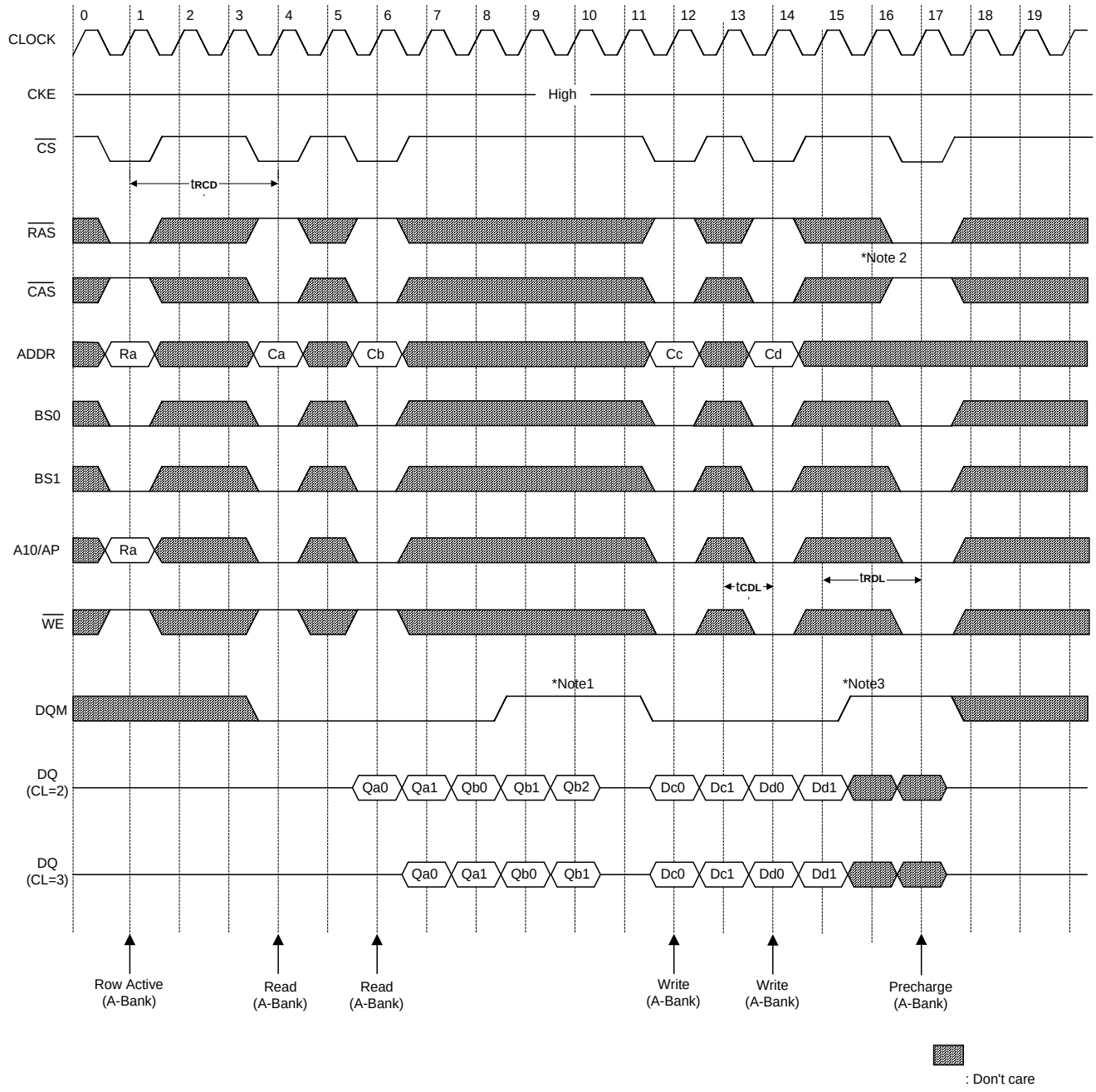
Read & Write Cycle at Same Bank @Burst Length=4



***Note :** 1. Minimum row cycle times is required to complete internal DRAM operation.

2. Row precharge can interrupt burst on any cycle. [CAS latency-1] valid output data available after Row enters precharge. Last valid output will be Hi-Z after t_{SHZ} from the clock.
3. Access time from Row address. t_{CC}*(t_{RCD} + CAS latency-1) + t_{SAC}
4. Output will be Hi-Z after the end of burst. (1,2,4 & 8)

Page Read & Write Cycle at Same Bank @Burst Length=4

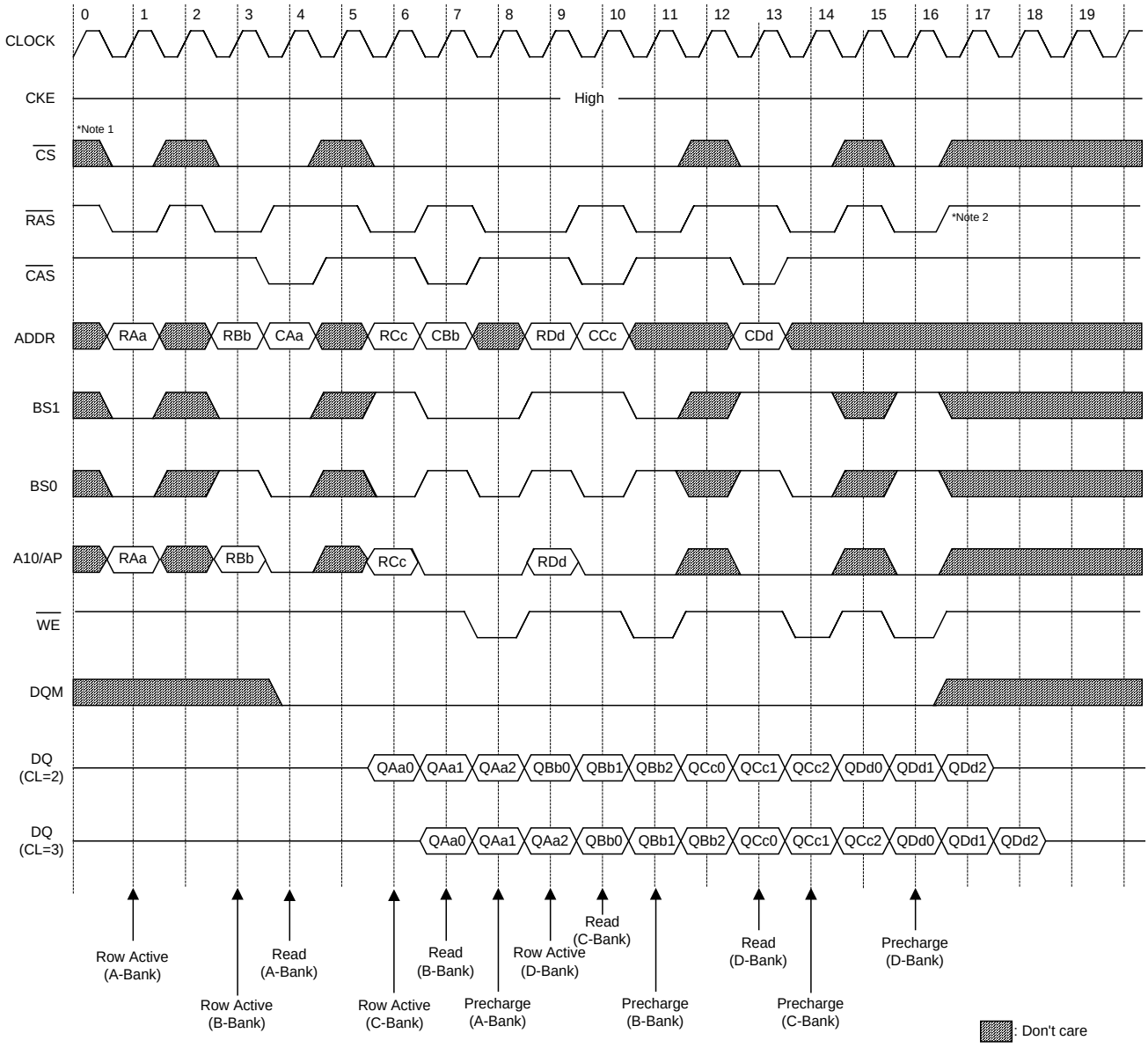


***Note :** 1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.

2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.

3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

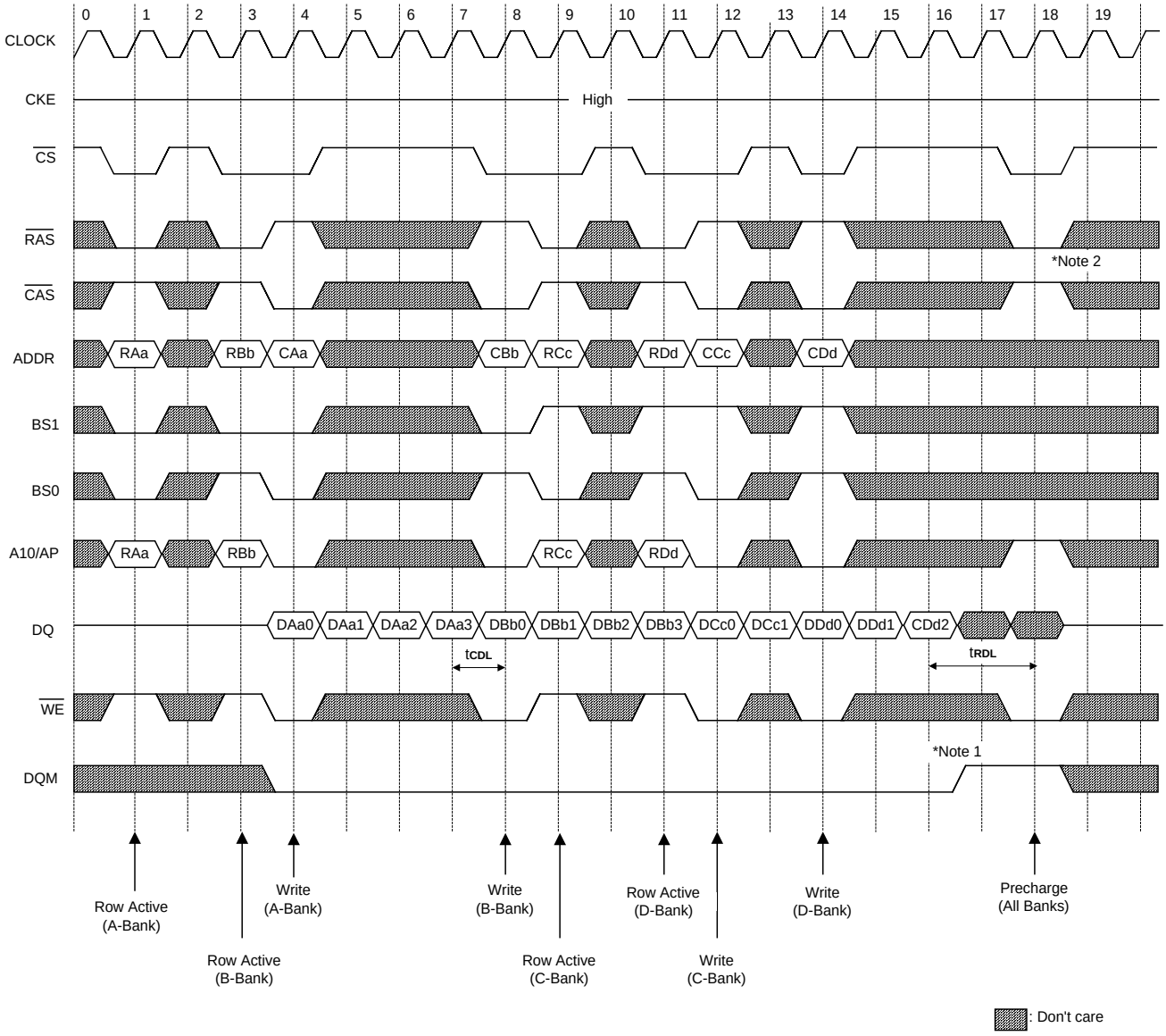
Page Read Cycle at Different Bank @Burst Length = 4



* Note : 1. $\overline{CS}$ can be don't care when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going edge.

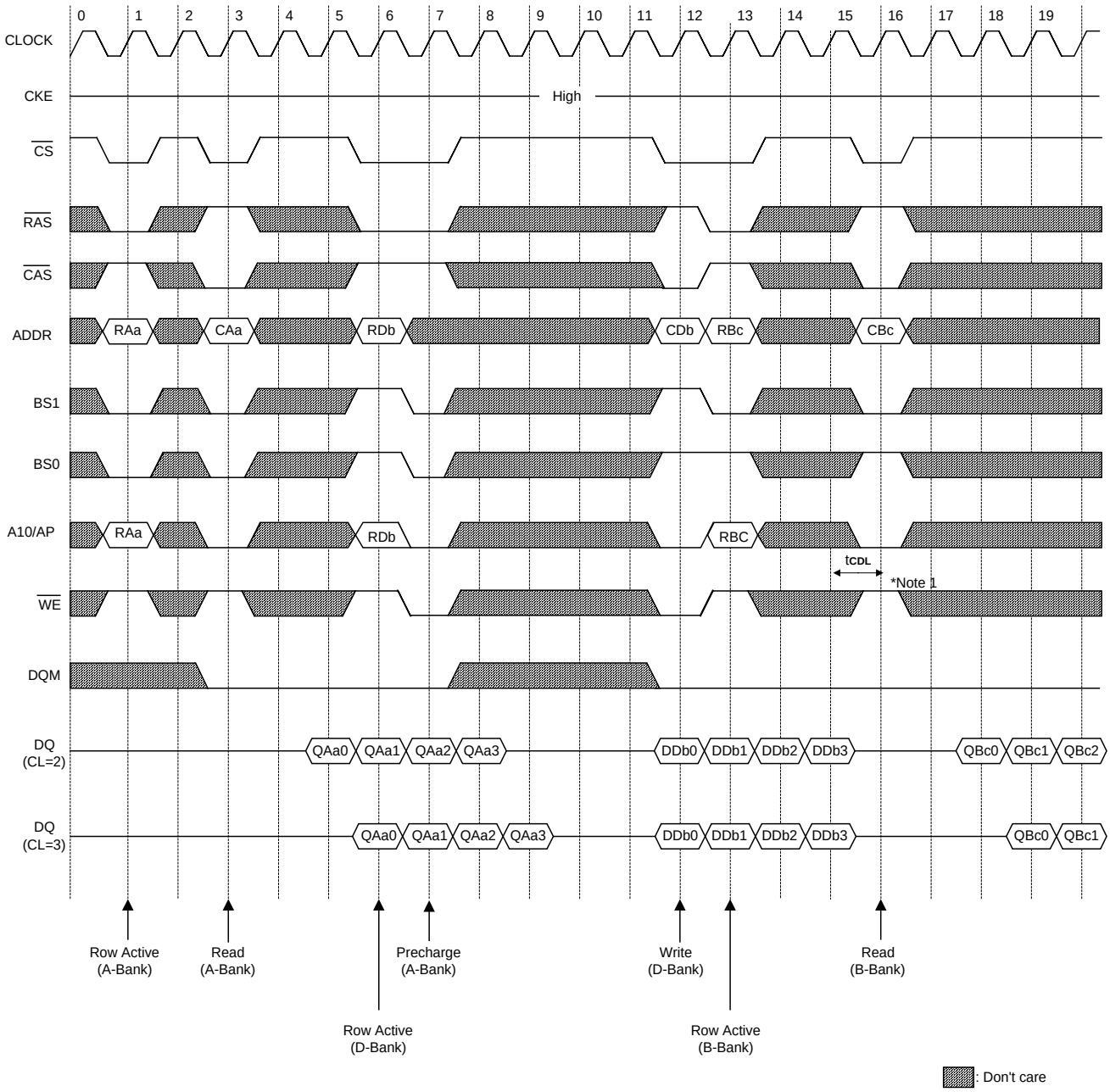
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4



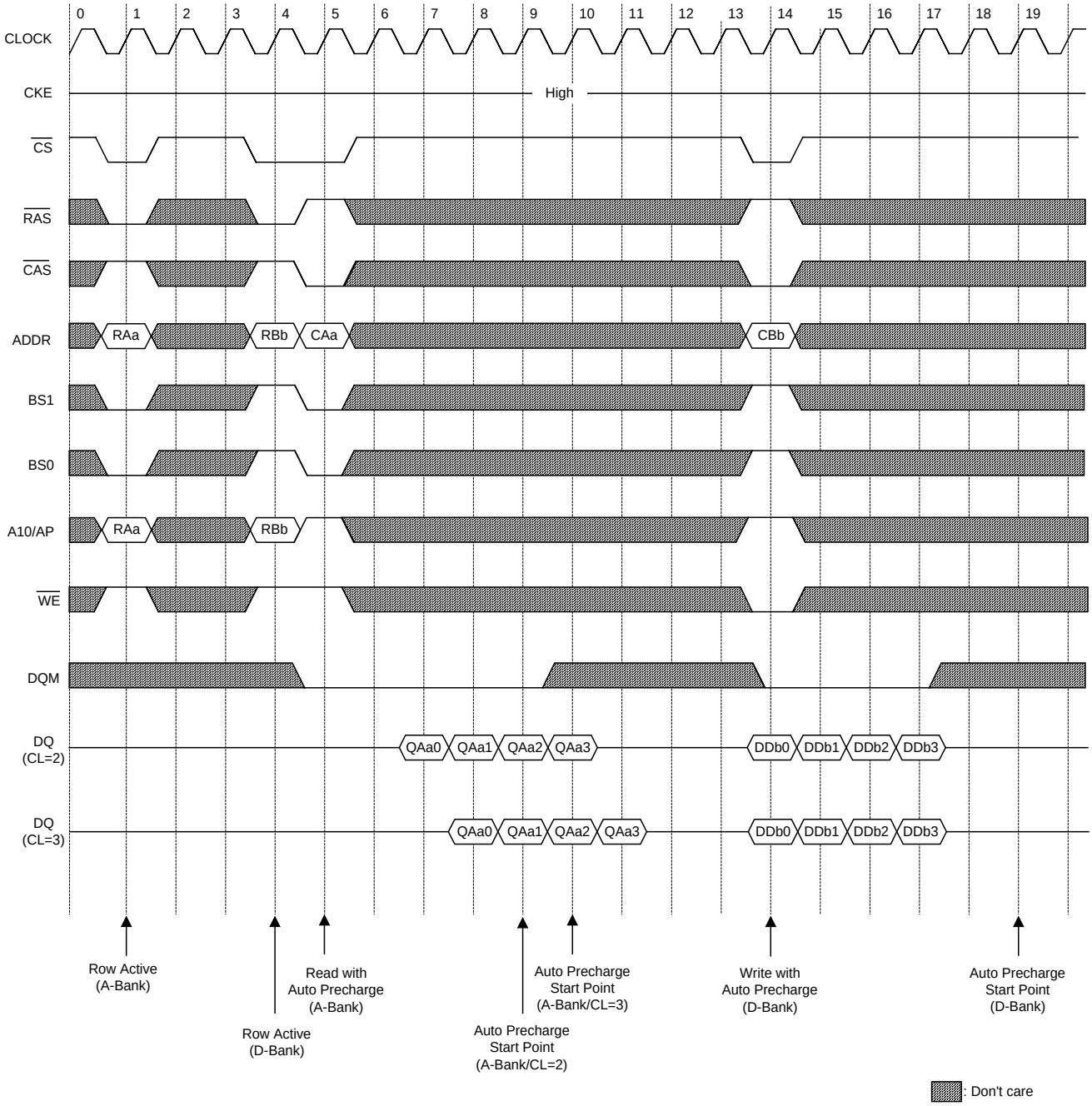
* Note:
1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and precharge banks must be the same.

Read & Write Cycle at Different Bank @Burst Length=4



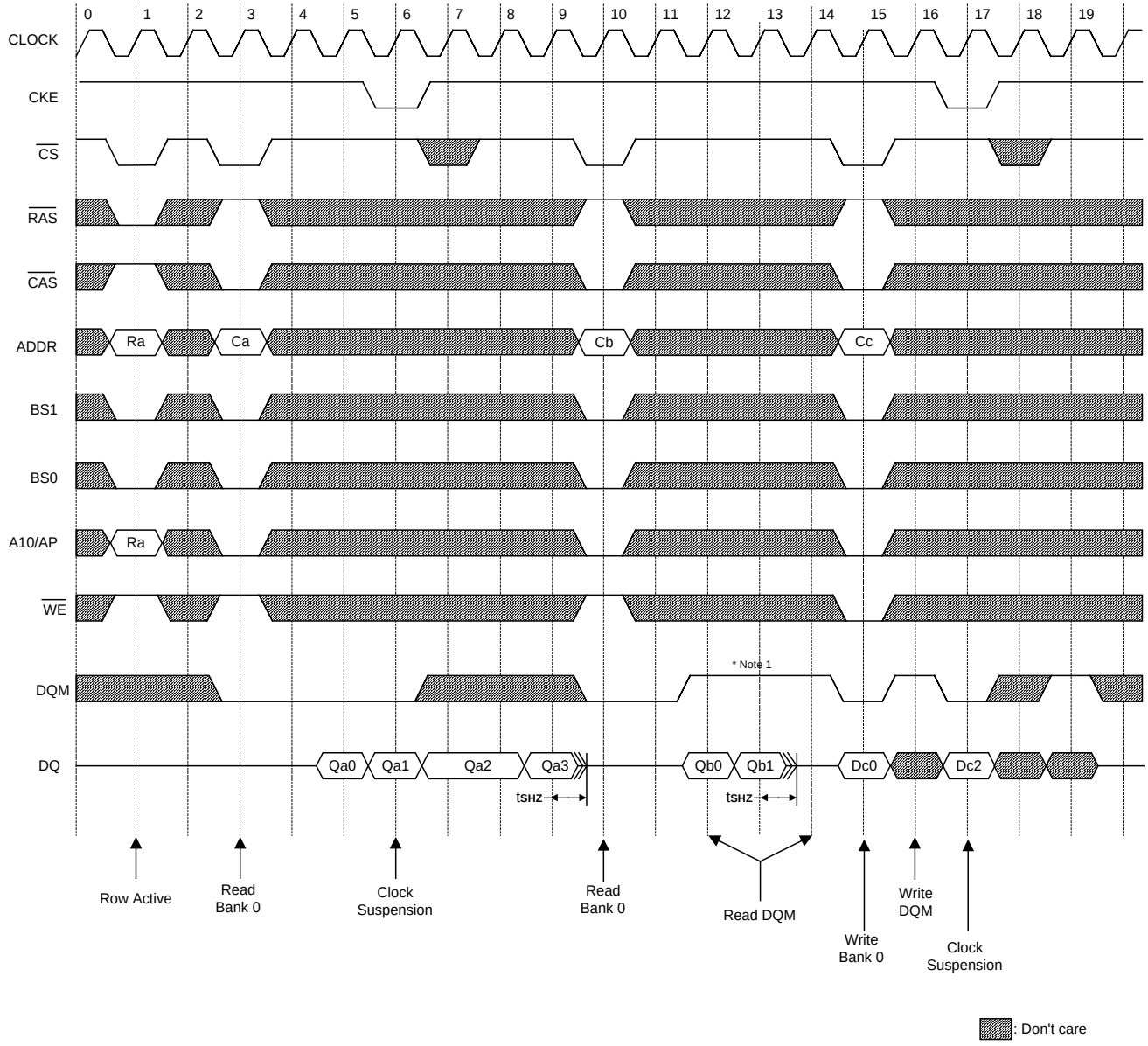
* Note : t_{CDL} should be met to complete write.

Read & Write Cycle with Auto Precharge @Burst Length=4



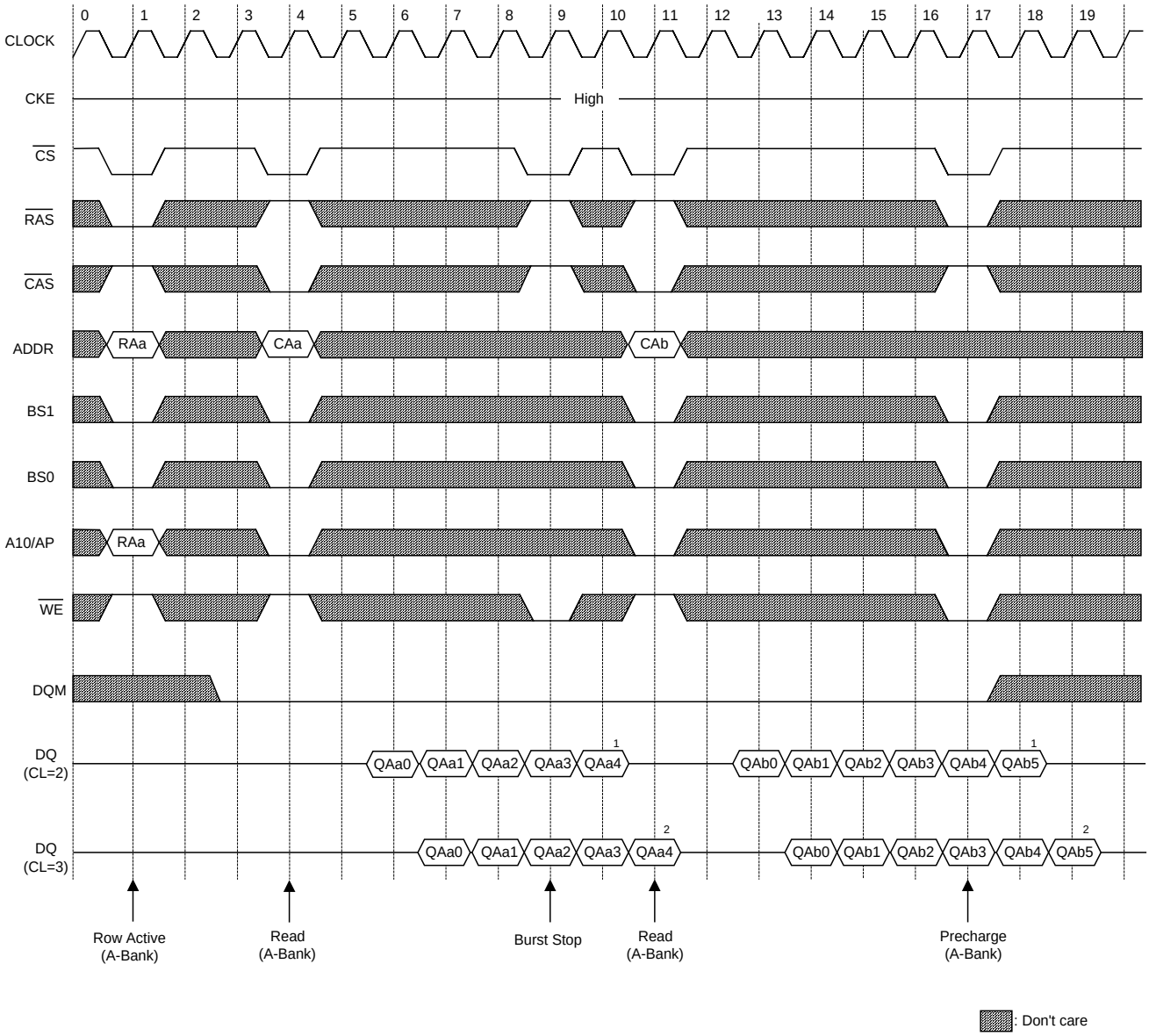
*Note : tRCD should be controlled to meet minimum tRAS before internal precharge start.
(In the case of Burst Length=1 & 2, BRSW mode)

Clock Suspension & DQM Operation Cycle @CAS Latency = 2, Burst Length=4



* Note : DQM needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @Burst Length=Full Page

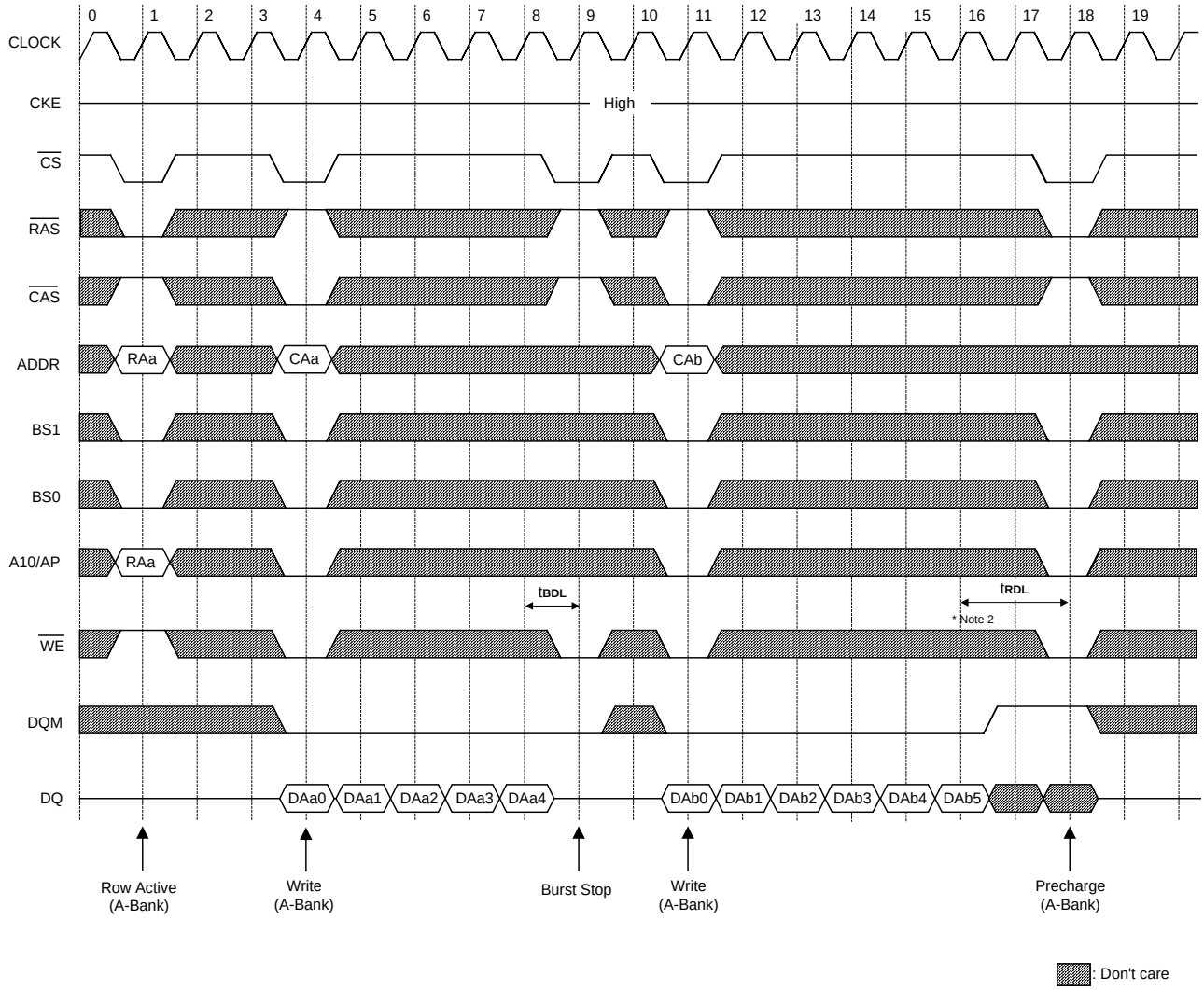


* Note : 1. At full page mode, burst is wrap-around at the end of burst. So auto precharge is impossible.

2. About the valid DQ's after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
   Both cases are illustrated above timing diagram. See the label 1,2 on them.
   But at burst write, burst stop and $\overline{RAS}$ interrupt should be compared carefully.
   Refer the timing diagram of "Full page write burst stop cycle".

3. Burst stop is valid at every burst length.

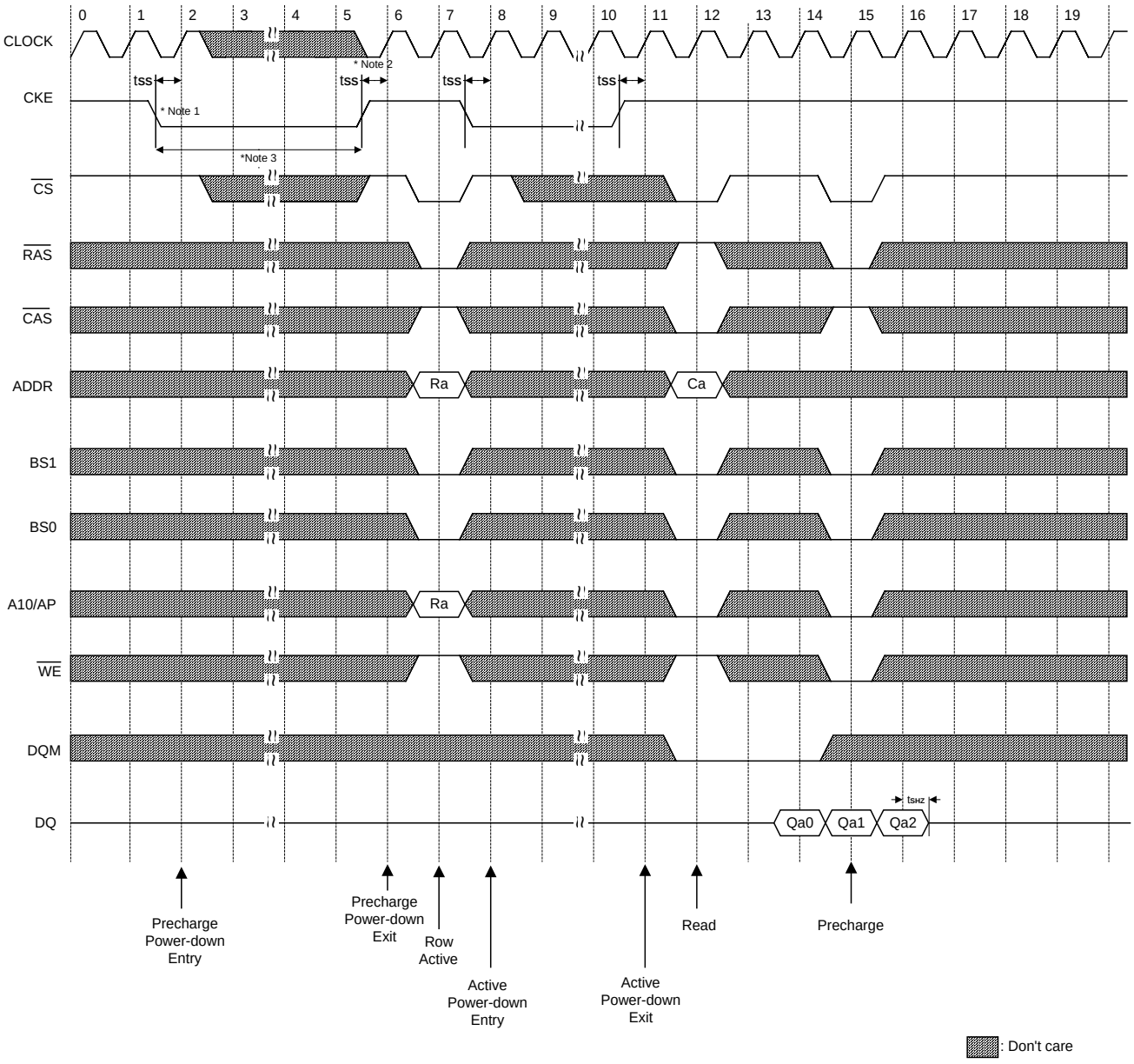
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Burst Length = Full Page



* Note : 1. At full page mode, burst is wrap-around at the end of burst. So auto precharge is impossible.

2. Data-in at the cycle of interrupted by precharge cannot be written into the corresponding memory cell.
   It is defined by AC parameter of t_{RDL}(=2CLK).
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst.
   Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

Active/Precharge Power Down Mode @CAS Lantency=2, Burst Length=4

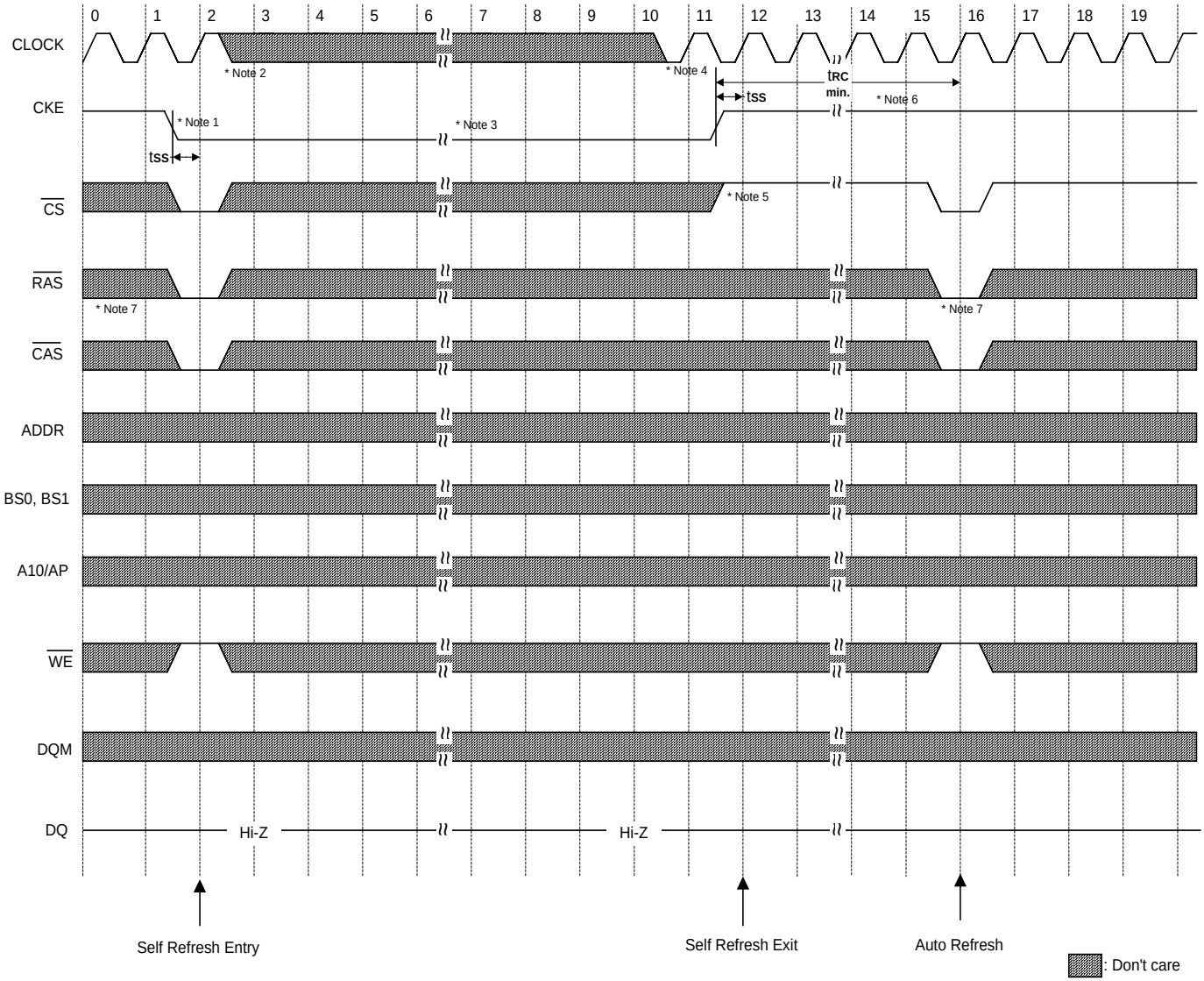


* Note : 1. All banks should be in idle state prior to entering precharge power down mode.

2. CKE should be set high at least “1CLK + tss” prior to Row active command.

3. Cannot violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



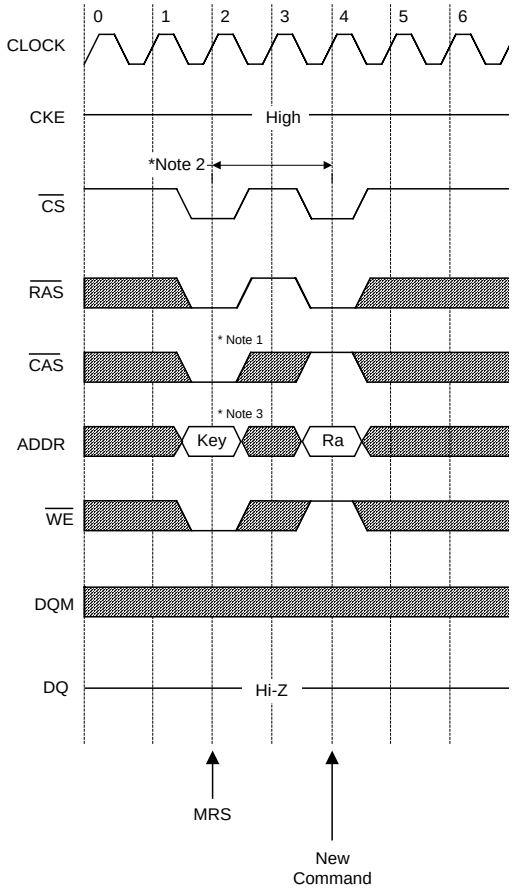
*** Note : TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ and CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   (cf.) Once the device enters self refresh mode, minimum tRAS is required before exit from self refresh.

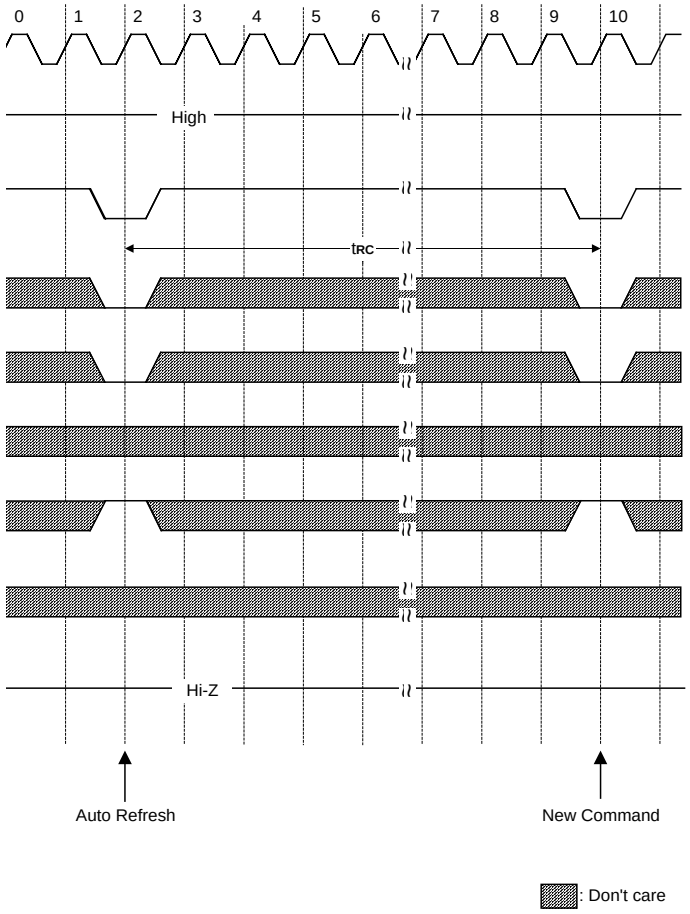
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum tRC is required after CKE going high to complete self refresh exit.
7. 4K cycle of burst auto refresh is required before self refresh entry and after self refresh exit.
   If the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



* All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

* Note : 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.

2. Minimum 2 clock cycles is required before new $\overline{RAS}$ activation.

3. Please refer to Mode Register Set table.

Function Truth Table (Table 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	Address	Action	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row Active; Latch Row Address	
	L	L	H	L	BA	A10/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP Code		Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA,A10/AP	Begin Read; Latch CA; Determine AP	
	L	H	L	L	BA	CA,A10/AP	Begin Write; Latch CA; Determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	PA	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP(Continue Burst to End →Row Active)	
	L	H	H	H	X	X	NOP(Continue Burst to End →Row Active)	
	L	H	H	L	X	X	Term burst →Row Active	
	L	H	L	H	BA	CA,A10/AP	Term burst; Begin Read; Latch CA; Determine AP	3
	L	H	L	L	BA	CA,A10/AP	Term burst; Begin Write; Latch CA; Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term Burst; Precharge timing for Reads	3
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP(Continue Burst to End→Row Active)	
	L	H	H	H	X	X	NOP(Continue Burst to End→Row Active)	
	L	H	H	L	X	X	Term burst →Row Active	
	L	H	L	H	BA	CA,A10/AP	Term burst; Begin Read; Latch CA; Determine AP	3
	L	H	L	L	BA	CA,A10/AP	Term burst; Begin Write; Latch CA; Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term Burst; Precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP(Continue Burst to End→Precharge)	
	L	H	H	H	X	X	NOP(Continue Burst to End→Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	BA	CA,A10/AP	ILLEGAL	2
	L	H	L	L	BA	CA,A10/AP	ILLEGAL	2
	L	L	H	X	BA	RA, PA	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	2

Function Truth Table (Table 1, Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS	Address	Action	Note
Write with Auto Precharge	H	X	X	X	X	X	NOP(Continue Burst to End→Precharge)	
	L	H	H	H	X	X	NOP(Continue Burst to End→Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	BS	CA,A10/AP	ILLEGAL	2
	L	H	L	L	BS	CA,A10/AP	ILLEGAL	2
	L	L	H	X	BS	RA, PA	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	2
Precharge	H	X	X	X	X	X	NOP→Idle after t_{RP}	
	L	H	H	H	X	X	NOP→Idle after t_{RP}	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BS	CA,A10/AP	ILLEGAL	2
	L	L	H	H	BS	RA	ILLEGAL	2
	L	L	H	L	BS	A10/AP	NOP→Idle after t_{RP}	2
	L	L	L	X	X	X	ILLEGAL	4
Row Activating	H	X	X	X	X	X	NOP→Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP→Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BS	CA,A10/AP	ILLEGAL	2
	L	L	H	H	BS	RA	ILLEGAL	2
	L	L	H	L	BS	A10/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	2
Refreshing	H	X	X	X	X	X	NOP→Idle after t_{RC}	
	L	H	H	X	X	X	NOP→Idle after t_{RC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP→Idle after 2 clocks	
	L	H	H	H	H	X	NOP→Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations

RA = Row Address BS = Bank Address AP = Auto Precharge

NOP = No Operation Command CA = Column Address PA = Precharge All

Note: 1. All entries assume that CKE was active (High) during the preceding clock cycle and the current clock cycle.

2. Illegal to bank in specified state: Function may be legal in the bank indicated by BA, depending on the state of that bank.

3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.

4. NOP to bank precharging or in idle state. May precharge bank indicated by BS (and PA).

5. Illegal if any banks is not idle.

Function Truth Table for CKE (Table 2)

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh→ABI after t_{RC}	6
	L	H	L	H	H	H	X	Exit Self Refresh→ABI after t_{RC}	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP(Maintain Self Refresh)	
Both Bank Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down→ABI	7
	L	H	L	H	H	H	X	Exit Power Down→ABI	7
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP(Maintain Power Down Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	8
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	L	H	X	Enter Self Refresh	8
	H	L	L	L	L	L	OPCODE	MRS	
	L	L	X	X	X	X	X	NOP	
Any State Other than Listed Above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain clock Suspend	

Abbreviations : ABI = All Banks Idle

Note: 6. After CKE's low to high transition to exit self refresh mode, a minimum of t_{RC}(min) has to be elapse before issuing a new command.

7. CKE low to high transition is asynchronous as if it restarts internal clock.
A minimum setup time "tSS + one clock" must be satisfied before any command can be issued other than exit.

8. Power-down and self refresh can be entered only when all the banks are in idle state.

9. Must be a legal command.

Ordering Information

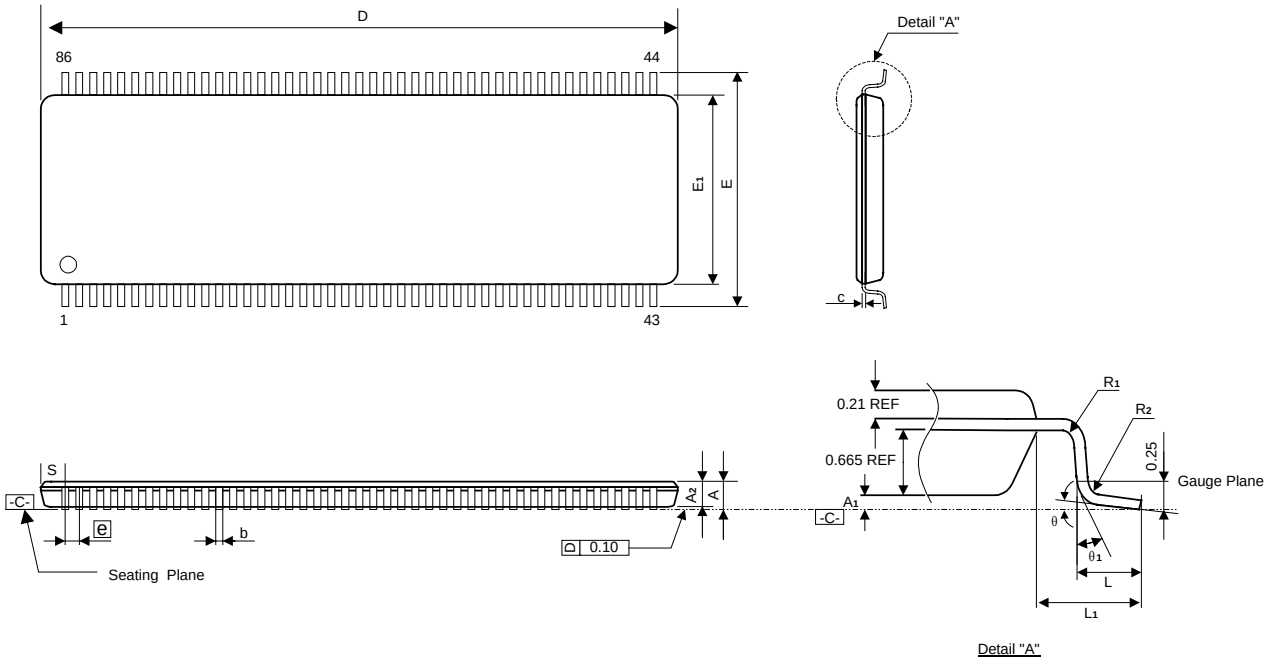
Part No.	Min. Cycle Time (ns)	Max. Clock Frequency (MHz)	Access Time	Package
A43L1632V-6	6	166	5.5 ns	86 TSOP (II)
A43L1632V-7	7	143	5.5 ns	86 TSOP (II)

Note: -U is for industrial operating temperature range -40ºC to +85ºC.

Package Information

TSOP 86L (Type II) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	-	0.011	0.17	-	0.27
c	0.005	-	0.008	0.12	-	0.21
D	0.875 BSC			22.22 BSC		
S	0.024 REF			0.61 REF		
E	0.463 BSC			11.76 BSC		
E1	0.400 BSC			10.16 BSC		
e	0.020 BSC			0.50 BSC		
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	0.031 REF			0.80 REF		
R1	0.005	-	-	0.12	-	-
R2	0.005	-	0.010	0.12	-	0.25
θ	0°	-	8°	0°	-	8°
θ1	0°	-	-	0°	-	-

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.