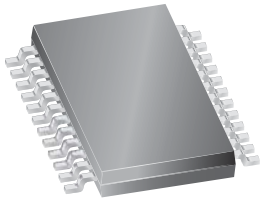
Microstepping DMOS Driver with Translator

Features and Benefits

- ±2.5 A, 35 V output rating
- Low $R_{DS(On)}$ outputs: 0.28 Ω source, 0.22 Ω sink, typical
- Automatic current decay mode detection/selection
- 3.0 to 5.5 V logic supply voltage range
- Slow, Fast or Mixed current decay modes
- Home output
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Crossover-current protection

Package: 28 lead TSSOP (suffix LP) with exposed thermal pad



Not to scale

Description

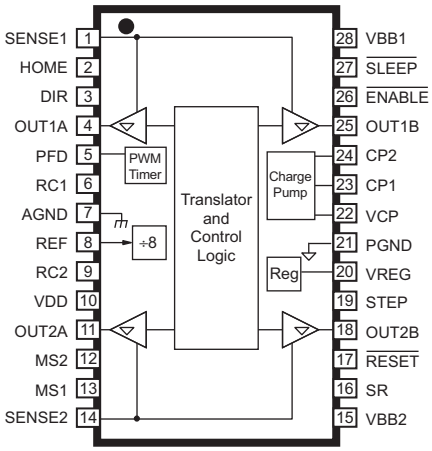
The A3979 is a complete microstepping motor driver with built-in translator, designed as a pin-compatible replacement for the successful A3977, with enhanced microstepping (1/16 step) precision. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and sixteenth-step modes, with an output drive capacity of up to 35 V and ±2.5 A. The A3979 includes a fixed off-time current regulator that has the ability to operate in Slow, Fast, or Mixed decay modes. This current-decay control scheme results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

The translator is the key to the easy implementation of the A3979. It allows the simple input of one pulse on the STEP pin to drive the motor one microstep, which can be either a full step, half, quarter, or sixteenth, depending on the setting of the MS1 and MS2 logic inputs. There are no phase-sequence tables, high-frequency control lines, or complex interfaces to program. The A3979 interface is an ideal fit for applications where a complex microprocessor is unavailable or is overburdened.

Internal synchronous-rectification control circuitry is provided to improve power dissipation during PWM operation. Internal circuit protection includes: thermal shutdown with hysteresis, UVLO (undervoltage lockout), and crossover-current protection. Special power-on sequencing is not required.

The A3979 is supplied in a low-profile (height ≤1.20 mm), 28-pin TSSOP with exposed thermal pad. The package is lead (Pb) free, with 100% matte tin leadframe plating.

Pin-out Diagram



AGND and PGND must be connected together externally

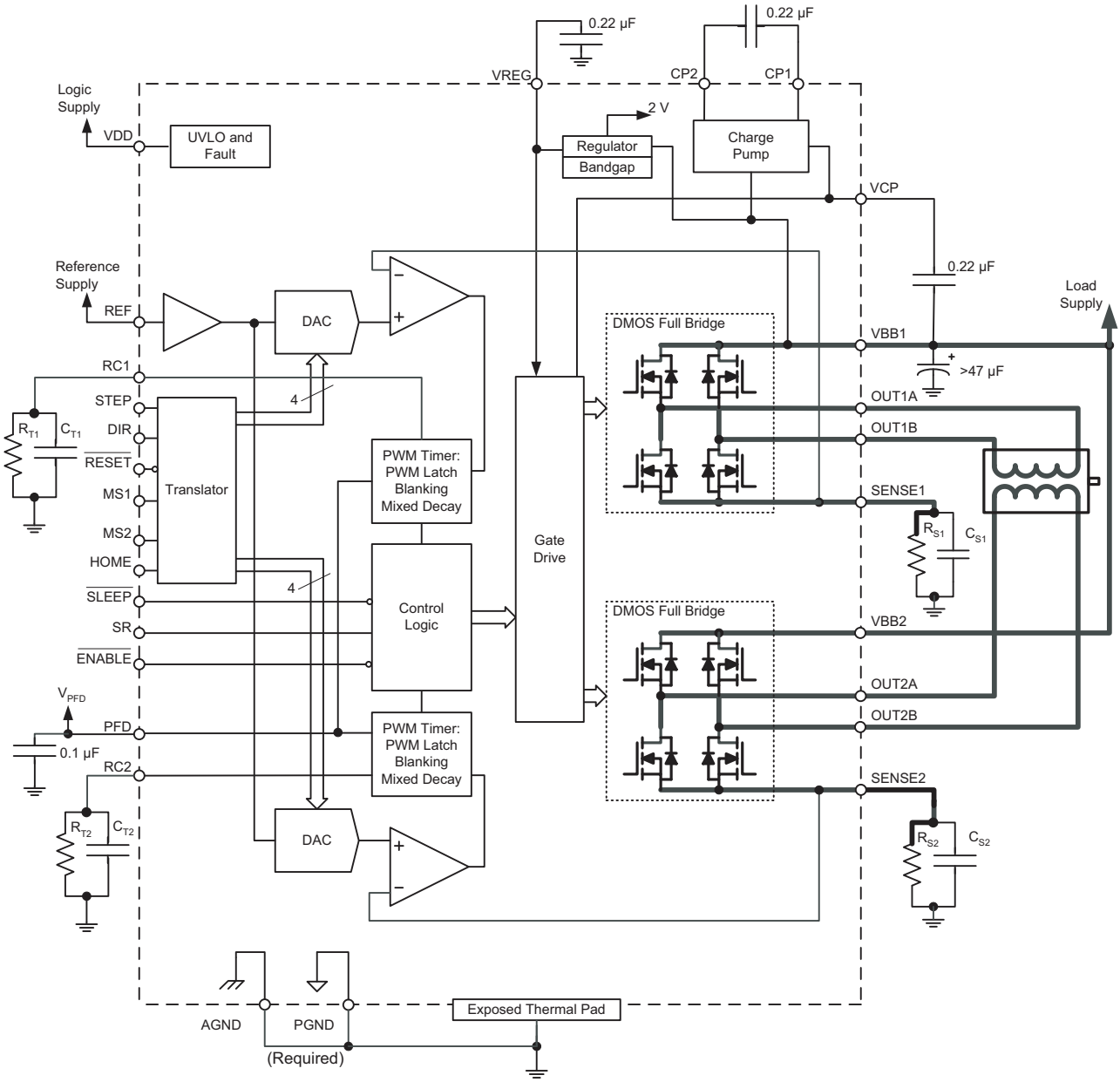
Selection Guide

Part Number	Packing
A3979SLPTR-T	4000 pieces per reel

Absolute Maximum Ratings

Load Supply Voltage	V_{BB}		35	V
Output Current	I_{OUT}	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	±2.5	A
Logic Supply Voltage	V_{DD}		7.0	V
Logic Input Voltage Range	V_{IN}	t_W > 30 ns	–0.3 to V_{DD} + 0.3	V
		t_W < 30 ns	–1 to V_{DD} + 1	V
Sense Voltage	V_{SENSE}		0.5	V
Reference Voltage	V_{REF}		V_{DD}	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

Functional Block Diagram



ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 35 V, V_{DD} = 3.0 to 5.5 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	8	–	35	V
		During Sleep mode	0	–	35	V
Output Leakage Current[2]	I_{DSS}	$V_{OUT} = V_{BB}$	–	<1.0	20	µA
		V_{OUT} = 0 V	–	<1.0	–20	µA
Output On Resistance	$R_{DS(On)}$	Source driver, I_{OUT} = –2.5 A	–	0.28	0.335	Ω
		Sink driver, I_{OUT} = 2.5 A	–	0.22	0.265	Ω
Body Diode Forward Voltage	V_F	Source diode, I_F = –2.5 A	–	–	1.4	V
		Sink diode, I_F = 2.5 A	–	–	1.4	V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	–	8.0	mA
		Operating, outputs disabled	–	–	6.0	mA
		Sleep mode	–	–	20	µA
Control Logic						
Logic Supply Voltage Range	V_{DD}	Operating	3.0	5.0	5.5	V
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz	–	–	12	mA
		Outputs off	–	–	10	mA
		Sleep mode	–	–	20	µA
Logic Input Voltage	$V_{IN(1)}$		0.7×V_{DD}	–	–	V
	$V_{IN(0)}$		–	–	0.3×V_{DD}	V
Logic Input Current[2]	$I_{IN(1)}$	V_{IN} = 0.7×V_{DD}	–20	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.3×V_{DD}	–20	<1.0	20	µA
Reference Input Voltage Range	V_{REF}	Operating	0	–	V_{DD}	V
Reference Input Current	I_{REF}		–	0	±3	µA
HOME Output Voltage	$V_{HOME(1)}$	$I_{HOME(1)}$ = –200 µA	0.7×V_{DD}	–	–	V
	$V_{HOME(0)}$	$I_{HOME(0)}$ = 200 µA	–	–	0.3×V_{DD}	V
Mixed Decay Mode Trip Point	V_{PFDH}		–	0.6×V_{DD}	–	V
	V_{PFDL}		–	0.21×V_{DD}	–	V
Gain (G_m) Error[3]	E_G	V_{REF} = 2 V, Phase Current = 38.27%	–	–	±10	%
		V_{REF} = 2 V, Phase Current = 70.71%	–	–	±5.0	%
		V_{REF} = 2 V, Phase Current = 100.00%	–	–	±5.0	%
STEP Pulse Width	t_W		1	–	–	µs
Blank Time	t_{BLANK}	R_T = 56 kΩ, C_T = 680 pF	700	950	1200	ns
Fixed Off-Time	t_{OFF}	R_T = 56 kΩ, C_T = 680 pF	30	38	46	µs
Crossover Dead Time	t_{DT}	Synchronous rectification enabled	100	475	800	ns

Continued on the next page...

ELECTRICAL CHARACTERISTICS, continued at T_A = 25°C, V_{BB} = 35 V, V_{DD} = 3.0 to 5.5 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
Thermal Shutdown Temperature	T_{JSD}		–	165	–	°C
Thermal Shutdown Hysteresis	T_{JSDHYS}		–	15	–	°C
UVLO Enable Threshold	V_{UVLO}	Increasing V_{DD}	2.45	2.7	2.95	V
UVLO Hysteresis	$V_{UVLOHYS}$		0.05	0.10	–	V

[1]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

[2]Negative current is defined as coming out of (sourcing from) the specified device pin.

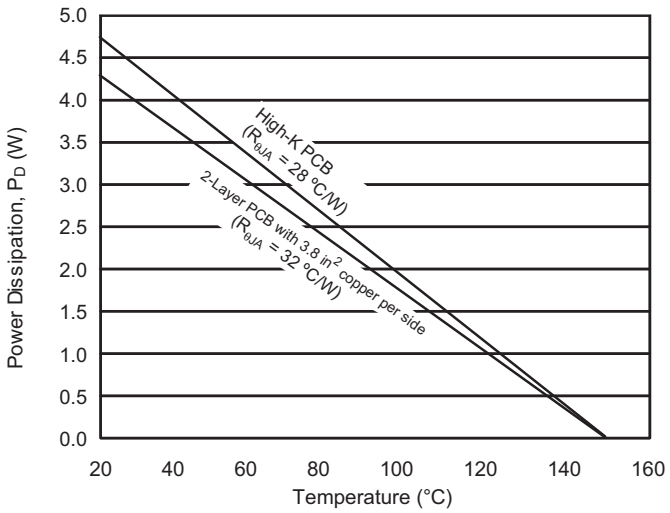
[3]$E_G = ([V_{REF}/8] - V_{SENSE})/(V_{REF}/8)$.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

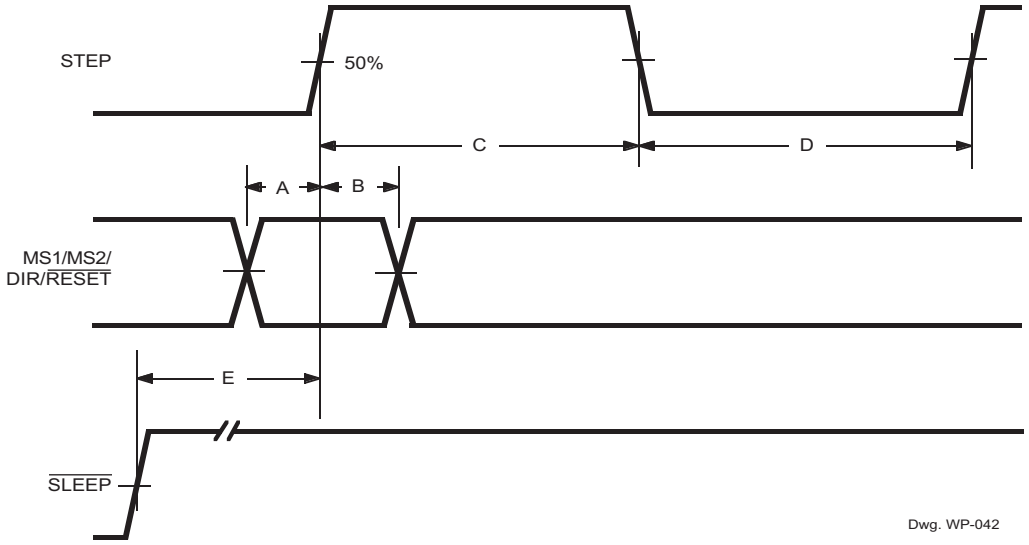
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Two-layer PCB with 3.8 in.^{2} of copper area on each side connected with thermal vias and to device exposed pad	32	ºC/W
		High-K PCB (multilayer with significant copper areas, based on JEDEC standard)	28	ºC/W

*Additional thermal information available on Allegro Web site.

Maximum Power Dissipation, $P_{D(max)}$



Timing Requirements
(T_A = +25°C, V_{DD} = 5 V, Logic Levels are V_{DD} and Ground)



A. Minimum Command Active Time
Before Step Pulse (Data Set-Up Time) ..... 200 ns

B. Minimum Command Active Time
After Step Pulse (Data Hold Time) ..... 200 ns

C. Minimum STEP Pulse Width ..... 1.0 µs

D. Minimum STEP Low Time ..... 1.0 µs

E. Maximum Wake-Up Time ..... 1.0 ms

Figure 1. Logic Interface Timing Diagram

Table 1. Microstep Resolution Truth Table

MS1	MS2	Microstep Resolution	Excitation Mode
L	L	Full Step	2 Phase
H	L	Half Step	1-2 Phase
L	H	Quarter Step	W1-2 Phase
H	H	Sixteenth Step	4W1-2 Phase

Functional Description

Device Operation. The A3979 is a complete microstepping motor driver with a built-in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and sixteenth-step modes. The currents in each of the two output full-bridges (all of the N-channel MOSFETs) are regulated with fixed off-time PMW (pulse width modulated) control circuitry. At each step, the current for each full-bridge is set by the value of its external current-sense resistor (R_{S1} or R_{S2}), a reference voltage (V_{REF}), and the output voltage of its DAC (which in turn is controlled by the output of the translator).

At power-on or reset, the translator sets the DACs and the phase current polarity to the initial Home state (shown in figures 2 through 5), and the current regulator to Mixed decay mode for both phases. When a step command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level and current polarity. (See table 2 for the current-level sequence.) The microstep resolution is set by the combined effect of inputs MS1 and MS2, as shown in table 1.

While stepping is occurring, if the next output level of the DACs is lower than the immediately preceeding output level, then the decay mode (Fast, Slow, or Mixed) for the active full bridge is set by the PFD input. If the next DAC output level is higher than or equal to the preceeding level, then the decay mode for that full bridge will be Slow decay. This automatic current-decay selection improves microstepping performance by reducing the distortion of the current waveform due to back EMF of the motor.

RESET Input ($\overline{\text{RESET}}$). The $\overline{\text{RESET}}$ input (active low) sets the translator to a predefined Home state (shown in figures 2 through 5), and turns off all of the DMOS outputs. The HOME output goes low and all STEP inputs are ignored until the $\overline{\text{RESET}}$ input is set to high.

Home Output (HOME). The HOME output is a logic output indicator of the initial state of the translator. At power-on, the translator is reset to the Home state (shown in figures 2 through 5).

Step Input (STEP). A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the combined state of inputs MS1 and MS2 (see table 1).

Microstep Select (MS1 and MS2). The input on terminals MS1 and MS2 selects the microstepping format, as shown in table 1. Any changes made to these inputs do not take effect until the next rising edge of a step command signal on the STEP input.

Direction Input (DIR). The state of the DIR input determines the direction of rotation of the motor. Any changes made to this input does not take effect until the next rising edge of a step command signal on the STEP input.

Internal PWM Current Control. Each full bridge is controlled by a fixed–off-time PWM current-control circuit that limits the load current to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink MOS outputs are enabled and current flows through the motor winding and the current sense resistor, R_{Sx}. When the voltage across R_{Sx} equals the DAC output voltage, the current-sense comparator resets the PWM latch. The latch then turns off either the source MOSFETs (when in Slow decay mode) or the sink and source MOSFETs (when in Fast or Mixed decay mode).

The maximum value of current limiting is set by the selection of R_S and the voltage at the V_{REF} input with a transconductance function approximated by:

$$I_{TRIP}max = V_{REF}/8R_S$$

The DAC output reduces the V_{REF} output to the current-sense comparator in precise steps (see table 2 for % I_{TRIP}max at each step).

$$I_{TRIP} = (\%\ I_{TRIP}max/100)\ I_{TRIP}max$$

It is critical that the maximum rating (0.5 V) on either the SENSE1 and SENSE2 pins is not exceeded. For full stepping, V_{REF} can be applied up to the maximum rating of V_{DD} because the peak sense value is $0.707 \times V_{REF}/8$. In all other modes, V_{REF} should not exceed 4 V.

Fixed Off-Time. The internal PWM current-control circuitry uses a one-shot timer to control the duration of time that the MOSFETs remain off. The one shot off-time, t_{OFF}, is determined by the selection of external resistors, R_{Tx}, and capacitors, C_{Tx}, connected from each R_{Cx} timing terminal to ground. The off-time, over a range of values of C_T = 470 pF to 1500 pF and R_T = 12 kΩ to 100 kΩ is approximated by:

$$t_{OFF} = R_T C_T$$

RC Blanking. In addition to the fixed off-time of the PWM control circuit, the CTx component sets the comparator blanking time. This function blanks the output of the current-sense comparators when the outputs are switched by the internal current-control circuitry. The comparator outputs are blanked to prevent false overcurrent detection due to reverse recovery currents of the clamp diodes, or to switching transients related to the capacitance of the load. The blank time t_{BLANK} can be approximated by:

$$t_{BLANK} = 1400 C_T$$

Charge Pump (CP1 and CP2). The charge pump is used to generate a gate supply greater than that of VBB for driving the source-side DMOS gates. A 0.22 µF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. In addition, a 0.22 µF ceramic capacitor is required between VCP and VBB, to act as a reservoir for operating the high-side DMOS gates.

V_{REG} (VREG). This internally-generated voltage is used to operate the sink-side DMOS outputs. The VREG pin must be decoupled with a 0.22 µF capacitor to ground. V_{REG} is internally monitored, and in the case of a fault condition, the DMOS outputs of the device are disabled.

Enable Input ($\overline{\text{ENABLE}}$). This active-low input enables all of the DMOS outputs. When set to a logic high, the outputs are disabled. The inputs to the translator (STEP, DIR, MS1, and MS2), all remain active, independent of the $\overline{\text{ENABLE}}$ input state.

Shutdown. During normal operation, in the event of a fault, such as overtemperature (excess T_J) or an undervoltage on VCP, the outputs of the device are disabled until the fault condition is removed.

At power up, and in the event of low V_{DD}, the undervoltage lockout (UVLO) circuit disables the drivers and resets the translator to the Home state.

Sleep Mode ($\overline{\text{SLEEP}}$). This active-low control input is used to minimize power consumption when the motor is not in use. It disables much of the internal circuitry including the output DMOS FETs, current regulator, and charge pump. Setting this to a logic high allows normal operation, as well as start-up (at which time the A3979 drives the motor to the Home microstep position). When bringing the device out of Sleep mode, in order to allow the charge pump (gate drive) to stabilize, provide a delay of 1 ms before issuing a step command signal on the STEP input.

Percent Fast Decay Input (PFD). When a STEP input signal commands a lower output current than the previous step, it switches the output current decay to either Slow, Fast, or Mixed decay mode, depending on the voltage level at the PFD input. If the voltage at the PFD input is greater than $0.6 \times V_{DD}$, then Slow decay mode is selected. If the voltage on the PFD input is less than $0.21 \times V_{DD}$, then Fast decay mode is selected. Mixed decay mode is selected when V_{PFD} is between these two levels, as described in the next section. This terminal should be decoupled with a 0.1 µF capacitor.

Mixed Decay Operation. If the voltage on the PFD input is between $0.6 \times V_{DD}$ and $0.21 \times V_{DD}$, the bridge operates in Mixed decay mode, as determined by the step sequence (shown in figures 2 through 5). As the trip point is reached, the device goes into Fast decay mode until the voltage on the RCx terminal decays to the same level as voltage applied to the PFD terminal. The time that the device operates in fast decay is approximated by:

$$t_{FD} = R_T C_T \ln (0.6 V_{DD} / V_{PFD})$$

After this Fast decay portion, the device switches to Slow decay mode for the remainder of the fixed off-time period.

Synchronous Rectification. When a PWM off-cycle is triggered by an internal fixed–off-time cycle, load current recirculates according to the decay mode selected by the control logic. The A3979 synchronous rectification feature turns on the appropriate MOSFETs during the decay of the current, and effectively shorts out the body diodes with the low $R_{DS(On)}$ driver. This reduces power dissipation significantly and eliminates the need for external Schottky diodes for most applications. The synchronous rectification can be set to either Active mode or Disabled mode:

- **Active Mode**. When the SR input is logic low, Active mode is enabled and synchronous rectification can occur. This mode prevents reversal of the load current by turning off synchronous rectification when a zero current level is detected. This prevents the motor winding from conducting in the reverse direction.
- **Disabled Mode.** When the SR input is logic high, synchronous rectification is disabled. This mode is typically used when external diodes are required to transfer power dissipation from the A3979 package to the external diodes.

Applications Information

Layout. The printed circuit board on which the device is mounted should have a heavy ground plane. For optimum electrical and thermal performance, the A3979 should be soldered directly onto the board.

The load supply terminals, VBB*x*, should be decoupled with an electrolytic capacitor (>47 µF is recommended), placed as close to the device as possible.

To avoid problems due to capacitive coupling of the high *dv*/*dt* switching transients, route the bridge-output traces away from the sensitive logic-input traces.

Always drive the logic inputs with a low source impedance to increase noise immunity.

Grounding. The AGND (analog ground) terminal and the PGND (power ground) terminal must be connected together externally.

All ground lines should be connected together and be as short as possible. A star ground system, centered under the device, is an optimum design.

The copper ground plane located under the exposed thermal pad is typically used as the star ground.

Current Sensing. To minimize inaccuracies caused by ground-trace IR drops in sensing the output current level, the current-sense resistors, R_{Sx}, should have an independent ground return to the star ground of the device. This path should be as short as possible.

For low-value sense resistors, the IR drops in the printed circuit board sense resistor traces can be significant and should be taken into account.

The use of sockets should be avoided as they can introduce variation in R_{Sx} due to their contact resistance.

Allegro MicroSystems recommends a value of R_S given by

$$R_S = 0.5/I_{TRIP}max$$

Thermal Protection. This internal circuitry turns off all drivers when the junction temperature reaches 165°C, typical. It is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

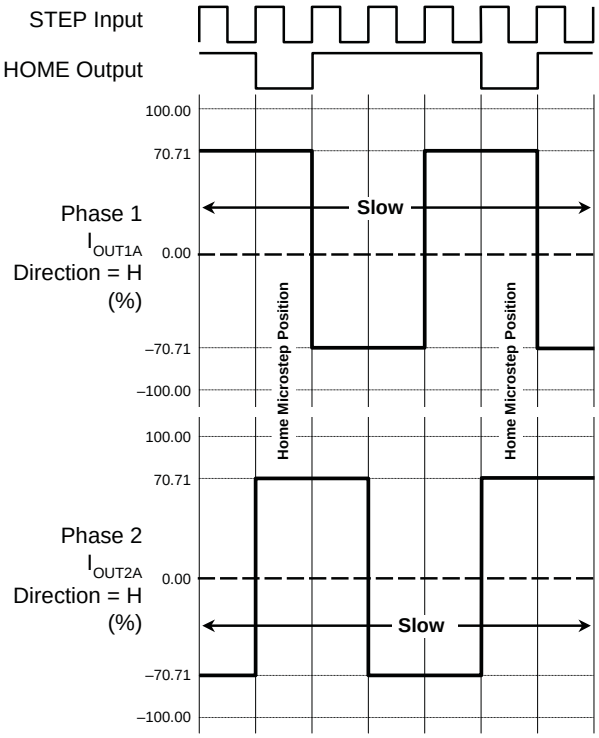


Figure 2. Decay Mode for Full-Step Increments

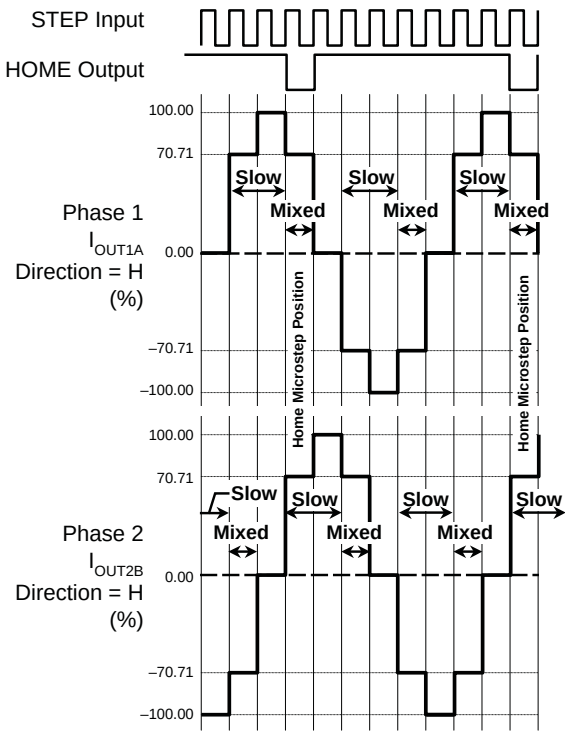


Figure 3. Decay Modes for Half-Step Increments

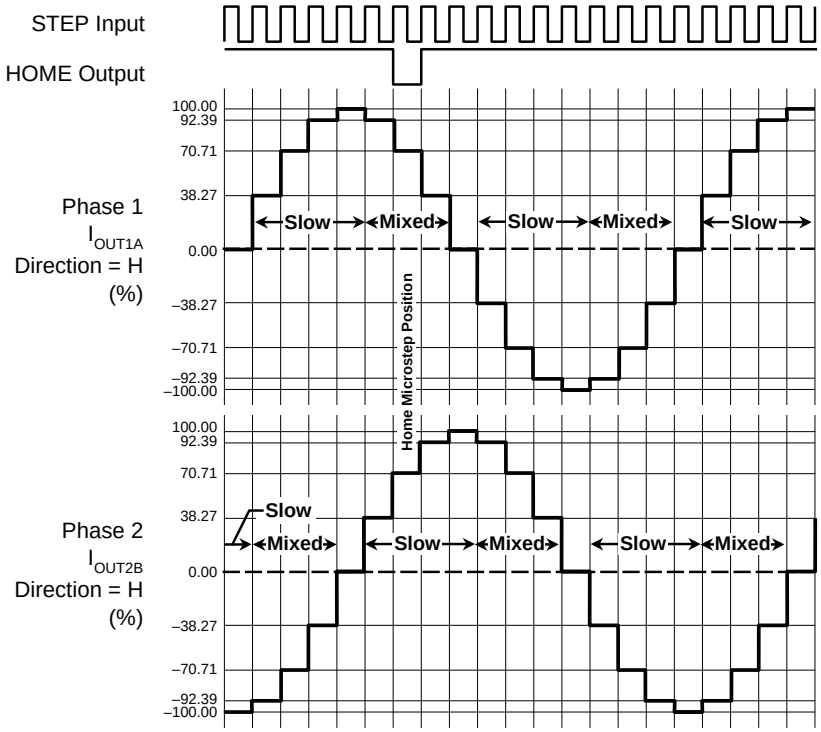


Figure 4. Decay Modes for Quarter-Step Increments

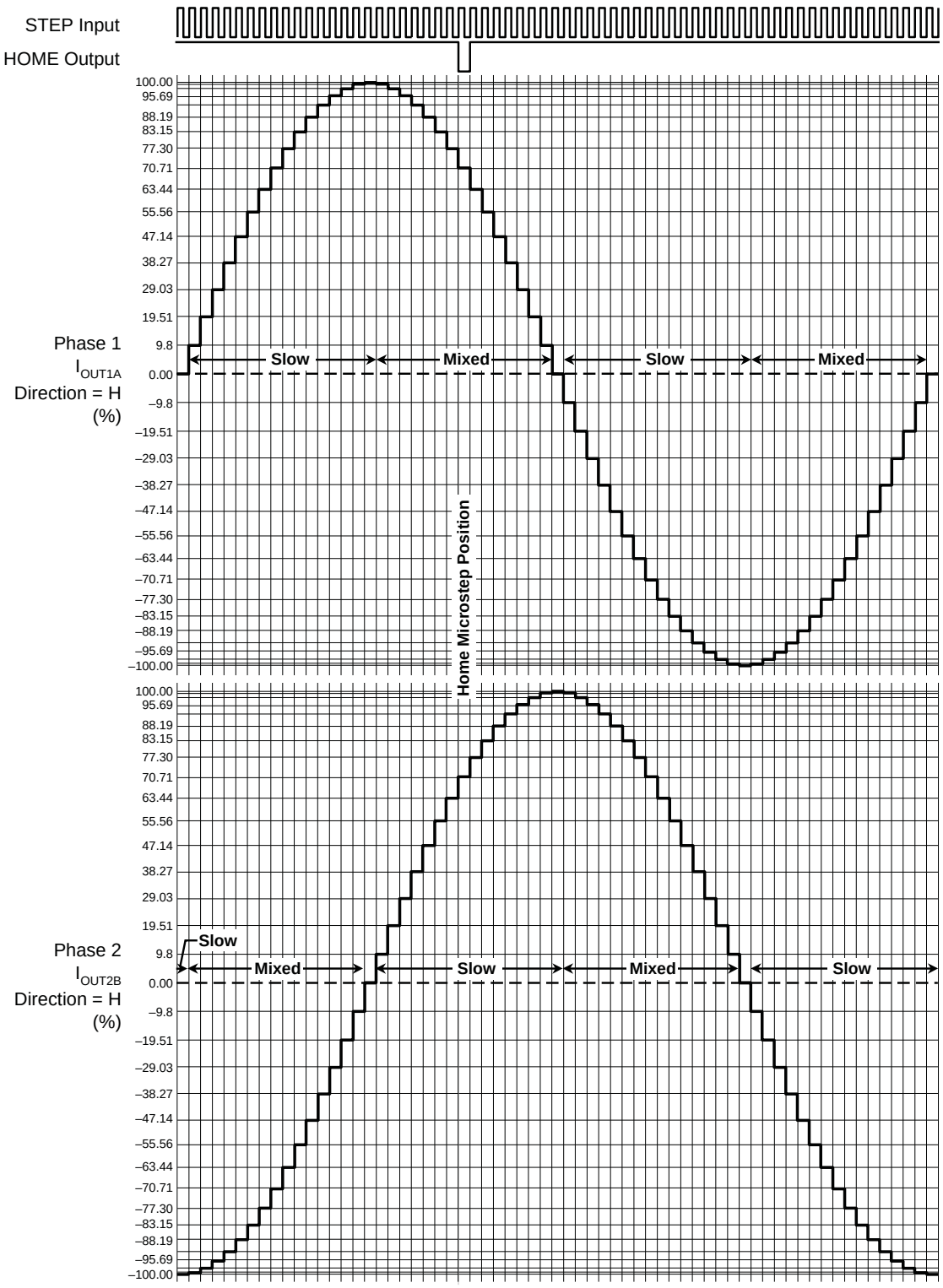


Figure 5. Decay Modes for Sixteenth-Step Increments

Table 2. Step Sequencing Settings

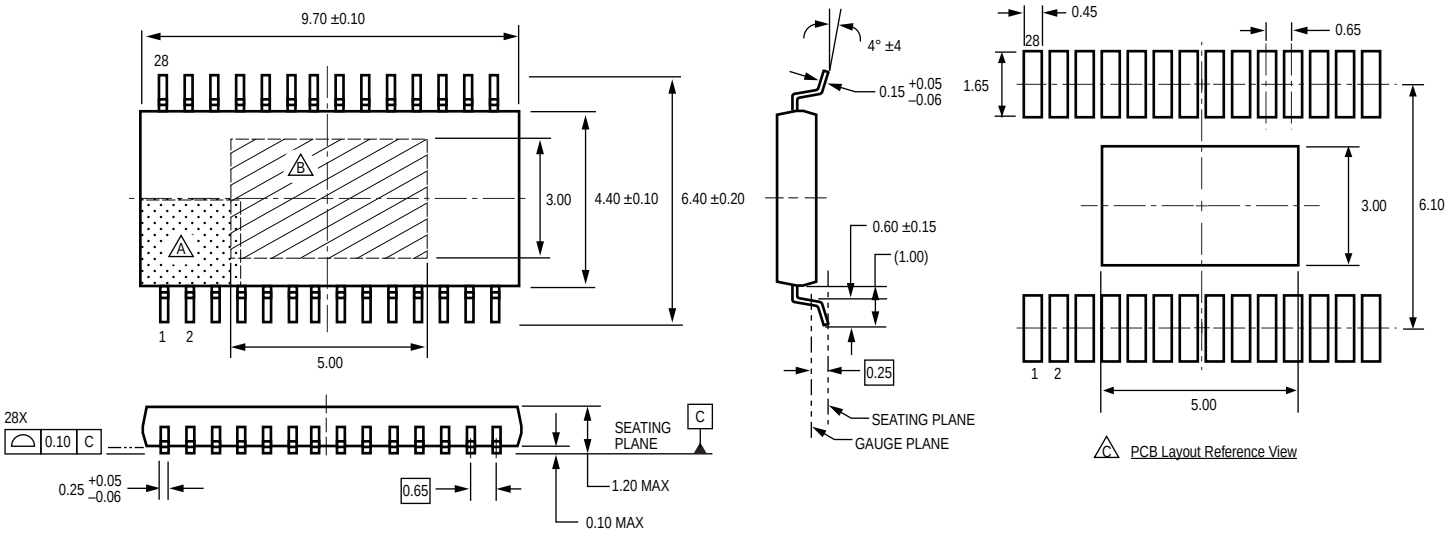
Home microstep position at Step Angle 45°; DIR = H; 360° = 4 full steps

Full Step #	Half Step #	1/4 Step #	1/16 Step #	Phase 1 Current [% $I_{tripMax}$] (%)	Phase 2 Current [% $I_{tripMax}$] (%)	Step Angle (°)	Full Step #	Half Step #	1/4 Step #	1/16 Step #	Phase 1 Current [% $I_{tripMax}$] (%)	Phase 2 Current [% $I_{tripMax}$] (%)	Step Angle (°)
	1	1	1	100.00	0.00	0.0		5	9	33	–100.00	0.00	180.0
			2	99.52	9.80	5.6				34	–99.52	–9.80	185.6
			3	98.08	19.51	11.3				35	–98.08	–19.51	191.3
			4	95.69	29.03	16.9				36	–95.69	–29.03	196.9
		2	5	92.39	38.27	22.5			10	37	–92.39	–38.27	202.5
			6	88.19	47.14	28.1				38	–88.19	–47.14	208.1
			7	83.15	55.56	33.8				39	–83.15	–55.56	213.8
			8	77.30	63.44	39.4				40	–77.30	–63.44	219.4
1	2	3	9	70.71	70.71	45.0	3	6	11	41	–70.71	–70.71	225.0
			10	63.44	77.30	50.6				42	–63.44	–77.30	230.6
			11	55.56	83.15	56.3				43	–55.56	–83.15	236.3
			12	47.14	88.19	61.9				44	–47.14	–88.19	241.9
		4	13	38.27	92.39	67.5			12	45	–38.27	–92.39	247.5
			14	29.03	95.69	73.1				46	–29.03	–95.69	253.1
			15	19.51	98.08	78.8				47	–19.51	–98.08	258.8
			16	9.80	99.52	84.4				48	–9.80	–99.52	264.4
	3	5	17	0.00	100.00	90.0		7	13	49	0.00	–100.00	270.0
			18	–9.80	99.52	95.6				50	9.80	–99.52	275.6
			19	–19.51	98.08	101.3				51	19.51	–98.08	281.3
			20	–29.03	95.69	106.9				52	29.03	–95.69	286.9
		6	21	–38.27	92.39	112.5			14	53	38.27	–92.39	292.5
			22	–47.14	88.19	118.1				54	47.14	–88.19	298.1
			23	–55.56	83.15	123.8				55	55.56	–83.15	303.8
			24	–63.44	77.30	129.4				56	63.44	–77.30	309.4
2	4	7	25	–70.71	70.71	135.0	4	8	15	57	70.71	–70.71	315.0
			26	–77.30	63.44	140.6				58	77.30	–63.44	320.6
			27	–83.15	55.56	146.3				59	83.15	–55.56	326.3
			28	–88.19	47.14	151.9				60	88.19	–47.14	331.9
		8	29	–92.39	38.27	157.5			16	61	92.39	–38.27	337.5
			30	–95.69	29.03	163.1				62	95.69	–29.03	343.1
			31	–98.08	19.51	168.8				63	98.08	–19.51	348.8
			32	–99.52	9.80	174.4				64	99.52	–9.80	354.4

Terminal List Table

Number	Name	Description
1	SENSE1	Sense resistor for Bridge 1
2	HOME	Logic Output
3	DIR	Logic input
4	OUT1A	Output A for Bridge 1
5	PFD	Mixed decay setting
6	RC1	Analog input for fixed off-time for Bridge 1
7	AGND	Analog Ground
8	REF	Current trip reference voltage input
9	RC2	Analog input for fixed off-time for Bridge 2
10	VDD	Logic supply
11	OUT2A	Output A for Bridge 2
12	MS2	Logic input
13	MS1	Logic input
14	SENSE2	Sense resistor for Bridge 2
15	VBB2	Load supply for Bridge 2
16	SR	Logic input
17	$\overline{\text{RESET}}$	Logic input
18	OUT2B	Output B for Bridge 2
19	STEP	Logic input
20	VREG	Regulator decoupling
21	PGND	Power Ground
22	VCP	Reservoir capacitor
23	CP1	Charge pump capacitor 1
24	CP2	Charge pump capacitor 2
25	1OUT1B	Output B for Bridge 1
26	$\overline{\text{ENABLE}}$	Logic input
27	$\overline{\text{SLEEP}}$	Logic input
28	VBB1	Load supply for Bridge 1

LP Package, 28-pin TSSOP



For reference only
(reference JEDEC MO-153 AET)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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