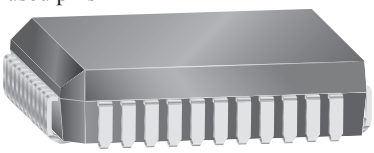
Microstepping DMOS Driver with Translator

Features and Benefits

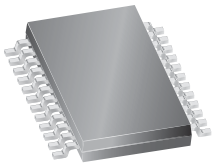
- ±2.5 A, 35 V output rating
- Low $r_{DS(on)}$ outputs, 0.45 Ω source, 0.36 Ω sink typical
- Automatic current decay mode detection/selection
- 3.0 to 5.5 V logic supply voltage range
- Mixed, fast, and slow current decay modes
- Home output
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Crossover-current protection

Packages:

Package ED, 44-pin PLCC
with internally fused pins



Package LP, 28-pin TSSOP
with exposed thermal pad



Not to scale

Description

The A3977 is a complete microstepping motor driver, with built-in translator. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes, with output drive capability of 35 V and ±2.5 A. The A3977 includes a fixed off-time current regulator that has the ability to operate in slow-, fast-, or mixed-decay modes. This current-decay control scheme results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

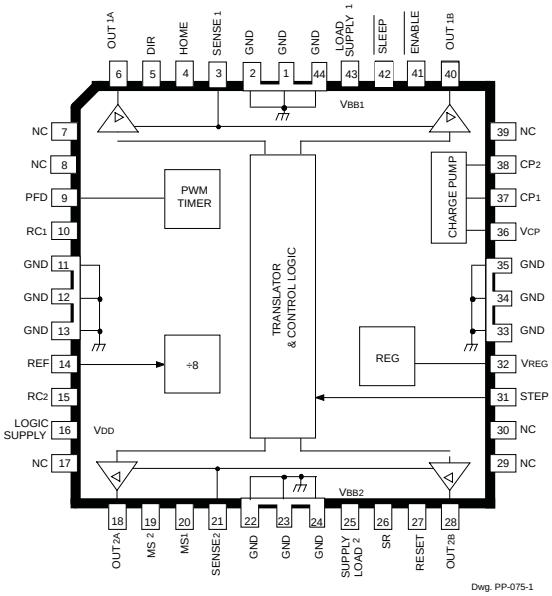
The translator is the key to the easy implementation of the A3977. Simply inputting one pulse on the STEP input drives the motor one step (two logic inputs determine if it is a full-, half-, quarter-, or eighth-step). There are no phase-sequence tables, high-frequency control lines, or complex interfaces to program. The A3977 interface is an ideal fit for applications where a complex microprocessor is unavailable or over-burdened.

Internal synchronous-rectification control circuitry is provided to improve power dissipation during PWM operation.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage lockout (UVLO) and crossover-current protection. Special power-up sequencing is not required.

The A3977 is supplied in a choice of two power packages, a 44-pin plastic PLCC with 3 internally-fused pins on each of four sides (suffix ED), and a thin (<1.2 mm), 28-pin TSSOP with an exposed thermal pad (suffix LP). Both packages are lead (Pb) free, with 100% matte tin leadframe plating.

Pin-out Diagram



Selection Guide

Part Number	Packing	Package	Ambient Temperature, T_A (°C)
~~A3977KEDTR-T*~~	450 per reel	44-pin PLCC	–40 to 125
~~A3977SEDTR-T*~~	450 per reel	44-pin PLCC	–20 to 85
A3977SLPTR-T	4000 per reel	28-pin TSSOP	–20 to 85

*Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change April 23, 2013. Deadline for receipt of LAST TIME BUY orders is September 30, 2013.

Absolute Maximum Ratings

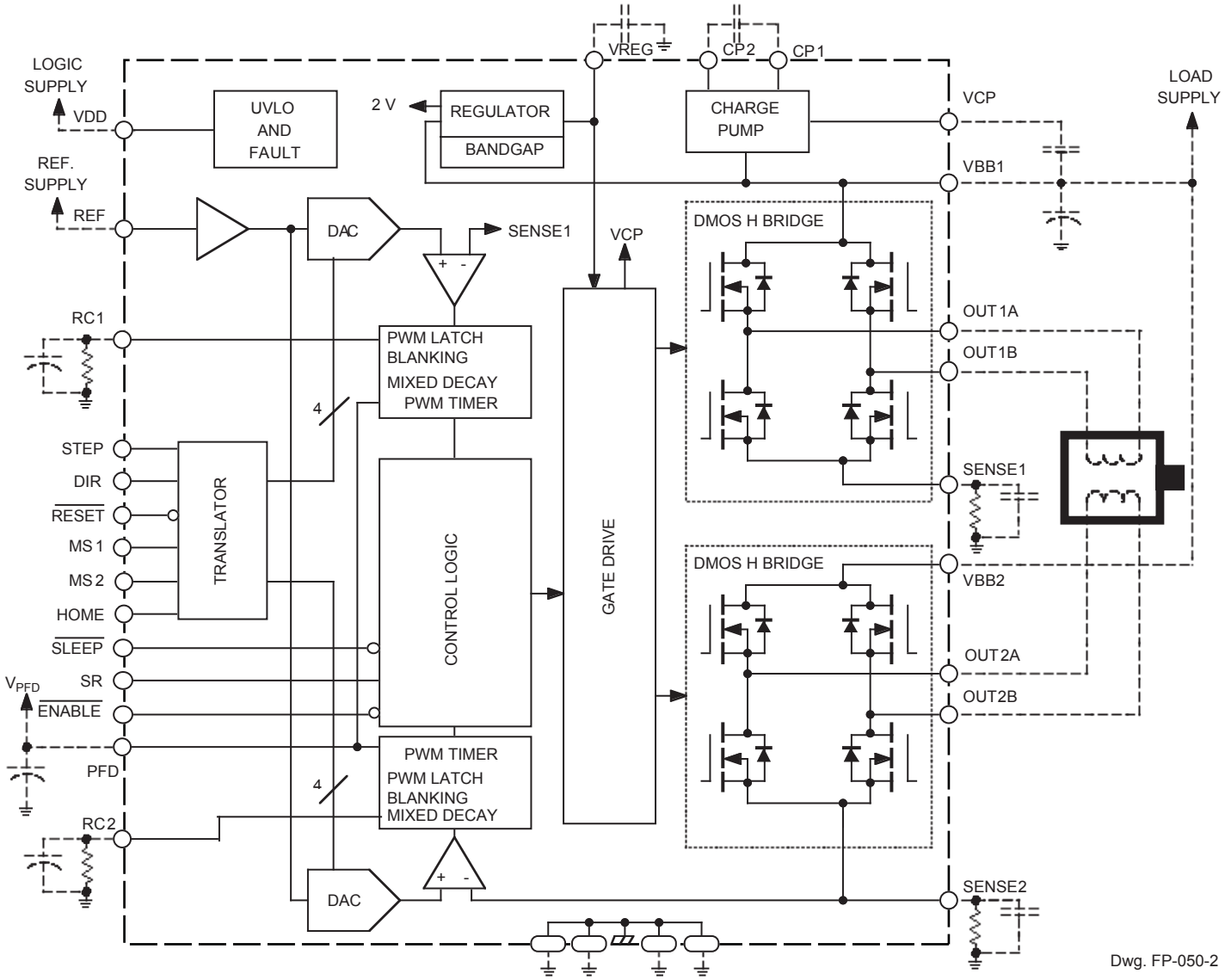
Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		35	V
Logic Supply Voltage	V_{DD}		7.0	V
Logic Input Voltage Range	V_{IN}	Pulsed, t_w > 30 ns	–0.3 to V_{DD}+ 0.3	V
		Pulsed, t_w < 30 ns	–1.0 to V_{DD}+ 1	V
Reference Voltage	V_{REF}		V_{DD}	V
Sense Voltage (DC)	V_{SENSE}		0.5	V
Output Current	I_{OUT}	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	±2.5	A
Operating Ambient Temperature	T_A	Range K	–40 to 125	ºC
		Range S	–20 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics

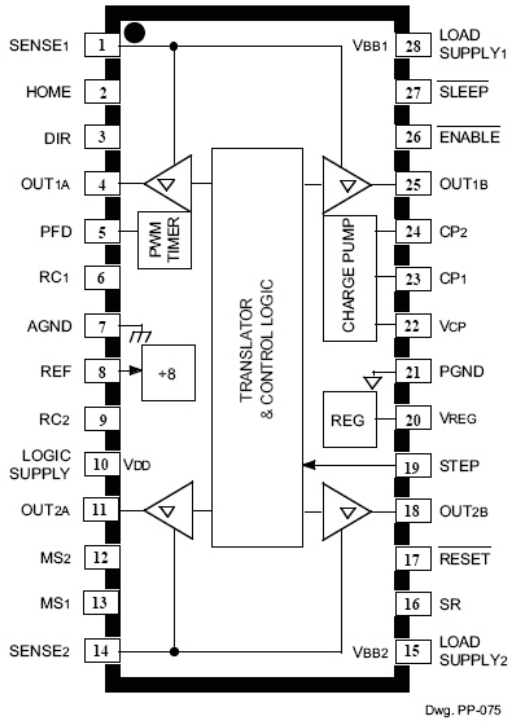
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package ED, on 4-layer PCB based on JEDEC standard	22	ºC/W
		Package LP, on 4-layer PCB based on JEDEC standard	28	ºC/W

*Additional thermal information available on the Allegro website.

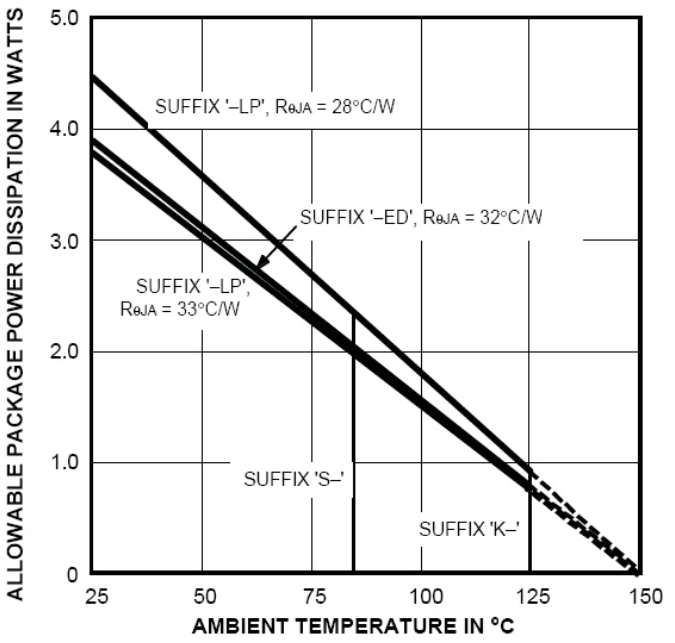
FUNCTIONAL BLOCK DIAGRAM



LP Pin-out
(TSSOP)



Dwg. PP-075



Dwg. GP-018-2A

Table 1. Microstep Resolution Truth Table

MS_1	MS_2	Resolution
L	L	Full step (2 phase)
H	L	Half step
L	H	Quarter step
H	H	Eighth step

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 35 V, V_{DD} = 3.0 V to 5.5V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	8.0	–	35	V
		During sleep mode	0	–	35	V
Output Leakage Current	I_{DSS}	$V_{OUT} = V_{BB}$	–	<1.0	20	µA
		V_{OUT} = 0 V	–	<1.0	-20	µA
Output On Resistance	$r_{DS(on)}$	Source driver, I_{OUT} = -2.5 A	–	0.45	0.57	Ω
		Sink driver, I_{OUT} = 2.5 A	–	0.36	0.43	Ω
Body Diode Forward Voltage	V_F	Source diode, I_F = -2.5 A	–	–	1.4	V
		Sink diode, I_F = 2.5 A	–	–	1.4	V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	–	8.0	mA
		Operating, outputs disabled	–	–	6.0	mA
		Sleep mode	–	–	20	µA
Control Logic						
Logic Supply Voltage Range	V_{DD}	Operating	3.0	5.0	5.5	V
Logic Input Voltage	$V_{IN(1)}$		$0.7V_{DD}$	–	–	V
	$V_{IN(0)}$		–	–	$0.3V_{DD}$	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = 0.7V_{DD}$	-20	<1.0	20	µA
	$I_{IN(0)}$	$V_{IN} = 0.3V_{DD}$	-20	<1.0	20	µA
Maximum STEP Frequency	f_{STEP}		500*	–	–	kHz
HOME Output Voltage	V_{OH}	I_{OH} = -200 µA	$0.7V_{DD}$	–	–	V
	V_{OL}	I_{OL} = 200 µA	–	–	$0.3V_{DD}$	V
Blank Time	t_{BLANK}	R_t = 56 kΩ, C_t = 680 pF	700	950	1200	ns
Fixed Off Time	t_{off}	R_t = 56 kΩ, C_t = 680 pF	30	38	46	µs
Mixed Decay Trip Point	PFDH		–	$0.6V_{DD}$	–	V
	PFDL		–	$0.21V_{DD}$	–	V
Ref. Input Voltage Range	V_{REF}	Operating	0	–	V_{DD}	V
Reference Input Current	I_{REF}		–	0	±3.0	µA
Gain (G_m) Error (note 3)	E_G	V_{REF} = 2 V, Phase Current = 38.27%	–	–	±10	%
		V_{REF} = 2 V, Phase Current = 70.71%	–	–	±5.0	%
		V_{REF} = 2 V, Phase Current = 100.00%	–	–	±5.0	%
Crossover Dead Time	t_{DT}	SR enabled	100	475	800	ns

Continued on the next page…

ELECTRICAL CHARACTERISTICS (continued) at T_A = +25°C, V_{BB} = 35 V, V_{DD} = 3.0 V to 5.5V (unless otherwise noted)						
Characteristic	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Output Drivers (continued)						
Thermal Shutdown Temp.	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	15	–	°C
UVLO Enable Threshold	V_{UVLO}	Increasing V_{DD}	2.45	2.7	2.95	V
UVLO Hysteresis	ΔV_{UVLO}		0.05	0.10	–	V
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz	–	–	12	mA
		Outputs off	–	–	10	mA
		Sleep mode	–	–	20	µA

* Operation at a step frequency greater than the specified minimum value is possible but not warranteed.

NOTES:

1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.
3. $E_G = ([V_{REF}/8] – V_{SENSE})/(V_{REF}/8)$

Functional Description

Device Operation. The A3977 is a complete microstepping motor driver with built in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, quarter- and eighth-step modes. The current in each of the two output full-bridges, all N-channel DMOS, is regulated with fixed off-time pulse-width modulated (PWM) control circuitry. The full-bridge current at each step is set by the value of an external current sense resistor (R_S), a reference voltage (V_{REF}), and the DACs output voltage controlled by the output of the translator.

At power up, or reset, the translator sets the DACs and phase current polarity to initial home state (see figures for home-state conditions), and sets the current regulator for both phases to mixed-decay mode. When a step command signal occurs on the STEP input the translator automatically sequences the DACs to the next level (see table 2 for the current level sequence and current polarity). The microstep resolution is set by inputs MS_1 and MS_2 as shown in table 1. If the new DAC output level is lower than the previous level the decay mode for that full-bridge will be set by the PFD input (fast, slow, or mixed decay). If the new DAC level is higher or equal to the previous level then the decay mode for that full-bridge will be slow decay. This automatic current-decay selection will improve microstepping performance by reducing the distortion of the current waveform due to the motor BEMF.

Reset Input ($\overline{\text{RESET}}$). The RESET input (active low) sets the translator to a predefined home state (see figures for home state conditions) and turns off all of the DMOS outputs. The HOME output goes low and all STEP inputs are ignored until the RESET input goes high.

Home Output (HOME). The HOME output is a logic output indicator of the initial state of the translator. At power up the translator is reset to the home state (see figures for home state conditions).

Step Input (STEP). A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the state of inputs MS_1 and MS_2 (see table 1).

Microstep Select (MS_1 and MS_2). Input terminals MS1 and MS_2 select the microstepping format per table 1. Changes to these inputs do not take effect until the STEP command (see figure).

Direction Input (DIR). The state of the DIRECTION input will determine the direction of rotation of the motor.

Internal PWM Current Control. Each full-bridge is controlled by a fixed off-time PWM current-control circuit that limits the load current to a desired value (I_{TRIP}). Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and R_S. When the voltage across the current-sense resistor equals the DAC output voltage, the current-sense comparator resets the PWM latch, which turns off the source driver (slow-decay mode) or the sink and source drivers (fast- or mixed-decay modes).

The maximum value of current limiting is set by the selection of R_S and the voltage at the V_{REF} input with a transconductance function approximated by:

$$I_{TRIP}max = V_{REF}/8R_S$$

The DAC output reduces the V_{REF} output to the current-sense comparator in precise steps (see table 2 for % I_{TRIP}max at each step).

$$I_{TRIP} = (\%\ I_{TRIP}max/100) \times I_{TRIP}max$$

It is critical to ensure that the maximum rating (0.5 V) on the SENSE terminal is not exceeded. For full-step mode, V_{REF} can be applied up to the maximum rating of V_{DD}, because the peak sense value is 0.707 x V_{REF}/8. In all other modes V_{REF} should not exceed 4 V.

Functional Description (cont'd)

Fixed Off-Time. The internal PWM current-control circuitry uses a one shot to control the time the drivers remain off. The one shot off-time, t_{off}, is determined by the selection of an external resistor (R_T) and capacitor (C_T) connected from the RC timing terminal to ground. The off-time, over a range of values of C_T = 470 pF to 1500 pF and R_T = 12 kΩ to 100 kΩ is approximated by:

$$t_{off} = R_T C_T$$

RC Blanking. In addition to the fixed off-time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the current-sense comparator when the outputs are switched by the internal current-control circuitry. The comparator output is blanked to prevent false over-current detection due to reverse recovery currents of the clamp diodes, and/or switching transients related to the capacitance of the load. The blank time t_{BLANK} can be approximated by:

$$t_{BLANK} = 1400 C_T$$

Charge Pump. (CP_1 and CP_2). The charge pump is used to generate a gate supply greater than V_{BB} to drive the source-side DMOS gates. A 0.22 µF ceramic capacitor should be connected between CP_1 and CP_2 for pumping purposes. A 0.22 µF ceramic capacitor is required between V_{CP} and V_{BB} to act as a reservoir to operate the high-side DMOS devices.

V_{REG}. This internally generated voltage is used to operate the sink-side DMOS outputs. The V_{REG} terminal should be decoupled with a 0.22 µF capacitor to ground. V_{REG} is internally monitored and in the case of a fault condition, the outputs of the device are disabled.

Enable Input (ENABLE). This active-low input enables all of the DMOS outputs. When logic high the outputs are disabled. Inputs to the translator (STEP, DIRECTION, MS_1, MS_2) are all active independent of the ENABLE input state.

Shutdown. In the event of a fault (excessive junction temperature, or low voltage on V_{CP}) the outputs of the device are disabled until the fault condition is removed. At power up, and in the event of low V_{DD}, the undervoltage lockout (UVLO) circuit disables the drivers and resets the translator to the HOME state.

Sleep Mode (SLEEP). An active-low control input used to minimize power consumption when not in use. This disables much of the internal circuitry including the output DMOS, regulator, and charge pump. A logic high allows normal operation and startup of the device in the home position. When coming out of sleep mode, wait 1 ms before issuing a STEP command to allow the charge pump (gate drive) to stabilize.

Percent Fast Decay Input (PFD). When a STEP input signal commands a lower output current from the previous step, it switches the output current decay to either slow-, fast-, or mixed-decay depending on the voltage level at the PFD input. If the voltage at the PFD input is greater than 0.6 V_{DD} then slow-decay mode is selected. If the voltage on the PFD input is less than 0.21 V_{DD} then fast-decay mode is selected. Mixed decay is between these two levels. This terminal should be decoupled with a 0.1 µF capacitor.

Mixed Decay Operation. If the voltage on the PFD input is between $0.6V_{DD}$ and $0.21V_{DD}$, the bridge will operate in mixed-decay mode depending on the step sequence (see figures). As the trip point is reached, the device will go into fast-decay mode until the voltage on the RC terminal decays to the voltage applied to the PFD terminal. The time that the device operates in fast decay is approximated by:

$$t_{FD} = R_T C_T \ln (0.6V_{DD}/V_{PFD})$$

After this fast decay portion, t_{FD}, the device will switch to slow-decay mode for the remainder of the fixed off-time period.

Functional Description (cont'd)

Synchronous Rectification. When a PWM off-cycle is triggered by an internal fixed off-time cycle, load current will recirculate according to the decay mode selected by the control logic. The A3977 synchronous rectification feature will turn on the appropriate MOSFETs during the current decay and effectively short out the body diodes with the low $r_{DS(on)}$ driver. This will reduce power dissipation significantly and eliminate the need for external Schottky diodes for most applications.

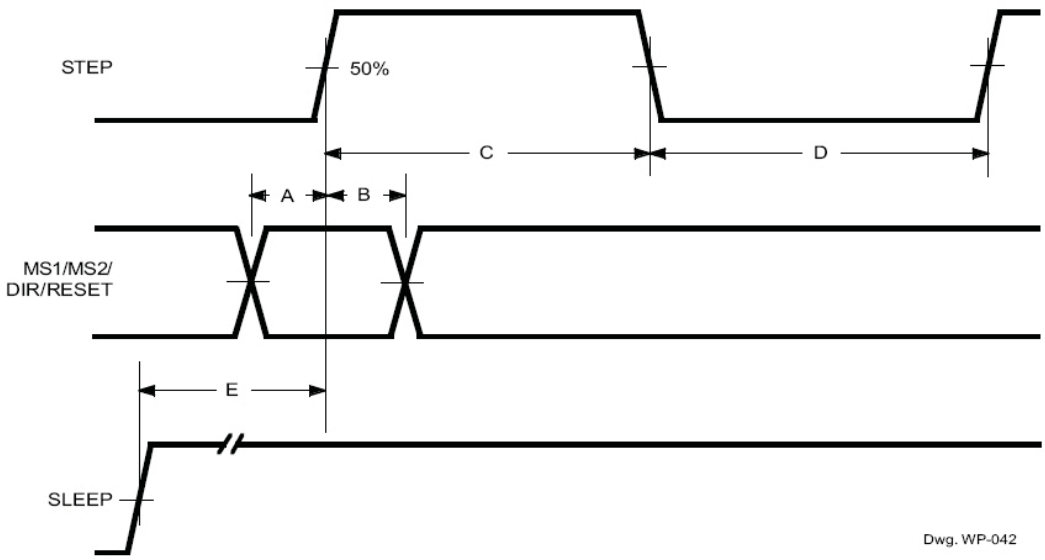
The synchronous rectification can be set in either active mode or disabled mode.

Active Mode. When the SR input is logic low, active mode is enabled and synchronous rectification will occur. This mode prevents reversal of the load current by turning off synchronous rectification when a zero current level is detected. This prevents the motor winding from conducting in the reverse direction.

Disabled Mode. When the SR input is logic high, synchronous rectification is disabled. This mode is typically used when external diodes are required to transfer power dissipation from the A3977 package to the external diodes.

Timing Requirements

(T_A = +25°C, V_{DD} = 5 V, Logic Levels are V_{DD} and Ground)



A. Minimum Command Active Time
Before Step Pulse (Data Set-Up Time) ..... 200 ns

B. Minimum Command Active Time
After Step Pulse (Data Hold Time) ..... 200 ns

C. Minimum STEP Pulse Width ..... 1.0 µs

D. Minimum STEP Low Time ..... 1.0 µs

E. Maximum Wake-Up Time ..... 1.0 ms

Applications Information

Layout.

The printed wiring board should use a heavy ground plane.

For optimum electrical and thermal performance, the driver should be soldered directly onto the board.

The load supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (>47 µF is recommended) placed as close to the device as possible.

To avoid problems due to capacitive coupling of the high dv/dt switching transients, route the bridge-output traces away from the sensitive logic-input traces. Always drive the logic inputs with a low source impedance to increase noise immunity.

Grounding. A star ground system located close to the driver is recommended.

The 44-lead PLCC has the analog ground and the power ground internally bonded to the power tabs of the package (leads 44, 1, 2, 11 – 13, 22 – 24, and 33 – 35).

On the 28-lead TSSOP package, the analog ground (lead 7) and the power ground (lead 21) must be connected together externally. The copper ground plane located under the exposed thermal pad is typically used as the star ground.

Current Sensing. To minimize inaccuracies caused by ground-trace IR drops in sensing the output current level, the current-sense resistor (R_S) should have an independent ground return to the star ground of the device. This path should be as short as possible. For low-value sense resistors the IR drops in the printed wiring board sense resistor's traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

Allegro MicroSystems recommends a value of R_S given by

$$R_S = 0.5/I_{TRIP}max$$

Thermal Protection. Circuitry turns off all drivers when the junction temperature reaches 165°C, typically. It is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

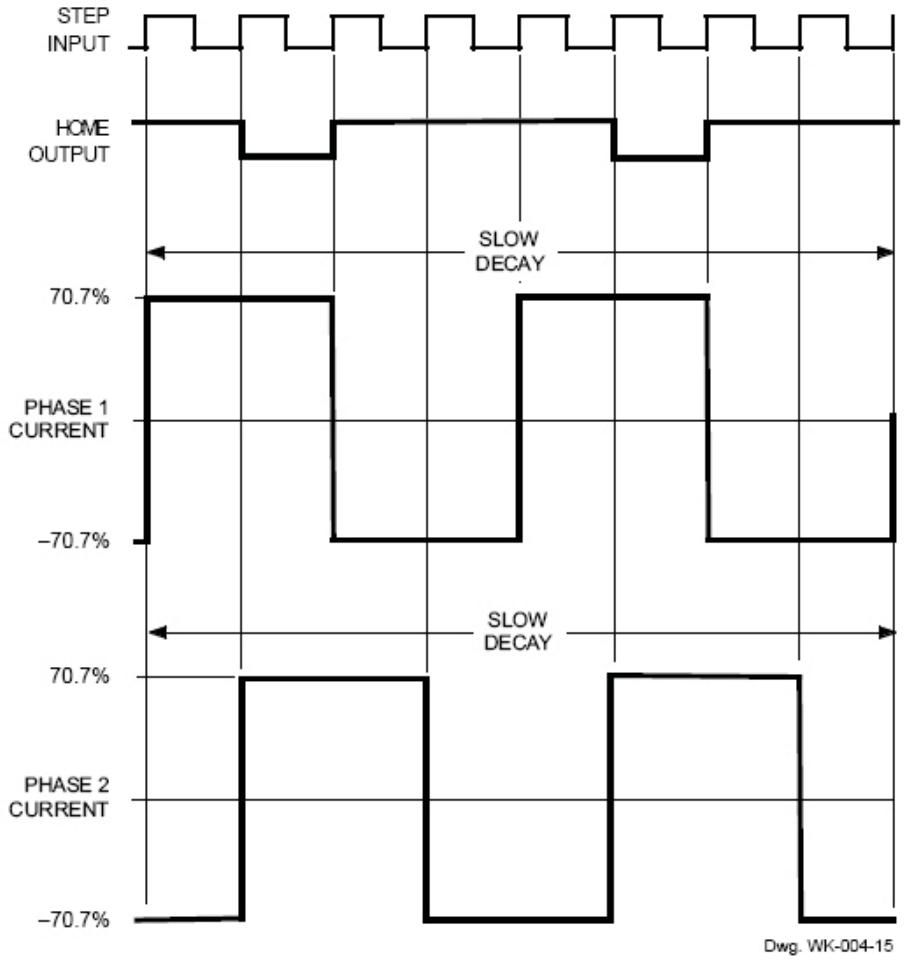
Table 2. Step Sequencing
(DIR = L)

Full Step #	Half Step #	Quarter Step #	Eighth Step #	Phase 2 Current [%I_{trip}max]	Phase 1 Current [%I_{trip}max]	Step Angle
	1	1	1	0.00	100.00	0
			2	19.51	98.08	11.25
		2	3	38.27	92.39	22.50
			4	55.56	83.15	33.75
1	2	3	5	70.71	70.71	45*
			6	83.15	55.56	56.25
		4	7	92.39	38.27	67.50
			8	98.08	19.51	78.75
	3	5	9	100.00	0.00	90
			10	98.08	-19.51	101.25
		6	11	92.39	-38.27	112.50
			12	83.15	-55.56	123.75
2	4	7	13	70.71	-70.71	135
			14	55.56	-83.15	146.25
		8	15	38.27	-92.39	157.50
			16	19.51	-98.08	168.75
	5	9	17	0.00	-100.00	180
			18	-19.51	-98.08	191.25
		10	19	-38.27	-92.39	202.50
			20	-55.56	-83.15	213.75
3	6	11	21	-70.71	-70.71	225
			22	-83.15	-55.56	236.25
		12	23	-92.39	-38.27	247.50
			24	-98.08	-19.51	258.75
	7	13	25	-100.00	0.00	270
			26	-98.08	19.51	281.25
		14	27	-92.39	38.27	292.50
			28	-83.15	55.56	303.75
4	8	15	29	-70.71	70.71	315
			30	-55.56	83.15	326.25
		16	31	-38.27	92.39	337.50
			32	-19.51	98.08	348.75

* Home state; HOME output low.

Full-Step Operation

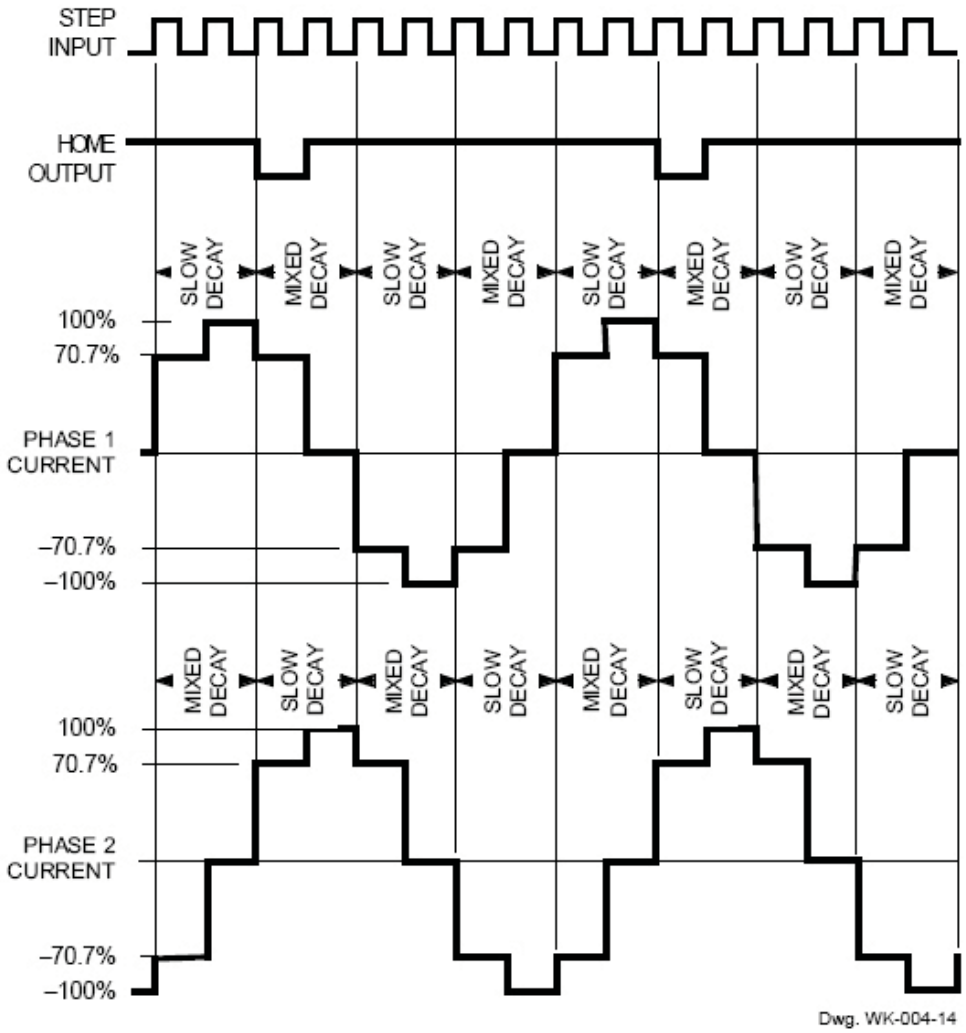
$MS_1 = MS_2 = L$, DIR = H



The vector addition of the output currents at any step is 100%.

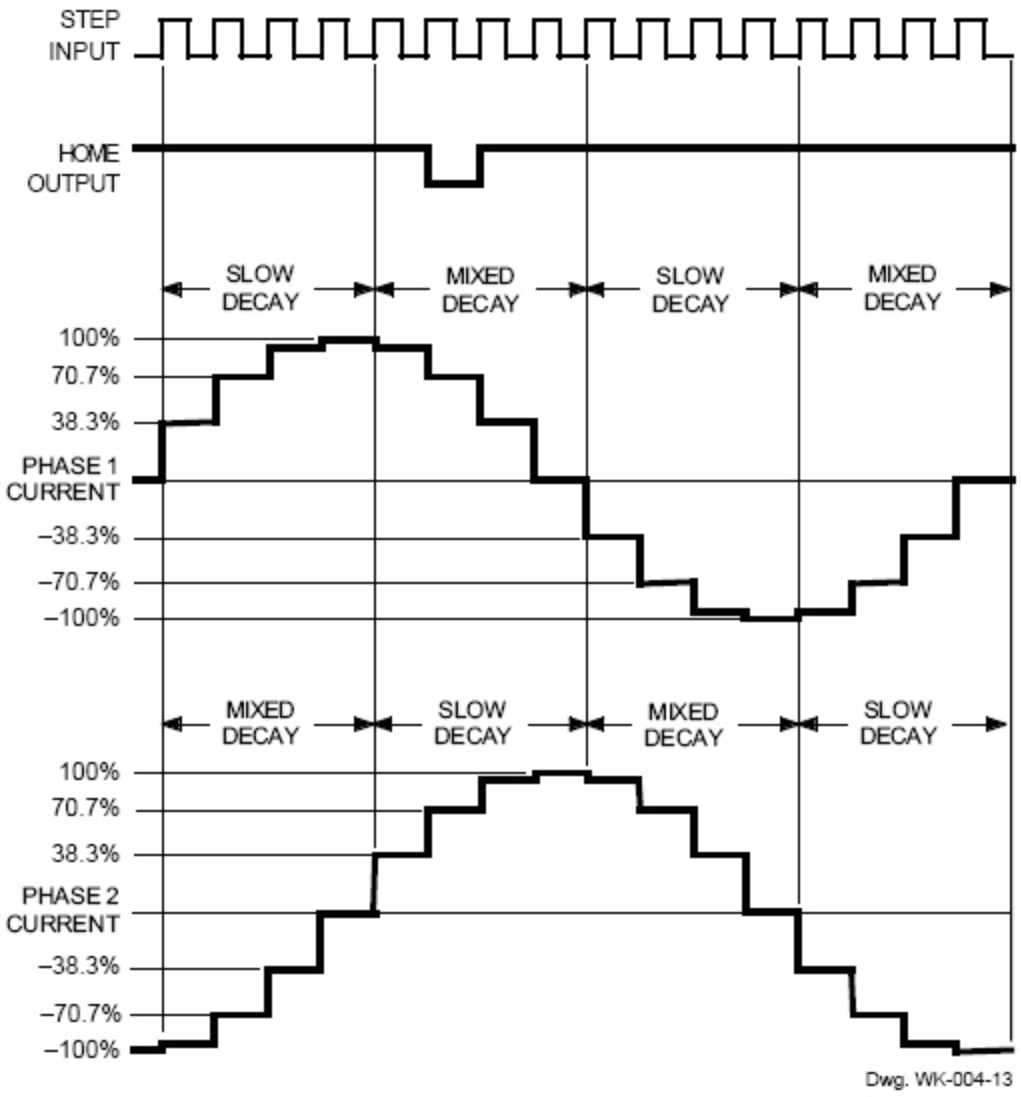
Half-Step Operation

MS_1 = H, MS_2 = L, DIR = H



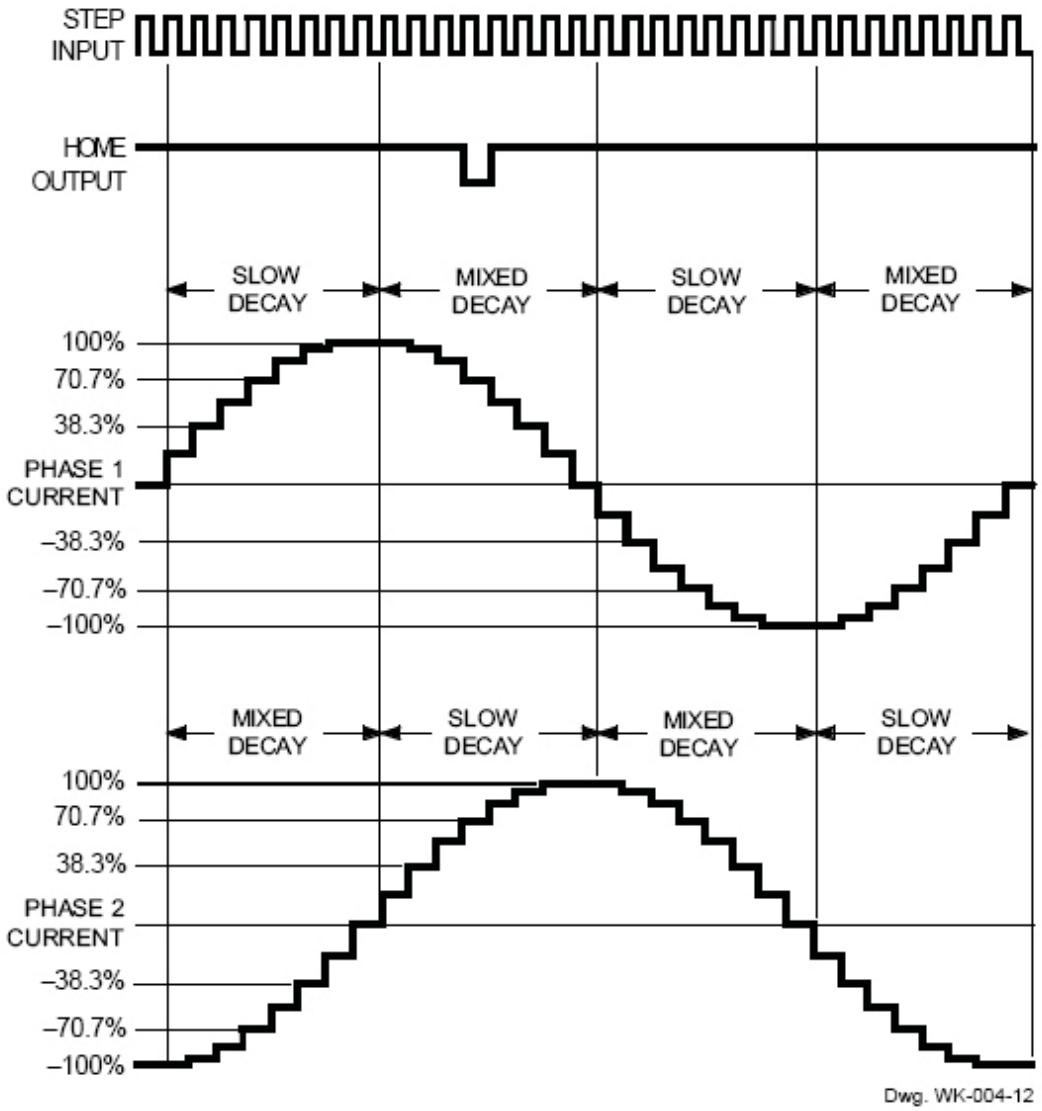
The mixed-decay mode is controlled by the percent fast decay voltage (V_{PFD}). If the voltage at the PFD input is greater than $0.6V_{DD}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{DD}$ then fast-decay mode is selected. Mixed decay is between these two levels.

Quarter-Step Operation
MS_1 = L, MS_2 = H, DIR = H



The mixed-decay mode is controlled by the percent fast decay voltage (V_{PFD}). If the voltage at the PFD input is greater than $0.6V_{DD}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{DD}$ then fast-decay mode is selected. Mixed decay is between these two levels.

8 Microstep/Step Operation
$MS_1 = MS_2 = H$, DIR = H



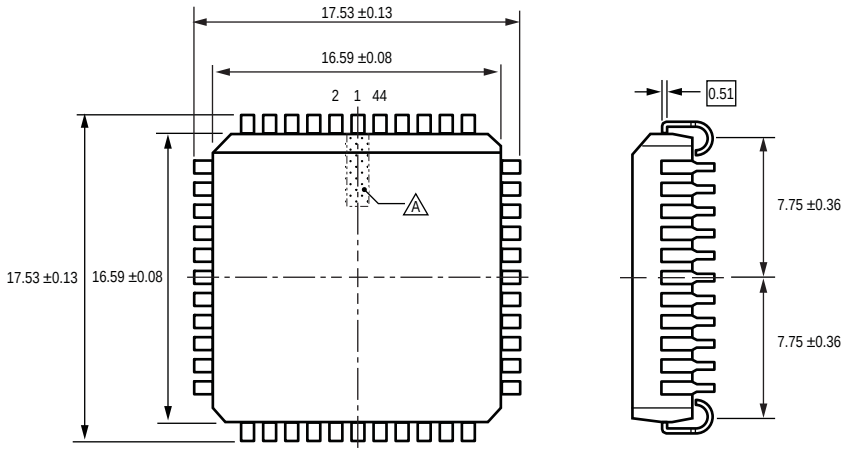
The mixed-decay mode is controlled by the percent fast decay voltage (V_{PFD}). If the voltage at the PFD input is greater than $0.6V_{DD}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{DD}$ then fast-decay mode is selected. Mixed decay is between these two levels.

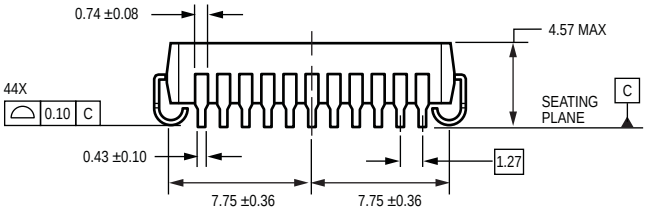
Terminal List

Terminal Name	Terminal Description	LP (TSSOP)	ED (PLCC)
GND	Analog and power ground	–	44, 1, 2
SENSE1	Sense resistor for bridge 1	1	3
HOME	Logic output	2	4
DIR	Logic Input	3	5
OUT1A	DMOS H bridge 1 output A	4	6
NC	No (internal) connection	–	7, 8
PFD	Mixed decay setting	5	9
RC1	Analog Input for fixed offtime – bridge 1	6	10
GND	Analog and power ground	–	11, 12, 13
AGND	Analog ground	7*	–
REF	Gm reference input	8	14
RC2	Analog input for fixed offtime – bridge 2	9	15
LOGIC SUPPLY	V_{DD}, the logic supply voltage	10	16
NC	No (internal) connection	–	17
OUT2A	DMOS H bridge 2 output A	11	18
MS2	Logic input	12	19
MS1	Logic input	13	20
SENSE2	Sense resistor for bridge 2	14	21
GND	Analog and power ground	–	22, 23, 24
LOAD SUPPLY2	V_{BB2}, the load supply for bridge 2	15	25
SR	Logic input	16	26
RESET	Logic input	17	27
OUT2B	DMOS H bridge 2 output B	18	28
NC	No (internal) connection	–	29, 30
STEP	Logic input	19	31
VREG	Regulator decoupling	20	32
PGND	Power ground	21*	–
GND	Analog and power ground	–	33, 34, 35
VCP	Reservoir capacitor	22	36
CP1	Charge pump capacitor	23	37
CP2	Charge pump capacitor	24	38
NC	No (internal) connection	–	39
OUT1B	DMOS H bridge 1 output B	25	40
ENABLE	Logic input	26	41
SLEEP	Logic input	27	42
LOAD SUPPLY1	V_{BB1}, the load supply for bridge 1	28	43

* AGND and PGND on the TSSOP package must be connected together externally.

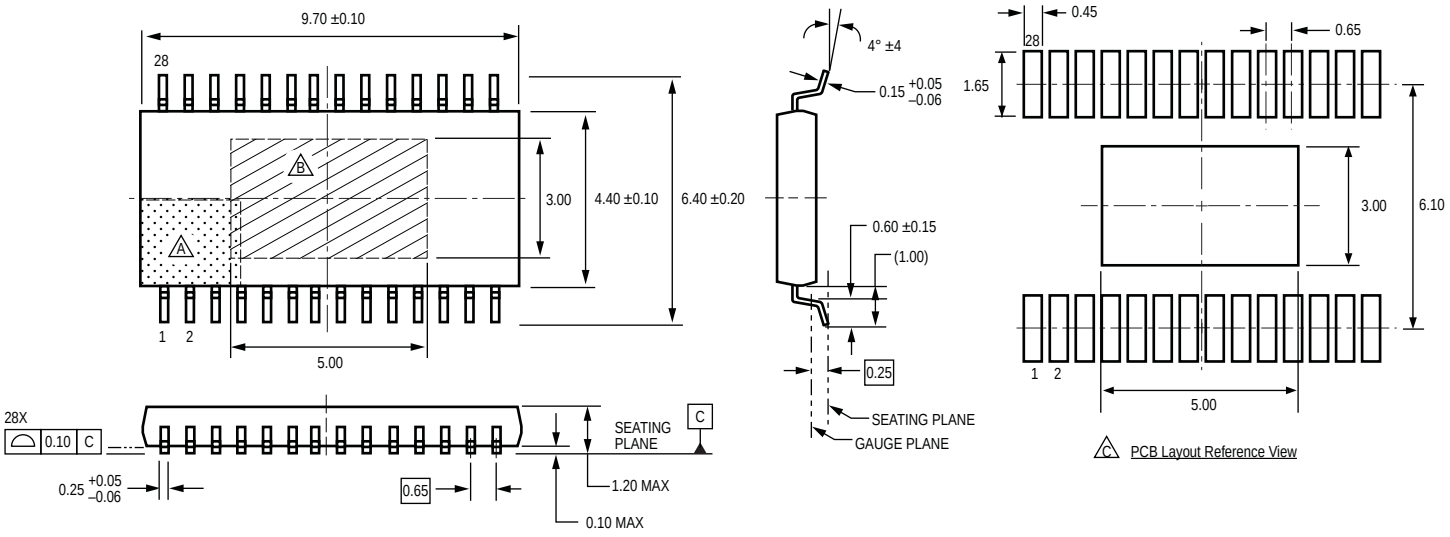
ED Package, 44-pin PLCC





For Reference Only
(reference JEDEC MS-018 AC)
Dimensions in millimeters
Internally fused pins 44, 1 and 2; 11-13; 22-24; and 33-35
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

LP Package, 28-pin TSSOP



For reference only
(reference JEDEC MO-153 AET)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Revision Date	Description of Revision
Rev. K	April 23, 2013	Update product selection and applications component recommendations

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