DATASHEET

DDR I/DDR II Phase Lock Loop Zero Delay Buffer

ICS9P935

Description

DDR I/DDR II Zero Delay Clock Buffer

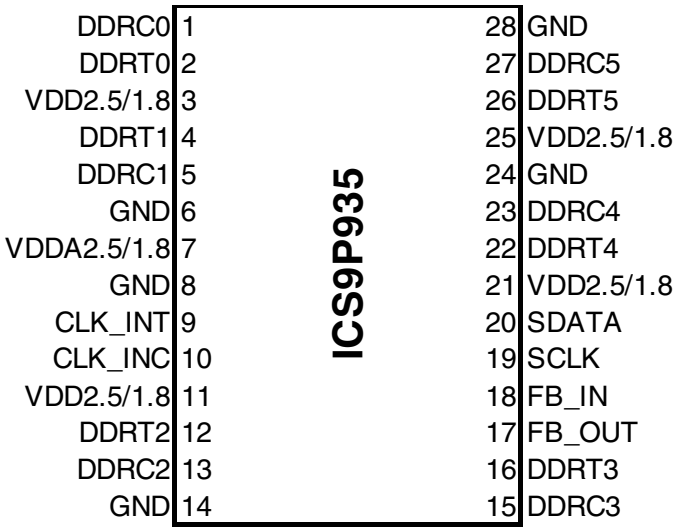
Output Features

- Low skew, low jitter PLL clock driver
- Max frequency supported = 400MHz (DDRII 800)
- I^2C for functional and output control
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- Programmable skew through SMBus
- Frequency defect control thorugh SMBus
- Individual output control programmable through SMBus

Key Specifications

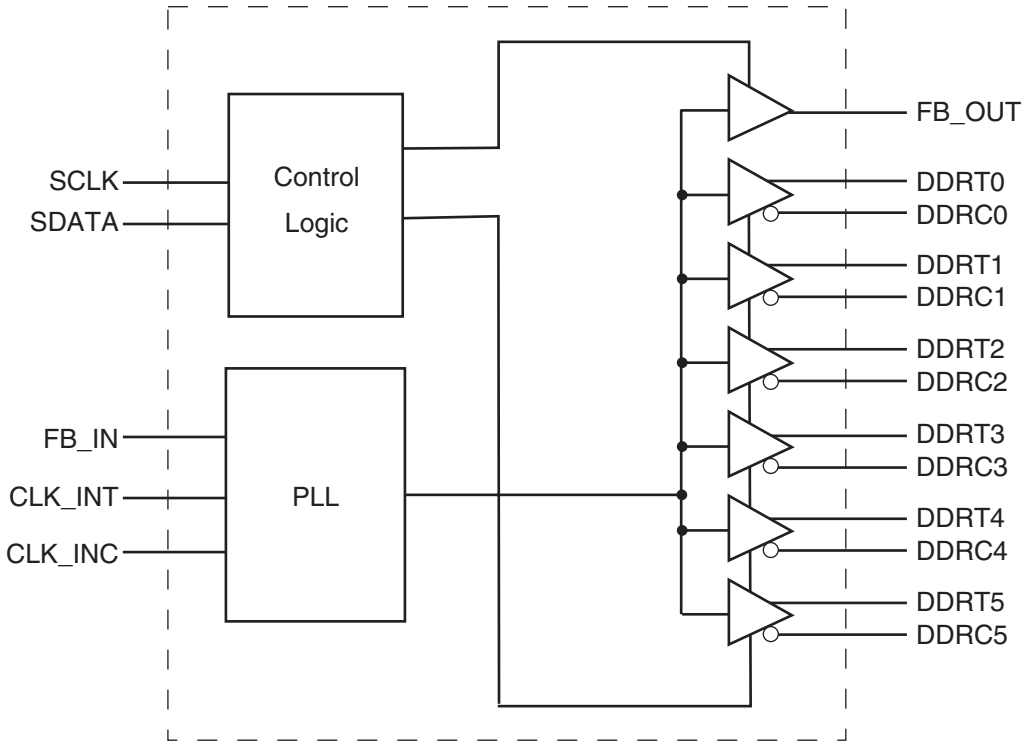
- CYCLE - CYCLE jitter: <100ps
- OUTPUT - OUTPUT skew: <100ps
- DUTY CYCLE: 48% - 52%
- 28-pin SSOP package
- Available in RoHS compliant packaging
- Operates @ 2.5V or 1.8V

Pin Configuration



28-SSOP/TSSOP

Funtional Block Diagram



Pin Description

Pin#	Pin Name	Type	Pin Description
1	DDRC0	OUT	"Complementary" Clock of differential pair output.
2	DDRT0	OUT	"True" Clock of differential pair output.
3	VDD2.5/1.8	PWR	Power supply, nominal 2.5V or 1.8V
4	DDRT1	OUT	"True" Clock of differential pair output.
5	DDRC1	OUT	"Complementary" Clock of differential pair output.
6	GND	PWR	Ground pin.
7	VDDA2.5/1.8	PWR	Output power supply, nominal 2.5V or 1.8V
8	GND	PWR	Ground pin.
9	CLK_INT	IN	"True" reference clock input.
10	CLK_INC	IN	"Complementary" reference clock input.
11	VDD2.5/1.8	PWR	Power supply, nominal 2.5V or 1.8V
12	DDRT2	OUT	"True" Clock of differential pair output.
13	DDRC2	OUT	"Complementary" Clock of differential pair output.
14	GND	PWR	Ground pin.
15	DDRC3	OUT	"Complementary" Clock of differential pair output.
16	DDRT3	OUT	"True" Clock of differential pair output.
17	FB_OUT	OUT	Feedback output, dedicated for external feedback.
18	FB_IN	IN	Single-ended feedback input, provides feedback signal to internal PLL to eliminate phase error with the input clock.
19	SCLK	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
20	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
21	VDD2.5/1.8	PWR	Power supply, nominal 2.5V or 1.8V
22	DDRT4	OUT	"True" Clock of differential pair output.
23	DDRC4	OUT	"Complementary" Clock of differential pair output.
24	GND	PWR	Ground pin.
25	VDD2.5/1.8	PWR	Power supply, nominal 2.5V or 1.8V
26	DDRT5	OUT	"True" Clock of differential pair output.
27	DDRC5	OUT	"Complementary" Clock of differential pair output.
28	GND	PWR	Ground pin.

Absolute Max

Supply Voltage	-0.5V to 2.7V
Logic Inputs	GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature	0°C to +70°C
Case Temperature	115°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage AVDD, VDD = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND			±250	µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			±10	µA
Output Disabled Low Current	I_{ODL}	OE = L, V_{ODL} = 100mV	100			µA
Operating Supply Current	$I_{DD1.8}$	C_L = 0pf @ 100MHz			300	mA
	I_{DDLD}	C_L = 0pf			500	µA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 1.8V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	I_{OH} = -100µA	V_{DD} -0.2			V
		I_{OH} = -9mA	1.1			V
Low-level output voltage	V_{OL}	I_{OL}=100µA			0.1	V
		I_{OL}=9mA			0.6	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}	2		3	pF
Output Capacitance[1]	C_{OUT}	V_{OUT} = GND or V_{DD}	2		3	pF

Recommended Operating Condition (see note1)

T_A = 0 - 70°C; Supply Voltage AVDD, VDD = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DDQ}, A_{VDD}		1.7	1.8	1.9	V
Low level input voltage	V_{IL}	CLK_INT, CLK_INC, FB_IN			0.35 x V_{DD}	V
High level input voltage	V_{IH}	CLK_INT, CLK_INC, FB_IN	0.65 x V_{DD}			V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DD} + 0.3	V
DC input signal voltage swing	$V_{IN-Diff}$	CLK_INT, CLK_INC	GND - 0.3	1.5	V_{DD} + 0.3	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLK_INT, CLK_INC, FB_IN	0.3		V_{DD} + 0.4	V
		AC - CLK_INT, CLK_INC, FB_IN	0.6		V_{DD} + 0.4	V
Output differential cross-voltage (note 4) .	V_{OX}		V_{DD} / 2 - 0.1		V_{DD} / 2 + 0.1	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DD}/2 - 0.15	V_{DD}/2	V_{DD} / 2 + 0.15	V
High level output current	I_{OH}				-9	mA
Low level output current	I_{OL}				9	mA
High Impedance Output Current	I_{OZ}	V_{DD}=1.9V, V_{OUT}=V_{DD} or GND			±10	mA
Operating free-air temperature	T_A		0		70	°C

Notes:
1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signal must be crossing.

Timing Requirements

T_A = 0 - 70°C Supply Voltage AVDD, VDD = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$freq_{op}$	1.8V±0.1V @ 25°C	125	500	MHz
Application Frequency Range	$freq_{App}$	1.8V±0.1V @ 25°C	160	400	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			15	µs

Switching Characteristics[1]

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output enable time	t_{en}	OE to any output			8	ns
Output disable time	t_{dis}	OE to any output			8	ns
Period jitter	$t_{jit\ (per)}$		-40		40	ps
Half-period jitter	$t_{jit(hper)}$		-75		75	ps
Input slew rate	$SLr1(i)$	Input Clock	1	2.5	4	v/ns
		Output Enable (OE), (OS)	0.5			v/ns
Output clock slew rate	$SLr1(o)$		1.5	2.5	3	v/ns
Cycle-to-cycle period jitter	$t_{jit(cc+)}$		0		40	ps
	$t_{jit(cc-)}$		0		-40	ps
Dynamic Phase Offset	$t_{( )dyn}$		-50		50	ps
Phase error	$t_{(phase\ error)}$[2]		-50	0	50	ps
Output to Output Skew	t_{skew}				40	ps
SSC modulation frequency			30.00		33	kHz
SSC clock input frequency deviation			0.00		-0.50	%

Notes:
1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{wH}/t_c, were the cycle (t_c) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage A_{VDD}, V_{DD} = 2.5V ± 0.2V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND	5			µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	C_L = 0pf @ 200MHz		250		mA
	I_{DDPD}	C_L = 0pf			100	µA
Output High Current	I_{OH}	V_{DD} = 2.3V, V_{OUT} = 1V	-18	-32		mA
Output Low Current	I_{OL}	V_{DD} = 2.3V, V_{OUT} = 1.2V	26	35		mA
High Impedance Output Current	I_{OZ}	V_{DD}=2.7V, Vout=V_{DD} or GND			±10	mA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 2.3V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1 mA	V_{DDQ} - 0.1			V
		V_{DDQ} = 2.3V, I_{OH} = -12 mA	1.7			V
Low-level output voltage	V_{OL}	V_{DD} = min to max I_{OL}=1 mA			0.1	V
		V_{DDQ} = 2.3V I_{OH}=12 mA			0.6	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}		3		pF
Output Capacitance[1]	C_{OUT}	V_{OUT} = GND or V_{DD}		3		pF

Recommended Operating Condition (see note 1)

T_A = 0 - 70°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}, A_{VDD}		2.3	2.5	2.7	V
Low level input voltage	V_{IL}	DDRT,DDRC		0.4	V_{DD}/2 - 0.18	V
High level input voltage	V_{IH}	DDRT,DDRC	V_{DD}/2 + 0.18	2.1		V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DD} + 0.3	V
Differential input signal voltage (note 3)	V_{ID}	DC - DDRT	0.36		V_{DD} + 0.6	V
		AC - DDRT	0.7		V_{DD} + 0.6	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DD}/2 - 0.15		V_{DD}/2 + 0.15	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DD}/2 - 0.2	V_{DD}/2	V_{DD}/2 + 0.2	V
High level output current	I_{OH}				-30	mA
Low level output current	I_{OL}				-30	mA
Operating free-air temperature	T_A		0		85	°C

Notes:
1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VT is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signal must be crossing.

Timing Requirements

T_A = 0 - =70°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$freq_{op}$	2.5V±0.2V @ 25°C	45	600	MHz
Application Frequency Range	$freq_{App}$	2.5V±0.2V @ 25°C	95	233	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			15	µs

Switching Characteristics[3]

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}[1]	BUF_IN to any output		3.5		ns
High-to low level propagation delay time	t_{PLL}[1]	BUF_IN to any output		3.5		ns
Period jitter	$T_{jit\ (per)}$	100MHz to 200MHz	-30		30	ps
Half-period jitter	t(jit_hper)	100MHz to 200MHz	-100		100	ps
Input clock slew rate	$t_{sl(i)}$		1		4	V/ns
Output clock slew rate	$t_{sl(o)}$		1		2	V/ns
Cycle to Cycle Jitter[1]	T_{cyc}-T_{cyc}	100MHz to 200MHz	-50		50	ps
Static Phase Offset	$t_{(static\ phase\ offset)}$[4]		-50	0	50	ps
Output to Output Skew	T_{skew}				40	ps

Notes:
1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{wH}/t_c, were the cycle (t_c) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.

General I²C serial interface information for the ICS9P935

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

.

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D4 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D5 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D4(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D4(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D5(H)			
RD	ReaD		
			ACK
			Data Byte Count = X
	ACK		
			Beginning Byte N
	ACK		
		X Byte	○
	○		○
	○		○
	○		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Notes:

1. The IDT clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support SMBus block read protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

I²C Table: Output Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Freq Detect	Low Frequency Detect PLL OFF Control	RW	OFF	ON	1
Bit 6	-	FB_IN/OUT	FB_OUT Control	RW	Disable	Enable	1
Bit 5	-	DDR_T5/C5	Output Control	RW	Disable	Enable	1
Bit 4	-	DDR_T4/C4	Output Control	RW	Disable	Enable	1
Bit 3	-	DDR_T3/C3	Output Control	RW	Disable	Enable	1
Bit 2	-	DDR_T2/C2	Output Control	RW	Disable	Enable	1
Bit 1	-	DDR_T1/C1	Output Control	RW	Disable	Enable	1
Bit 0	-	DDR_T0/C0	Output Control	RW	Disable	Enable	1

I²C Table: Group Skew Control Register

Byte 8		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		DDR Skw3	CLKIN to DDR Skew Control	RW	See Table 1: 7-Step Skew Programming Table		0
Bit 6	-		DDR Skw2		RW			0
Bit 5	-		DDR Skw1		RW			0
Bit 4	-		DDR Skw0		RW			0
Bit 3	-		DDR Skw3	CLKIN to DDR Skew Control	RW	See Table 2: 7-Step Skew Programming Table		0
Bit 2	-		DDR Skw2		RW			0
Bit 1	-		DDR Skw1		RW			0
Bit 0	-		DDR Skw0		RW			0

I²C Table: Revision ID and Vendor ID Register

Byte 10		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Revision_ID bit 3	Rev ID	RW	-	-	X
Bit 6	-		Revision_ID bit 2		RW	-	-	X
Bit 5	-		Revision_ID bit 1		RW	-	-	X
Bit 4	-		Revision_ID bit 0		RW	-	-	X
Bit 3	-		Vendor_ID bit3	Vendor ID	RW	-	-	0
Bit 2	-		Vendor_ID bit2		RW	-	-	0
Bit 1	-		Vendor_ID bit1		RW	-	-	0
Bit 0	-		Vendor_ID bit0		RW	-	-	1

I²C Table: Byte Count Register

Byte 15		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes		0
Bit 6	-		BC6		RW			0
Bit 5	-		BC5		RW			0
Bit 4	-		BC4		RW			0
Bit 3	-		BC3		RW			1
Bit 2	-		BC2		RW			1
Bit 1	-		BC1		RW			1
Bit 0	-		BC0		RW			1

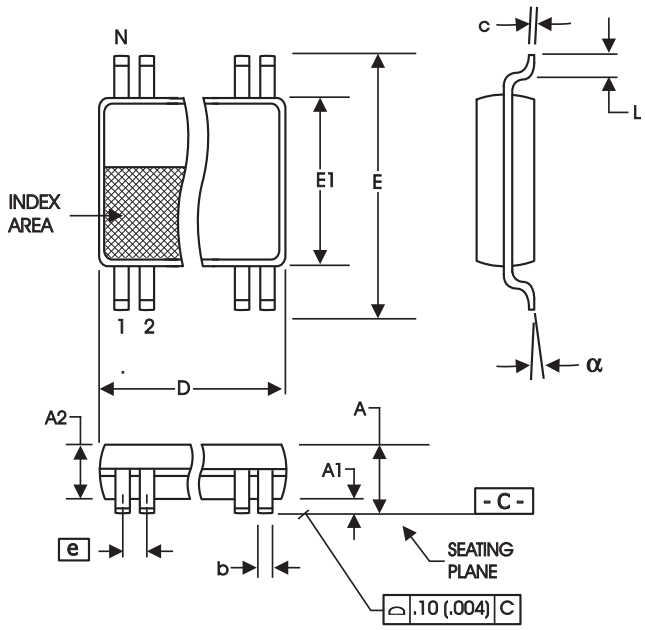
I2C Table: All other I2C Registers are Reserved

Table 1: 7-Steps Skew Programming Table

7 Step	11	10	01	00	LSB
11	600 ps	500 ps	400 ps	300 ps	
10	N/A	N/A	N/A	200 ps	
01	N/A	N/A	N/A	100 ps	
00	N/A	N/A	N/A	0.0 ps	
MSB					

Table 2: 7-Steps Skew Programming Table

7 Step	11	10	01	00	LSB
11	-600 ps	-500 ps	-400 ps	-300 ps	
10	N/A	N/A	N/A	-200 ps	
01	N/A	N/A	N/A	-100 ps	
00	N/A	N/A	N/A	0.0 ps	
MSB					



209 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

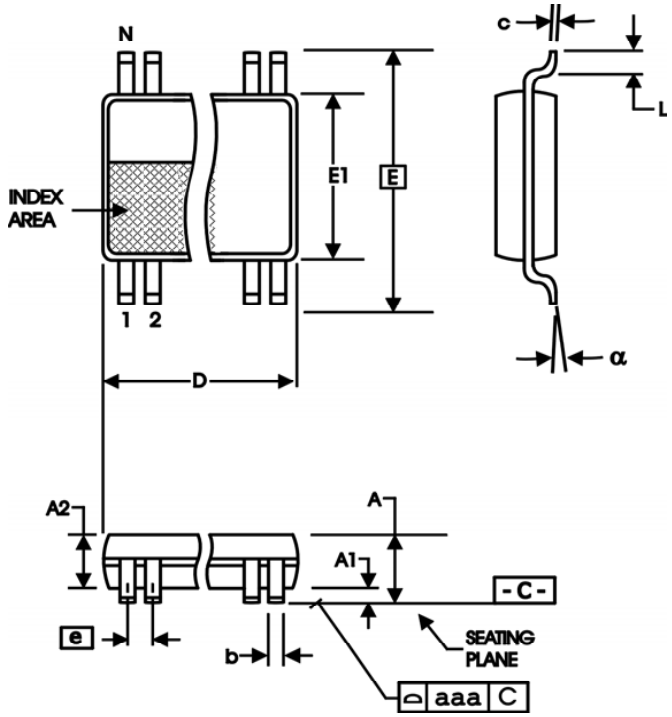
Ordering Information

ICS9P935yFLF-T

Example:

ICS XXXX y F LF- T

- **Designation for tape and reel packaging**
- **RoHS Compliant (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device



4.40 mm. Body, 0.65 mm. Pitch TSSOP

(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

ICS9P935yGLF-T

Example:

ICS XXXX y **G LF- T**

- **Designation for tape and reel packaging**
- **RoHS Compliant (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

Revision History

Rev.	Issue Date	Description	Page #
A	2/8/2007	Final Release.	-
B	6/4/2007	Fixed various typos.	-
C	6/14/2007	Added TSSOP Ordering Information.	12
D	6/20/2007	1. Updated Output Features: Max Frequency Supported. 2. Updated DDRI/DDRII Max Clock Frequency.	1 5, 8
E	8/16/2007	1. Updated Supply Voltage. 2. Updated Input High/Low Current Max.	 3
F	9/5/2007	Updated Electrical Specifications.	3-5
G	11/19/2007	Updated Serial Interface Information.	9
H	12/1/2008	Updated Pin Description.	2

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For Sales
800-345-7015
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408-284-6578
pcclockhelp@idt.com

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339

www.IDT.com

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