MOSFET - Power, Single N-Channel, μ8FL
60 V, 29.7 mΩ, 19 A

NVTFS030N06C

Features
- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVTFWS030N06C – Wettable Flank Option for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications
- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	19	A
		T_C = 100°C		13	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	23	W
		T_C = 100°C		11	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	6	A
		T_A = 100°C		4	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	2.5	W
		T_A = 100°C		1.2	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	86	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	19	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 4.6 A)			E_{AS}	11	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

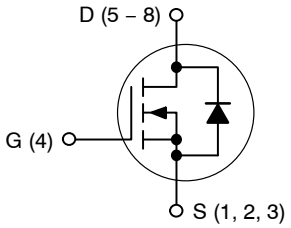
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	29.7 mΩ @ 10 V	19 A

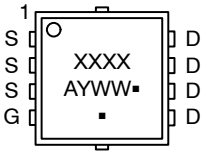
N−Channel

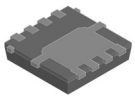


MARKING DIAGRAMS

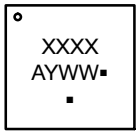


WDFN8 (μ8FL) CASE 511AB





WDFNW8 (Full−Cut μ8FL) CASE 515AN



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION
See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 4)	$R_{\theta JC}$	6.3	°C/W
Junction−to−Ambient − Steady State (Note 4)	$R_{\theta JA}$	60	

4. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, referenced to 25°C			32		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			10	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 13 μA		2.0		4.0	V
Negative Treshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 13 μA, referenced to 25°C			−7.9		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 3 A			24.7	29.7	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 3 A			8.5		S
Gate−Resistance	R_G	T_A = 25°C			1.5		Ω
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 30 V			255		pF
Output Capacitance	C_{oss}				173		
Reverse Transfer Capacitance	C_{rss}				4.4		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 3 A			4.7		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.1		
Gate−to−Source Charge	Q_{GS}				1.7		
Gate−to−Drain Charge	Q_{GD}				0.54		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 3 A, R_G = 6 Ω			5.7		ns
Rise Time	t_r				1.2		
Turn−Off Delay Time	$t_{d(off)}$				8.7		
Fall Time	t_f				2.3		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 3 A	T_J = 25°C		0.82	1.2	V
			T_J = 125°C		0.68		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, V_{DS} = 30 V, I_S = 3 A			21		ns
Charge Time	t_a				11		
Discharge Time	t_b				10		
Reverse Recovery Charge	Q_{RR}				9.7		nC

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

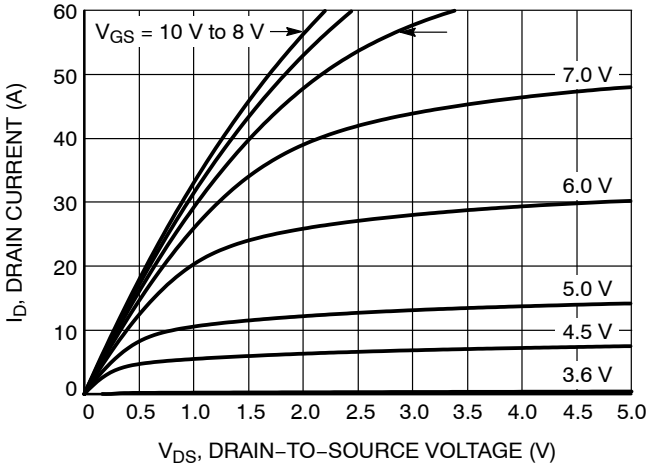


Figure 1. On−Region Characteristics

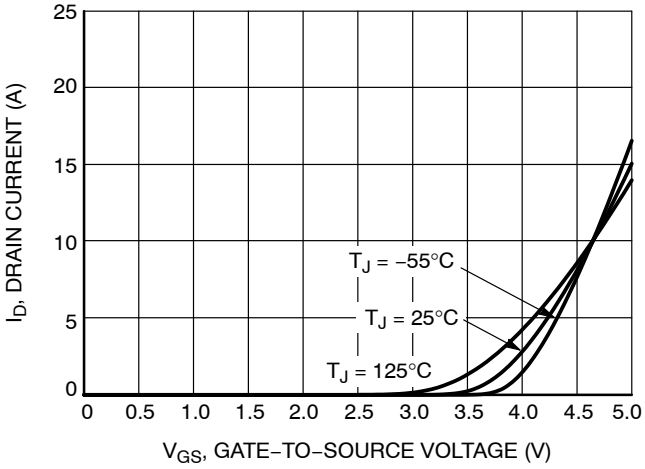


Figure 2. Transfer Characteristics

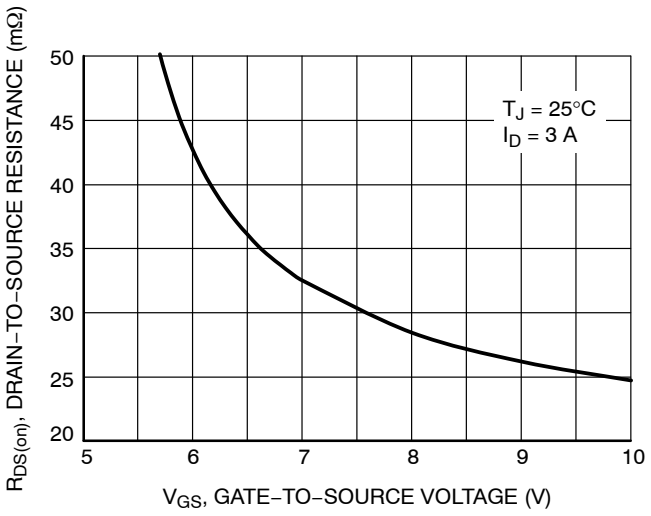


Figure 3. On−Resistance vs. Gate−to−Source Voltage

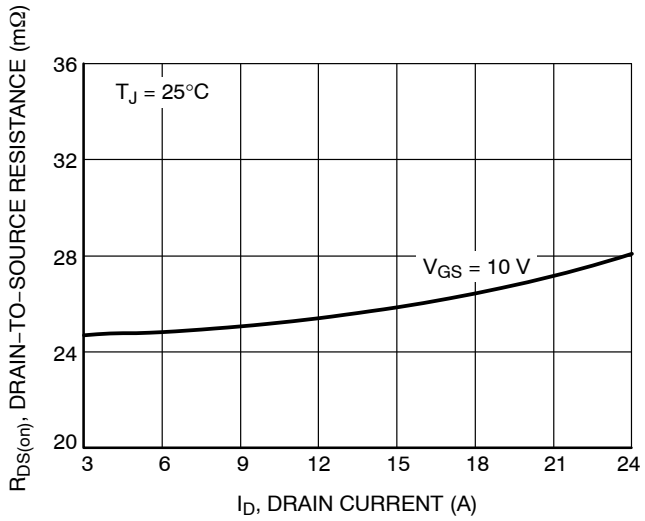


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

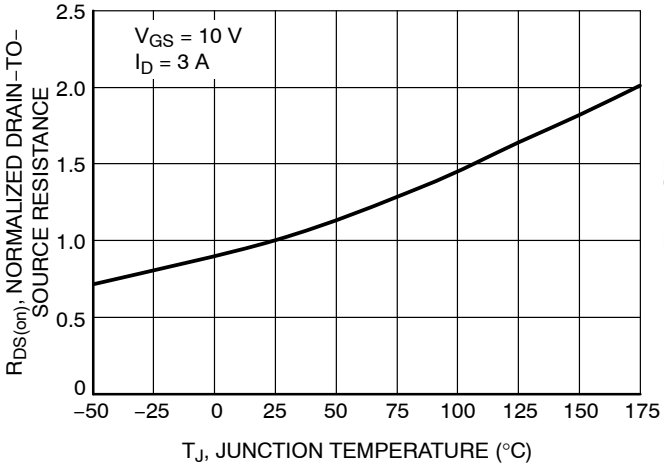


Figure 5. On−Resistance Variation with Temperature

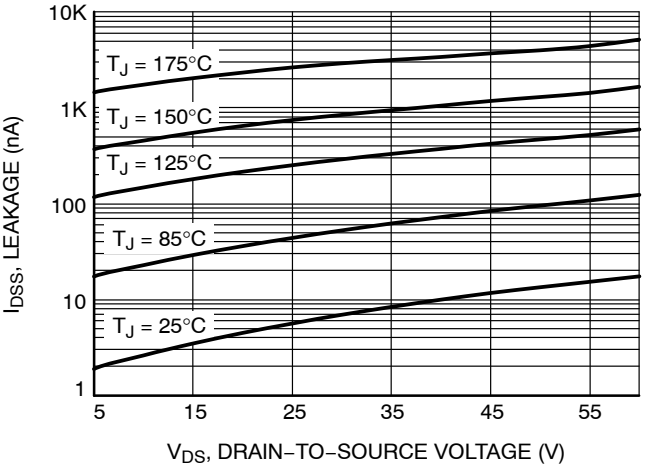


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

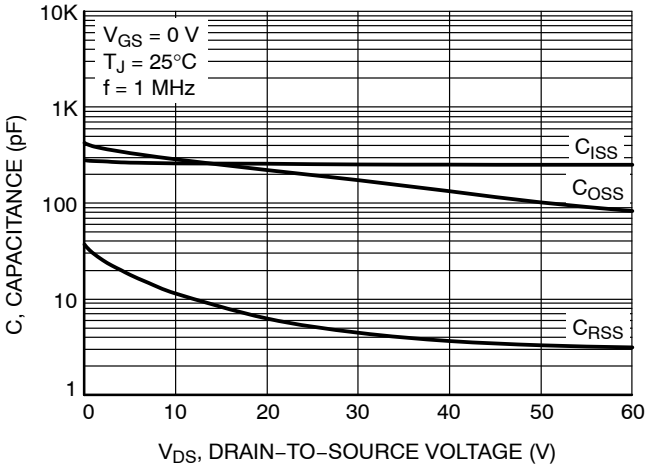


Figure 7. Capacitance Variation

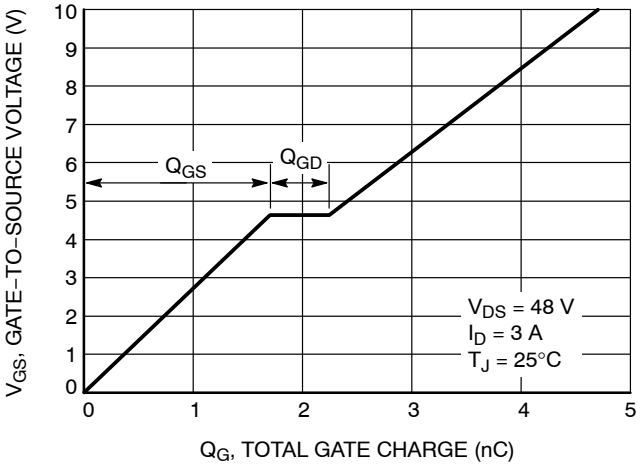


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

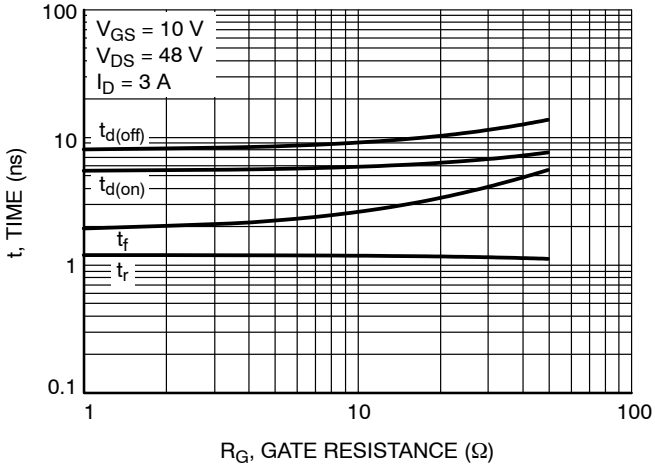


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

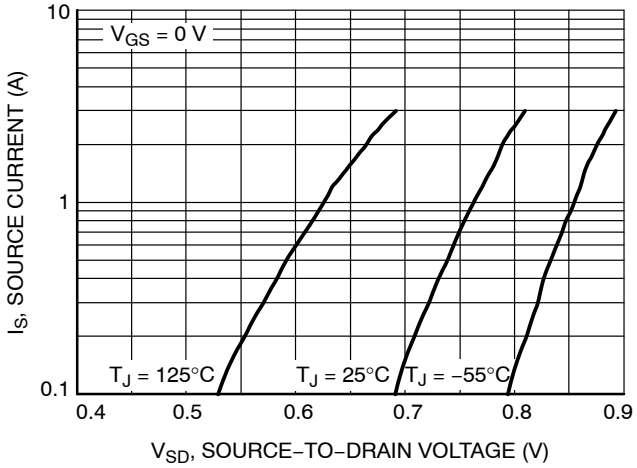


Figure 10. Diode Forward Voltage vs. Current

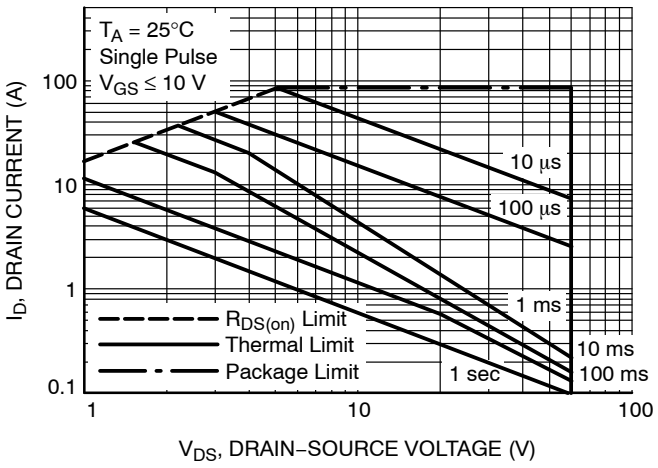


Figure 11. Safe Operating Area

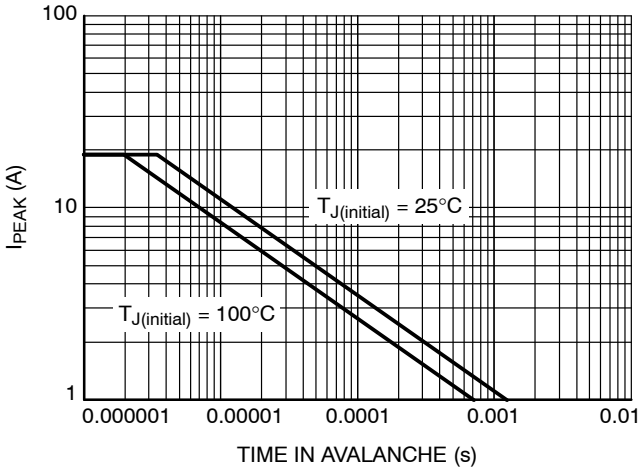


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

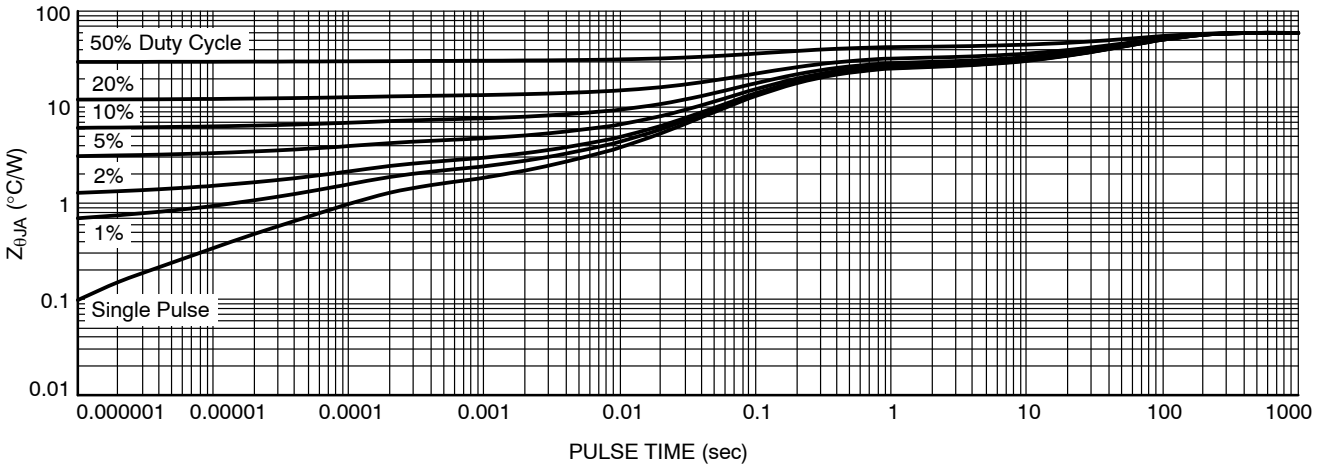


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVTFS030N06CTAG	30NC	μ8FL (Pb−Free)	1500 / Tape & Reel
NVTFWS030N06CTAG	30NW	μ8FL (Pb−Free, Wettable Flanks)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

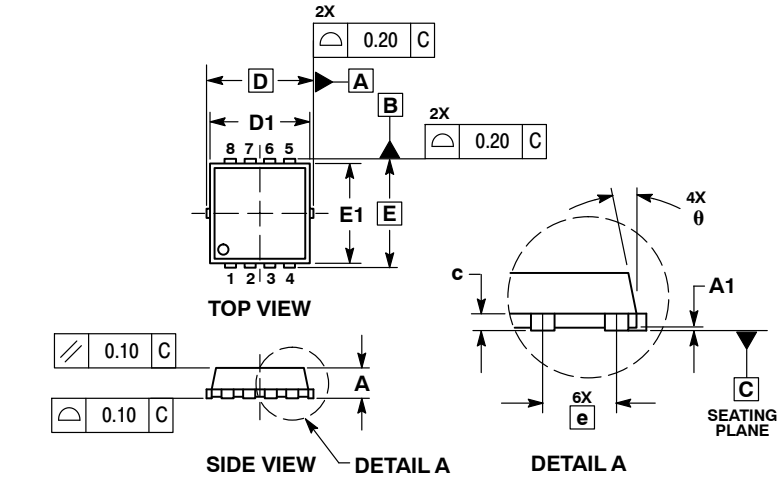
ON Semiconductor®



WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

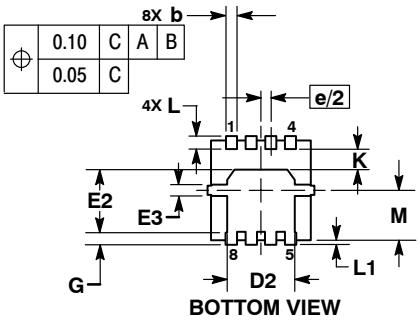
DATE 23 APR 2012

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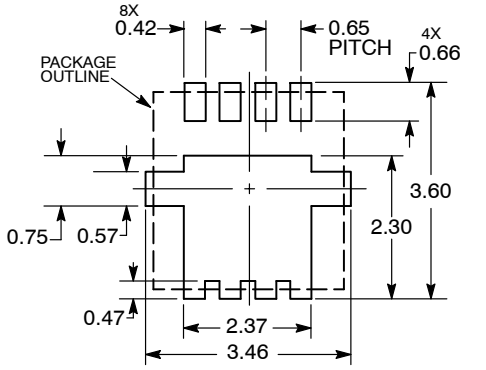


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D		3.30 BSC			0.130 BSC	
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E		3.30 BSC			0.130 BSC	
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e		0.65 BSC			0.026 BSC	
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °



SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

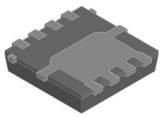
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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 1 OF 1**

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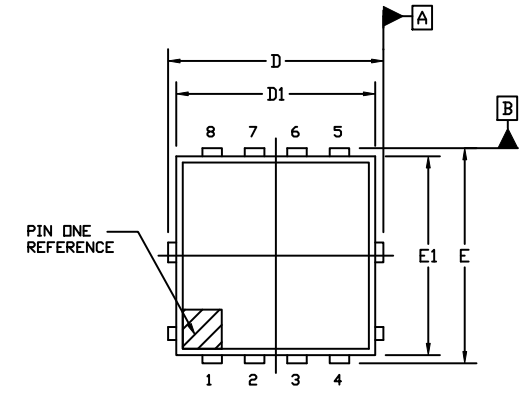
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

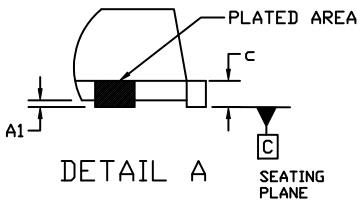


WDFNW8 3.3x3.3, 0.65P (Full−Cut μ8FL WF)
CASE 515AN
ISSUE O

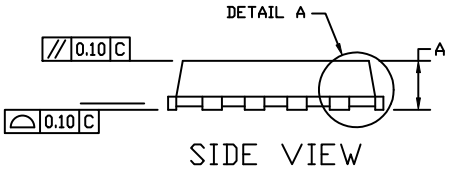
DATE 25 AUG 2020



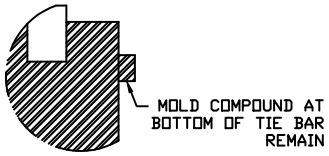
TOP VIEW



DETAIL A



SIDE VIEW

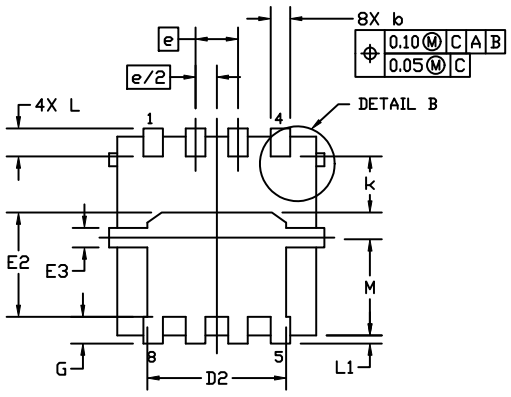


DETAIL B

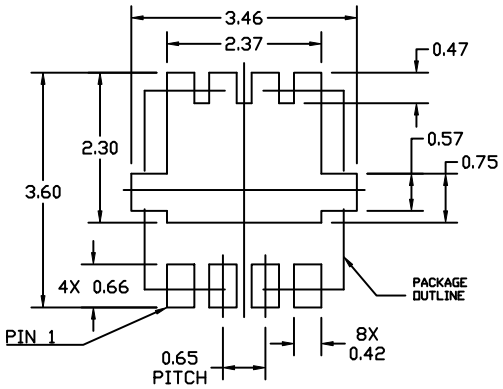
NOTES:

1. DIMENSIONING AND TOLERANCING PER.ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



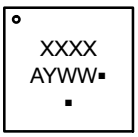
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON24556H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**WDFNW8 3.3x3.3, 0.65P (Full−Cut μ8FL WF)**	**PAGE 1 OF 1**

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