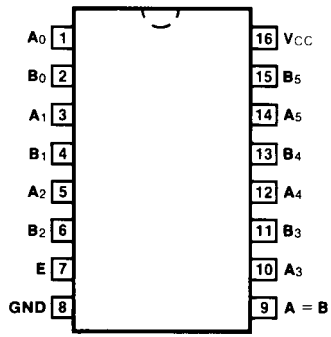
93S46 01054?

HIGH SPEED 6-BIT IDENTITY COMPARATOR

DESCRIPTION — The '46 is a very high speed 6-bit identity comparator. The device compares two words of up to six bits and indicates identity in less than 12 ns. It is easily expandable to any word length by using either serial or parallel expansion techniques. When the Enable input (E) is LOW, it forces the output LOW.

- **COMPARES TWO 6-BIT WORDS IN 12 ns**
- **EASILY EXPANDABLE TO ANY WORD SIZE**
- **ACTIVE HIGH ENABLE FOR FAST RIPPLE EXPANSION**

CONNECTION DIAGRAM
PINOUT A



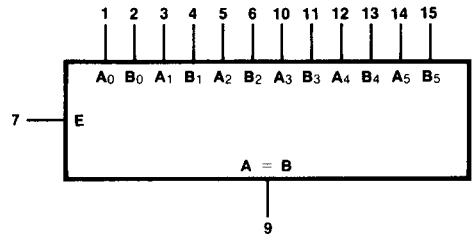
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	93S46PC		9B
Ceramic DIP (D)	A	93S46DC	93S46DM	6B
Flatpak (F)	A	93S46FC	93S46FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93S (U.L.) HIGH/LOW
A_0 — A_5	Word A Inputs	1.25/1.25
B_0 — B_5	Word B Inputs	1.25/1.25
E	Enable Input (Active HIGH)	1.25/1.25
A = B	A Equal to B Output	25/12.5

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '46 is a very high speed 6-bit identity comparator. The A = B output is HIGH when the Enable (E) is HIGH and the two 6-bit words are equal. Equality is determined by Exclusive-NOR circuits which individually compare the equivalent bits from each word. When any two of the equivalent bits from each word have different logic levels, the A = B output is LOW.

$$(A = B) = \overline{(A_0 \oplus B_0)} \bullet \overline{(A_1 \oplus B_1)} \bullet \overline{(A_2 \oplus B_2)} \bullet \overline{(A_3 \oplus B_3)} \bullet \overline{(A_4 \oplus B_4)} \bullet \overline{(A_5 \oplus B_5)} \bullet E$$

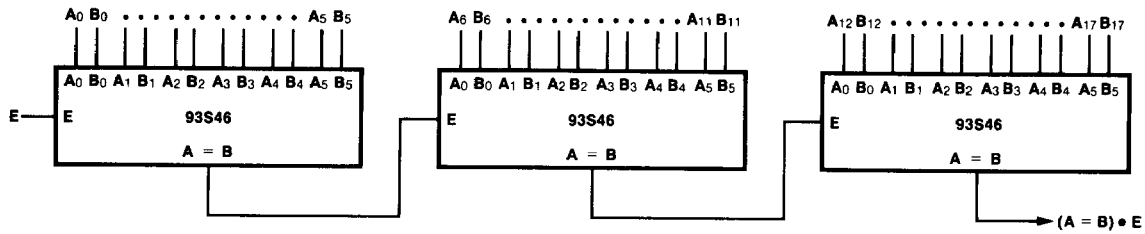
An active HIGH Enable (E) provides a means of fast ripple expansion. By connecting the A = B output of the first stage of the comparator to the enable of the next stage, the comparator can be expanded in 6-bit increments at an additional 4.5 ns per stage. An even faster expansion technique is achieved by connecting the A = B outputs to a Schottky NAND gate. This method compares two words of up to 78 bits each in 15 ns (typical) using the '133 13-input Schottky NAND gate.

TRUTH TABLE

INPUTS		OUTPUT
E	A_n, B_n	A = B
L	$A_n = B_n$	L
L	$A_n \neq B_n$	L
H	$A_n \neq B_n$	L
H	$A_n = B_n$	H

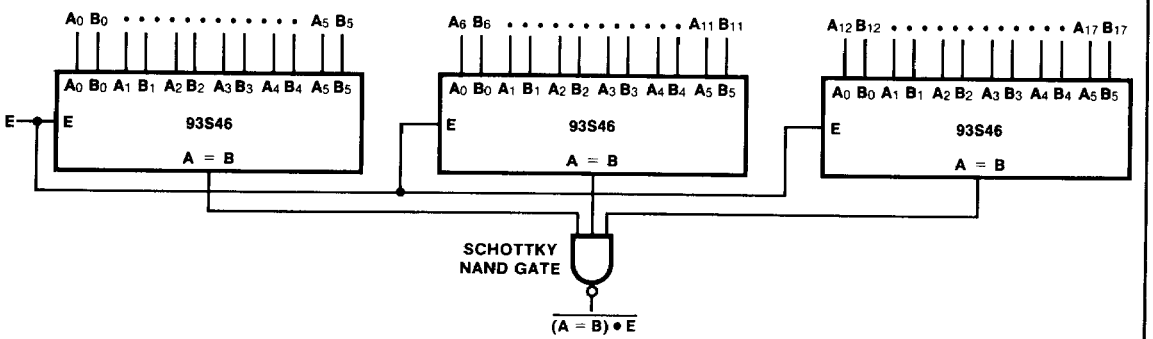
H = HIGH Voltage Level
L = LOW Voltage Level

RIPPLE EXPANSION



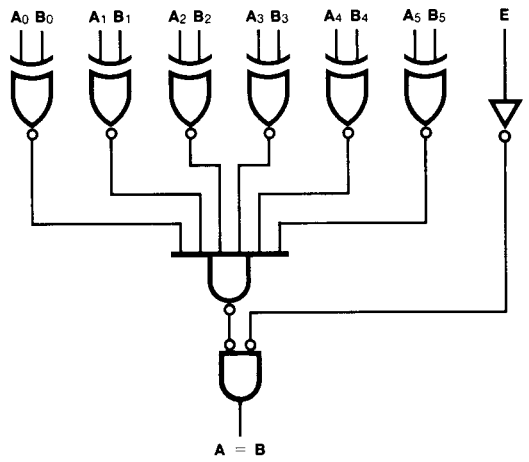
NOTE: This simple method of expansion adds 4.5 ns for each additional '46 used.

PARALLEL EXPANSION



NOTE: This method of expansion adds one gate delay (≈3 ns) to the '46, independent of the word length that is compared.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93S		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		70	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93S C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	3.0 3.0	17 17	ns	E = 4.5 V, Other Inputs = 4.5 V, Test each input individually, Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	3.0 3.0	14 15	ns	E = 4.5 V, Other Inputs = Gnd, Test each input individually, Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay E to A = B	2.0 2.0	10 10	ns	A_n = B_n Figs. 3-1, 3-5