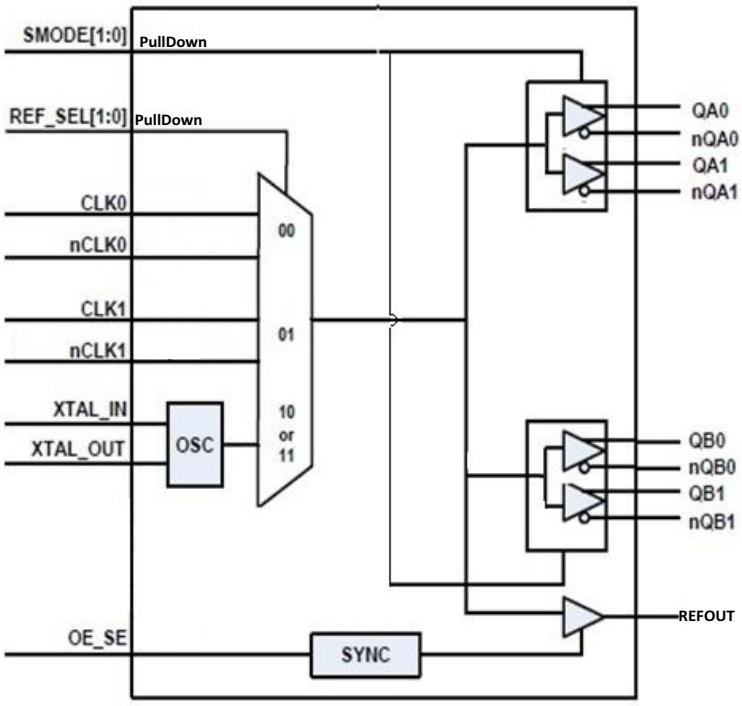
## General Description

The 8T39S04A is a high-performance clock fanout buffer. The input clock can be selected from two differential inputs or one crystal input. The internal oscillator circuit is automatically disabled if the crystal input is not selected. The crystal pin can be driven by a single-ended clock.The selected signal is distributed to four differential outputs which can be configured as LVPECL, LVDS or HSCL outputs. In addition, an LVCMOS output is provided. All outputs can be disabled into a high-impedance state. The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. The outputs are at a defined level when inputs are open or tied to ground. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

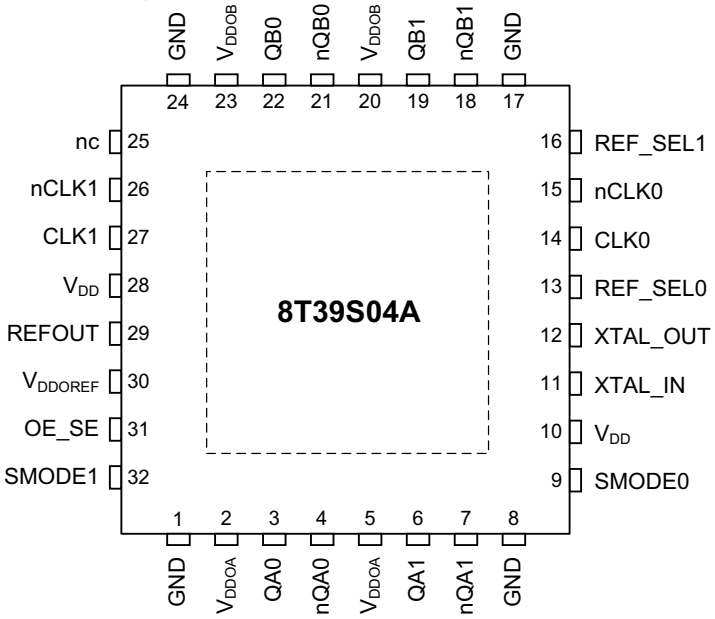
## Block Diagram




## Features

- Two differential reference clock input pairs
- Differential input pairs can accept the following input levels: LVPECL, LVDS, HCSL, HSTL and Single-ended
- Crystal Oscillator Interface
- Crystal input frequency range: 10MHz to 40MHz
- Maximum Output Frequency
  LVPECL - 2GHz
  LVDS - 2GHz
  HCSL - 250MHz
  LVCMOS - 250MHz
- Two banks, each has two differential output pairs that can be configured as LVPECL or LVDS or HCSL
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: 80ps (maximum), Bank A and Bank B at the same output level
- Part-to-part skew: 200ps (typical), design target
- Additive RMS phase jitter @ 156.25MHz, (12kHz - 20MHz): 34.7fs (typical), 3.3V/ 3.3V
- Supply voltage modes:
  $V_{DD}/V_{DDO}$
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

## Pin Assignment




**32-pin, 5mm x 5mm VFQFN Package**

# Pin Description and Pin Characteristic Table

**Table 1. Pin Descriptions**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | GND | Power | | Power supply ground. |
| 2 | $V_{DDOA}$ | Power | | Output supply pin for Bank QA outputs. |
| 3 | QA0 | Output | | Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 4 | nQA0 | Output | | Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 5 | $V_{DDOA}$ | Power | | Output supply pin for Bank QA outputs. |
| 6 | QA1 | Output | | Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 7 | nQA1 | Output | | Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 8 | GND | Power | | Power supply ground. |
| 9 | SMODE0 | Input | Pulldown | Output driver select for Bank A and Bank B outputs. See Table 3D for function. LVCMOS/LVTTL interface levels. |
| 10 | $V_{DD}$ | Power | | Power supply pin. |
| 11 | XTAL_IN | Input | | Crystal oscillator interface. |
| 12 | XTAL_OUT | Output | | Crystal oscillator interface. |
| 13 | REF_SEL0 | Input | Pulldown | Input clock selection. LVCMOS/LVTTL interface levels. See Table 3A for function. |
| 14 | CLK0 | Input | Pullup/ Pulldown | Non-inverting differential clock. Internally biased to $0.33V_{DD}$. |
| 15 | nCLK0 | Input | Pullup/ Pulldown | Inverting differential clock. Internal resistor bias to $0.4V_{DD}$. |
| 16 | REF_SEL1 | Input | Pulldown | Input clock selection. LVCMOS/LVTTL interface levels. See Table 3A for function. |
| 17 | GND | Power | | Power supply ground. |
| 18 | nQB1 | Output | | Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 19 | QB1 | Output | | Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 20 | $V_{DDOB}$ | Power | | Output supply pin for Bank QB outputs. |
| 21 | nQB0 | Output | | Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 22 | QB0 | Output | | Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 23 | $V_{DDOB}$ | Power | | Output supply pin for Bank QB outputs. |
| 24 | GND | Power | | Power supply ground. |
| 25 | nc | Unused | | No connect pin. |
| 26 | nCLK1 | Input | Pullup/ Pulldown | Inverting differential clock. Internal resistor bias to $0.4V_{DD}$. |
| 27 | CLK1 | Input | Pullup/ Pulldown | Non-inverting differential clock. Internally biased to $0.33V_{DD}$. |
| 28 | $V_{DD}$ | Power | | Power supply pin. |
| 29 | REFOUT | Output | | Single-ended reference clock output. LVCMOS/LVTTL interface levels. |
| 30 | $V_{DDOREF}$ | Power | | Output supply pin for REFOUT output. |
| 31 | OE_SE | Input | Pulldown | Output enable. LVCMOS/LVTTL interface levels. See Table 3B. |
| 32 | SMODE1 | Input | Pulldown | Output driver select for Bank A and Bank B outputs. See Table 3D for function. LVCMOS/LVTTL interface levels. |
| 0 | ePAD | Power | | Connect ePAD to ground to ensure proper heat dissipation. |

NOTE: *Pulldown* and *Pullup* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

**Table 2. Pin Characteristics**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | OE_SE, SMODE[1:0], REF_SEL[1:0] | | | 2 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | | 50 | | kΩ |
| $R_{PULLUP}$ | Input Pullup Resistor | CLK0, CLK1 | | | 100 | | kΩ |
| | | nCLK0, nCLK1 | | | 75 | | kΩ |
| $C_{PD}$ | Power Dissipation Capacitance | REFOUT | $V_{DDOREF}$ = 3.465V | | 5.3 | | pF |
| | | | $V_{DDOREF}$ = 2.625V | | 6.3 | | pF |
| $R_{OUT}$ | Output Impedance | REFOUT | $V_{DDOREF}$ = 3.3V | | 52 | | Ω |
| | | | $V_{DDOREF}$ = 2.5V | | 63 | | Ω |

# Function Tables

**Table 3A. REF_SELx Function Table**

| Control Input REF_SEL[1:0] | Selected Input Reference Clock |
|---|---|
| 00 (default) | CLK0, nCLK0 |
| 01 | CLK1, nCLK1 |
| 10 | XTAL |
| 11 | XTAL |

**Table 3B. OE_SE Function Table**

| OE_SE | REFOUT |
|---|---|
| 0 (default) | High-Impedance |
| 1 | Enabled |

NOTE: Synchronous output enable to avoid clock glitch.

**Table 3C. Input/Output Operation Table, OE_SE**

| Input Status | | | Output State |
|---|---|---|---|
| OE_SE | REF_SEL [1:0] | CLKx and nCLKx | REFOUT |
| 0 (default) | Don't care | Don't Care | High Impedance |
| 1 | 10 or 11 | Don't Care | Fanout Crystal Oscillator |
| 1 | 00 (default) | CLK0 and nCLK0 are both open circuit | Logic Low |
| | | CLK0 and nCLK0 are tied to ground | Logic Low |
| | | CLK0 is high, nCLK0 is low | Logic High |
| | | CLK0 is low, nCLK0 is high | Logic Low |
| 1 | 01 | CLK1 and nCLK1 are both open circuit | Logic Low |
| | | CLK1 and nCLK1 are tied to ground | Logic Low |
| | | CLK1 is high, nCLK1 is low | Logic High |
| | | CLK1 is low, nCLK1 is high | Logic Low |

**Table 3D. Output Level Selection Table, QX[0:1], nQX[0:1]**

| SMODE1 | SMODE0 | Output Type |
|---|---|---|
| 0 | 0 | LVPECL (default) |
| 0 | 1 | LVDS |
| 1 | 0 | HCSL |
| 1 | 1 | High-Impedance |

NOTE: X denotes A and B.

**Table 3E. Input/Output Operation Table, SMODE[1:0]**

| Input Status | | | Output State |
|---|---|---|---|
| **SMODE[1:0]** | **REF_SEL[1:0]** | **CLKx and nCLKx** | **QA[1:0], nQA[1:0]** |
| 11 | Don't care | Don't Care | High Impedance |
| 00, 01 or 10 | 10 or 11 | Don't Care | Fanout crystal oscillator |
| 00, 01 or 10 | 00 (default) | CLK0 and nCLK0 are both open circuit | QA[1:0] = Low<br>nQA[1:0] = High |
| | | CLK0 and nCLK0 are tied to ground | QA[1:0] = Low<br>nQA[1:0] = High |
| | | CLK0 is high, nCLK0 is low | QA[1:0] = High<br>nQA[1:0] = Low |
| | | CLK0 is low, nCLK0 is high | QA[1:0] = Low<br>nQA[1:0] = High |
| 00, 01 or 10 | 01 | CLK1 and nCLK1 are both open circuit | QA[1:0] = Low<br>nQA[1:0] = High |
| | | CLK1 and CLK1 are tied to ground. | QA[1:0] = Low<br>nQA[1:0] = High |
| | | CLK1 is high, nCLK1 is low | QA[1:0] = High<br>nQA[1:0] = Low |
| | | CLK1 is low, nCLK1 is high | QA[1:0] = Low<br>nQA[1:0] = High |

**Table 3F. Input/Output Operation Table, SMODE[1:0]**

| Input Status | | | Output State |
|---|---|---|---|
| **SMODE[1:0]** | **REF_SEL[1:0]** | **CLKx and nCLKx** | **QB[1:0], nQB[1:0]** |
| 11 | Don't care | Don't Care | High Impedance |
| 00, 01 or 10 | 10 or 11 | Don't Care | Fanout Crystal Oscillator |
| 00, 01 or 10 | 00 (default) | CLK0 and nCLK0 are both open circuit | QB[1:0] = Low<br>nQB[1:0] = High |
| | | CLK0 and nCLK0 are tied to ground | QB[1:0] = Low<br>nQB[1:0] = High |
| | | CLK0 is high, nCLK0 is low | QB[1:0] = High<br>nQB[1:0] = Low |
| | | CLK0 is low, nCLK0 is high | QB[1:0] = Low<br>nQB[1:0] = High |
| 00, 01 or 10 | 01 | CLK1 and nCLK1 are both open circuit | QB[1:0] = Low<br>nQB[1:0] = High |
| | | CLK1 and nCLK1 are tied to ground | QB[1:0] = Low<br>nQB[1:0] = High |
| | | CLK1 is high, nCLK1 is low | QB[1:0] = High<br>nQB[1:0] = Low |
| | | CLK1 is low, nCLK1 is high | QB[1:0] = Low<br>nQB[1:0] = High |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$<br>XTAL_IN<br>Other Inputs | <br>0V to 2V<br>-0.5V to $V_{DD}$ + 0.5V |
| Outputs, $V_O$, (HCSL, LVCMOS) | -0.5V to $V_{DDOX}$[1] + 0.5V |
| Outputs, $I_O$, (LVPECL)<br>Continuous Current<br>Surge Current | <br>50mA<br>100mA |
| Outputs, $I_O$, (LVDS)<br>Continuous Current<br>Surge Current | <br>10mA<br>15mA |
| Junction Temperature, $T_J$ | 125°C |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE 1. $V_{DDOX}$ denotes $V_{DDOA}$, $V_{DDOB}$ and $V_{DDOREF}$.

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{DD} = V_{DDOA} = V_{DDOB} = V_{DDOREF}$ = 3.3V±5%, GND = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDOA}$, $V_{DDOB}$, $V_{DDOREF}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | SMODE[1:0] = 01 | | 80 | 100 | mA |
| $I_{DDOA} + I_{DDOB}$ | Output Supply Current[1] | SMODE[1:0] = 01 | | 80 | 100 | mA |
| $I_{EE}$ | Power Supply Current | SMODE[1:0] = 00 (default) | | 110 | 130 | mA |
| $I_{DD}$ | Power Supply Current | SMODE[1:0] = 10 | | 80 | 100 | mA |
| $I_{DDOA} + I_{DDOB}$ | Output Power Supply Current[2] | SMODE[1:0] = 10 | | 50 | 60 | mA |

NOTE 1. Differential outputs are terminated with 100Ω.

NOTE 2. Differential outputs are running at 250MHz and floating.

**Table 4B. Power Supply DC Characteristics,** $V_{DD}$ = 3.3V±5%, $V_{DDOA}$ = $V_{DDOB}$ = $V_{DDOREF}$ = 2.5V±5%, GND = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDOA}$, $V_{DDOB}$, $V_{DDOREF}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | SMODE[1:0] = 01 | | 80 | 100 | mA |
| $I_{DDOA}$ + $I_{DDOB}$ | Output Supply Current[1] | SMODE[1:0] = 01 | | 80 | 100 | mA |
| $I_{EE}$ | Power Supply Current | SMODE[1:0] = 00 (default) | | 110 | 130 | mA |
| $I_{DD}$ | Power Supply Current | SMODE[1:0] = 10 | | 80 | 100 | mA |
| $I_{DDOA}$ + $I_{DDOB}$ | Output Power Supply Current[2] | SMODE[1:0] = 10 | | 40 | 50 | mA |

NOTE 1. Differential outputs are terminated with 100Ω.

NOTE 2. Differential outputs are running at 250MHz and floating.

**Table 4C. Power Supply DC Characteristics,** $V_{DD}$ = $V_{DDOA}$ = $V_{DDOB}$ = $V_{DDOREF}$ = 2.5V±5%, GND = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{DDOA}$, $V_{DDOB}$, $V_{DDOREF}$ | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | SMODE[1:0] = 01 | | 70 | 85 | mA |
| $I_{DDOA}$ + $I_{DDOB}$ | Output Supply Current[1] | SMODE[1:0] = 01 | | 80 | 95 | mA |
| $I_{EE}$ | Power Supply Current | SMODE[1:0] = 00 (default) | | 95 | 115 | mA |
| $I_{DD}$ | Power Supply Current | SMODE[1:0] = 10 | | 70 | 80 | mA |
| $I_{DDOA}$ + $I_{DDOB}$ | Output Power Supply Current[2] | SMODE[1:0] = 10 | | 40 | 50 | mA |

NOTE 1. Differential outputs are terminated with 100Ω.

NOTE 2. Differential outputs are running at 250MHz and floating.

**Table 4D. LVCMOS/LVTTL DC Characteristics,**
$V_{DD}$ = 3.3V±5%, 2.5V±5%, $V_{DDOREF}$ = = 3.3V±5% or 2.5V±5%, GND = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | OE_SE, SMODE[1:0], REF_SEL[1:0] | $V_{DD}$ = 3.3V±5% | 2 | | $V_{DD}$ + 0.3 | V |
| | | | $V_{DD}$ = 2.5V±5% | 1.7 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | OE_SE, SMODE[1:0], REF_SEL[1:0] | $V_{DD}$ = 3.3V±5% | -0.3 | | 0.8 | V |
| | | | $V_{DD}$ = 2.5V±5% | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input High Current | OE_SE, SMODE[1:0], REF_SEL[1:0] | $V_{DD}$ = $V_{IN}$ = 3.465V or 2.625V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | OE_SE, SMODE[1:0], REF_SEL[1:0] | $V_{DD}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -5 | | | µA |
| $V_{OH}$ | Output High Voltage | REFOUT | $V_{DDOREF}$ = 3.3V±5%: $I_{OH}$ = -1mA | 2.6 | | | V |
| | | | $V_{DDOREF}$ = 2.5V±5%: $I_{OH}$ = -1mA | 1.8 | | | V |
| $V_{OL}$ | Output Low Voltage | REFOUT | $V_{DDOREF}$ = 3.3V±5% or 2.5V±5%: $I_{OL}$ = 1mA | | | 0.5 | V |

**Table 4E. Differential DC Characteristics,** $V_{DD}$ = 3.3V±5% or 2.5V±5%, GND = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK[1:0], nCLK[1:0] | $V_{DD}$ = $V_{IN}$ = 3.465V or 2.625V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK[1:0], nCLK[1:0] | $V_{DD}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage[1] | | | 0.240 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage[1, 2] | | | GND + 0.5 | | $V_{DD}$ – 0.85 | V |

NOTE 1. Input voltage should not be less than -0.3V and greater than $V_{DD}$.

NOTE 2. Common mode voltage is defined as the crosspoint.

**Table 4F. LVPECL DC Characteristics,** $V_{DDOA} = V_{DDOB}$ = 3.3V±5%, GND = 0V, $T_A$ = -40°C to 85°C[1]

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage[2] | | $V_{DDOX}$ – 1.4 | | $V_{DDOX}$ – 0.8 | V |
| $V_{OL}$ | Output Low Voltage[2] | | $V_{DDOX}$ – 2.0 | | $V_{DDOX}$ – 1.6 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1. $V_{DDOX}$ denotes $V_{DDOA}$ and $V_{DDOB}$.
NOTE 2. Outputs terminated with 50Ω to $V_{DDOX}$ – 2V.

**Table 4G. LVPECL DC Characteristics,** $V_{DDOA} = V_{DDOB}$ = 2.5V±5%, GND = 0V, $T_A$ = -40°C to 85°C[1]

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage[2] | | $V_{DDOX}$ – 1.4 | | $V_{DDOX}$ – 0.8 | V |
| $V_{OL}$ | Output Low Voltage[2] | | $V_{DDOX}$ – 2.0 | | $V_{DDOX}$ – 1.6 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.4 | | 1.0 | V |

NOTE 1. $V_{DDOX}$ denotes $V_{DDOA}$ and $V_{DDOB}$.
NOTE 2. Outputs terminated with 50Ω to $V_{DDOX}$ – 2V.

**Table 4H. LVDS DC Characteristics,** $V_{DDOA} = V_{DDOB}$ = 3.3V±5%, GND = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 247 | | 454 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | 50 | | mV |
| $V_{OS}$ | Offset Voltage | | 1.025 | | 1.375 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | 50 | | mV |

**Table 4I. LVDS DC Characteristics,** $V_{DDOA} = V_{DDOB}$ = 2.5V±5%, GND = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 247 | | 454 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | 50 | | mV |
| $V_{OS}$ | Offset Voltage | | 1.025 | | 1.375 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | 50 | | mV |

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | | Fundamental | | |
| Frequency | | 10 | | 40 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Capacitive Loading ($C_L$) | | | 12 | 18 | pF |

## AC Electrical Characteristics

**Table 4: AC Characteristics,** $V_{DD} = V_{DDOA} = V_{DDOB} = V_{DDOREF}$ = 3.3V±5%, GND = 0V, $T_A$ = -40°C to 85°C[1, 2]

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | LVDS, LVPECL Outputs | | | | 2000 | MHz |
| | | HCSL Outputs | | | | 250 | MHz |
| | | REFOUT | | | | 250 | MHz |
| $t_{jit}$ | Buffer Additive Phase Jitter, RMS: Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01 | | Clock Frequency = 156.25MHz; Input Clock from 8T49NS010, Input Clock Jitter = 86.6fs; SMODEA/B[1:0] = 00 | | 34.7 | | fs |
| NF | Noise Floor | LVPECL Outputs | Offset Freq. >10MHz; 156.25MHz Clock Freq. | | -159.1 | | dBc/Hz |
| | | LVDS Outputs | | | -157.0 | | dBc/Hz |
| | | HCSL Outputs | | | -156.0 | | dBc/Hz |
| tjit(Ø) | RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz | | REF_SEL[1:0] = 10 or 11[3] | | 0.176 | | ps |
| $t_{PD}$ | Propagation Delay[4] | CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs | SMODEA/B[1:0] = 00 | 0.28 | | 0.75 | ns |
| | | | SMODEA/B[1:0] = 01 | 0.28 | | 0.75 | ns |
| | | | SMODEA/B[1:0] = 10 | 0.90 | | 2.65 | ns |
| *t*sk(o) | Output Skew[5, 6] | | | | | 80 | ps |
| *t*sk(pp) | Part-to-Part Skew[6,, 7] | | | | 200 | | ps |
| $V_{OH}$ | Voltage High[8, 9] | HCSL Outputs | $T_A$ = 25°C, DC Measurement, $R_T$ = 50Ω to GND $C_L \leq$ 5pF | 520 | | 920 | mV |
| $V_{OL}$ | Voltage Low[8, 10] | HCSL Outputs | | -150 | | +150 | mV |
| $V_{CROSS}$ | Absolute Crossing Voltage[8, 11, 12] | HCSL Outputs | $R_T$ = 50Ω to GND $C_L \leq$ 5pF | 160 | | 460 | mV |
| $\Delta V_{CROSS}$ | Total Variation of $V_{CROSS}$ over all Edges[8, 11, 13] | HCSL Outputs | | | | 140 | mV |
| | Rise/Fall Edge Rate[3, 14, 15] | HCSL Outputs | | 0.6 | | 4.0 | V/ns |
| $t_R$ / $t_F$ | Output Rise/Fall Time | LVPECL Outputs | 20% to 80% | | 150 | 300 | ps |
| | | LVDS Outputs | 20% to 80% | | 150 | 300 | ps |
| | | HCSL Outputs | 20% to 80% | | 400 | 750 | ps |
| | | REFOUT | 20% to 80% | | 450 | 750 | ps |
| odc | Output Duty Cycle[16] | | with Crystal Input | 45 | | 55 | % |
| | | | with External 50%/ 50% Duty Cycle Clock Input | 45 | | 55 | % |
| $MUX_{-ISOLATION}$ | MUX Isolation | | 156.25MHz | | 75 | | dB |

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. All LVDS and LVPECL parameters characterized up to 1.5GHz. HCSL parameters characterized up to 250MHz.

NOTE 3. Measurement taken from differential waveform.

NOTE 4. Measured from the differential input crosspoint to the differential output crosspoint.

NOTE 5. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.

NOTE 6. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 7. Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross-point.

NOTE 8. Measurement taken from single-ended waveform.

NOTE 9. Defined as the maximum instantaneous voltage including overshoot.

NOTE 10. Defined as the minimum instantaneous voltage including undershoot.

NOTE 11. Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

NOTE 12. Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement.

NOTE 13. Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

NOTE 14. Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

NOTE 15. Measured at 100MHz.

NOTE 16. Measured for the following frequencies: 25MHz, 100MHz, 125MHz, 156.25MHz, 312.5MHz, 400MHz, and 644.5313MHz.

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**Table 5: AC Characteristics,** $V_{DD}$ = 3.3V±5%, $V_{DDOA}$ = $V_{DDOB}$ = $V_{DDOREF}$ = 2.5V±5%, GND = 0V, $T_A$ = -40°C to 85°C [1, 2]

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | LVDS, LVPECL Outputs | | | | 2000 | MHz |
| | | HCSL Outputs | | | | 250 | MHz |
| | | REFOUT | | | | 250 | MHz |
| $t_{jit}$ | Buffer Additive Phase Jitter, RMS: Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01 | | Clock Frequency = 156.25MHz; Input Clock from 8T49NS010, Input Clock Jitter = 86.8fs; SMODEA/B[1:0] = 00 | | 36.7 | | fs |
| NF | Noise Floor | LVPECL | Offset Freq. >10MHz; 156.25MHz Clock Freq. | | -159.1 | | dBc/Hz |
| | | LVDS | | | -157.0 | | dBc/Hz |
| | | HCSL | | | -155.7 | | dBc/Hz |
| tjit(Ø) | RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz | | REF_SEL[1:0] = 10 or 11[3] | | 0.191 | | ps |
| $t_{PD}$ | Propagation Delay[4] | CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs | SMODEA/B[1:0] = 00 | 0.225 | | 0.80 | ns |
| | | | SMODEA/B[1:0] = 01 | 0.275 | | 0.80 | ns |
| | | | SMODEA/B[1:0] = 10 | 0.9 | | 2.80 | ns |
| *t*sk(o) | Output Skew[5, 6] | | | | | 80 | ps |
| *t*sk(pp) | Part-to-Part Skew[6, 7] | | | | 200 | | ps |
| $V_{OH}$ | Voltage High[8, 9] | HCSL Outputs | $T_A$ = 25°C, DC Measurement, $R_T$ = 50Ω to GND $C_L \leq$ 5pF | 520 | | 920 | mV |
| $V_{OL}$ | Voltage Low[8, 10] | HCSL Outputs | | -150 | | +150 | mV |
| $V_{CROSS}$ | Absolute Crossing Voltage[8, 11, 12] | HCSL Outputs | $R_T$ = 50Ω to GND $C_L \leq$ 5pF | 160 | | 460 | mV |
| $\Delta V_{CROSS}$ | Total Variation of $V_{CROSS}$ over all Edges[8, 11, 13] | HCSL Outputs | | | | 140 | mV |
| | Rise/Fall Edge Rate[3, 14, 15] | HCSL Outputs | | 0.6 | | 4.0 | V/ns |
| $t_R$ / $t_F$ | Output Rise/Fall Time | LVPECL Outputs | 20% to 80% | | 150 | 300 | ps |
| | | LVDS Outputs | 20% to 80% | | 150 | 300 | ps |
| | | HCSL Outputs | 20% to 80% | | 400 | 650 | ps |
| | | REFOUT | 20% to 80% | | 450 | 750 | ps |
| odc | Output Duty Cycle[16] | | with Crystal Input | 45 | | 55 | % |
| | | | with external 50%/ 50% Duty Cycle Clock Input | 45 | | 55 | % |
| $MUX_{_ISOLATION}$ | MUX Isolation | | 156.25MHz | | 75 | | dB |

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. All LVDS and LVPECL parameters characterized up to 1.5GHz. HCSL parameters characterized up to 250MHz.

NOTE 3. Measurement taken from differential waveform.

NOTE 4. Measured from the differential input crosspoint to the differential output crosspoint.

NOTE 5. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross-point.

NOTE 6. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 7. Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross-point.

NOTE 8. Measurement taken from single-ended waveform.

NOTE 9. Defined as the maximum instantaneous voltage including overshoot.

NOTE 10. Defined as the minimum instantaneous voltage including undershoot.

NOTE 11. Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

NOTE 12. Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all cross-point for this measurement.

NOTE 13. Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

NOTE 14. Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

NOTE 15. Measured at 100MHz.

NOTE 16. Measured for the following frequencies: 25MHz, 100MHz, 125MHz, 156.25MHz, 312.5MHz, 400MHz, and 644.5313MHz.

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**Table 6: AC Characteristics,** $V_{DD} = V_{DDOA} = V_{DDOB} = V_{DDOREF}$ = 2.5V±5%, GND = 0V, $T_A$ = -40°C to 85°C [1, 2]

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | LVDS, LVPECL Outputs | | | | 2000 | MHz |
| | | HCSL Outputs | | | | 250 | MHz |
| | | REFOUT | | | | 250 | MHz |
| $t_{jit}$ | Buffer Additive Phase Jitter, RMS: Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01 | | Clock Frequency = 156.25MHz; Input Clock from 8T49NS010, Input Clock Jitter = 86.8fs; SMODEA/B[1:0] = 00 | | 37.1 | | fs |
| tjit(Ø) | RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz | | REF_SEL[1:0] = 10 or 11[3] | | 0.371 | | ps |
| NF | Noise Floor | LVPECL | Offset Freq. >10MHz; 156.25MHz Clock Freq. | | -159 | | dBc/Hz |
| | | LVDS | | | -157 | | dBc/Hz |
| | | HCSL | | | -155 | | dBc/Hz |
| $t_{PD}$ | Propagation Delay[4] | CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs | SMODEA/B[1:0] = 00 | 0.275 | | 0.75 | ns |
| | | | SMODEA/B[1:0] = 01 | 0.275 | | 0.75 | ns |
| | | | SMODEA/B[1:0] = 10 | 0.9 | | 2.80 | ns |
| *t*sk(o) | Output Skew[5, 6] | | | | | 80 | ps |
| *t*sk(pp) | Part-to-Part Skew[6, 7] | | | | 200 | | ps |
| $V_{OH}$ | Voltage High[8, 9] | HCSL Outputs | $T_A$ = 25°C, DC Measurement, $R_T$ = 50Ω to GND $C_L \leq$ 5pF | 520 | | 920 | mV |
| $V_{OL}$ | Voltage Low[8, 10] | HCSL Outputs | | -150 | | +150 | mV |
| $V_{CROSS}$ | Absolute Crossing Voltage[8, 11, 12] | HCSL Outputs | $R_T$ = 50Ω to GND $C_L \leq$ 5pF | 160 | | 460 | mV |
| $\Delta V_{CROSS}$ | Total Variation of $V_{CROSS}$ over all Edges[8, 11, 13] | HCSL Outputs | | | | 140 | mV |
| | Rise/Fall Edge Rate[3, 14, 15] | HCSL Outputs | | 0.6 | | 4.0 | V/ns |
| $t_R$ / $t_F$ | Output Rise/Fall Time | LVPECL Outputs | 20% to 80% | | 150 | 300 | ps |
| | | LVDS Outputs | 20% to 80% | | 150 | 300 | ps |
| | | HCSL Outputs | 20% to 80% | | 400 | 650 | ps |
| | | REFOUT | 20% to 80% | | 450 | 750 | ps |
| odc | Output Duty Cycle[16] | | With Crystal Input | 45 | | 55 | % |
| | | | With external 50%/ 50% Duty Cycle Clock Input | 45 | | 55 | % |
| $MUX_{-ISOLATION}$ | MUX Isolation | | 156.25MHz | | 75 | | dB |

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. All LVDS and LVPECL parameters characterized up to 1.5GHz. HCSL parameters characterized up to 250MHz.

NOTE 3. Measurement taken from differential waveform.

NOTE 4. Measured from the differential input crosspoint to the differential output crosspoint.

NOTE 5. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross-point.

NOTE 6. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 7. Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross-point.

NOTE 8. Measurement taken from single-ended waveform.

NOTE 9. Defined as the maximum instantaneous voltage including overshoot.

NOTE 10. Defined as the minimum instantaneous voltage including undershoot.

NOTE 11. Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

NOTE 12. Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all cross-point for this measurement.

NOTE 13. Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

NOTE 14. Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

NOTE 15. Measured at 100MHz.

NOTE 16. Measured for the following frequencies: 25MHz, 100MHz, 125MHz, 156.25MHz, 312.5MHz, 400MHz, and 644.5313MHz.

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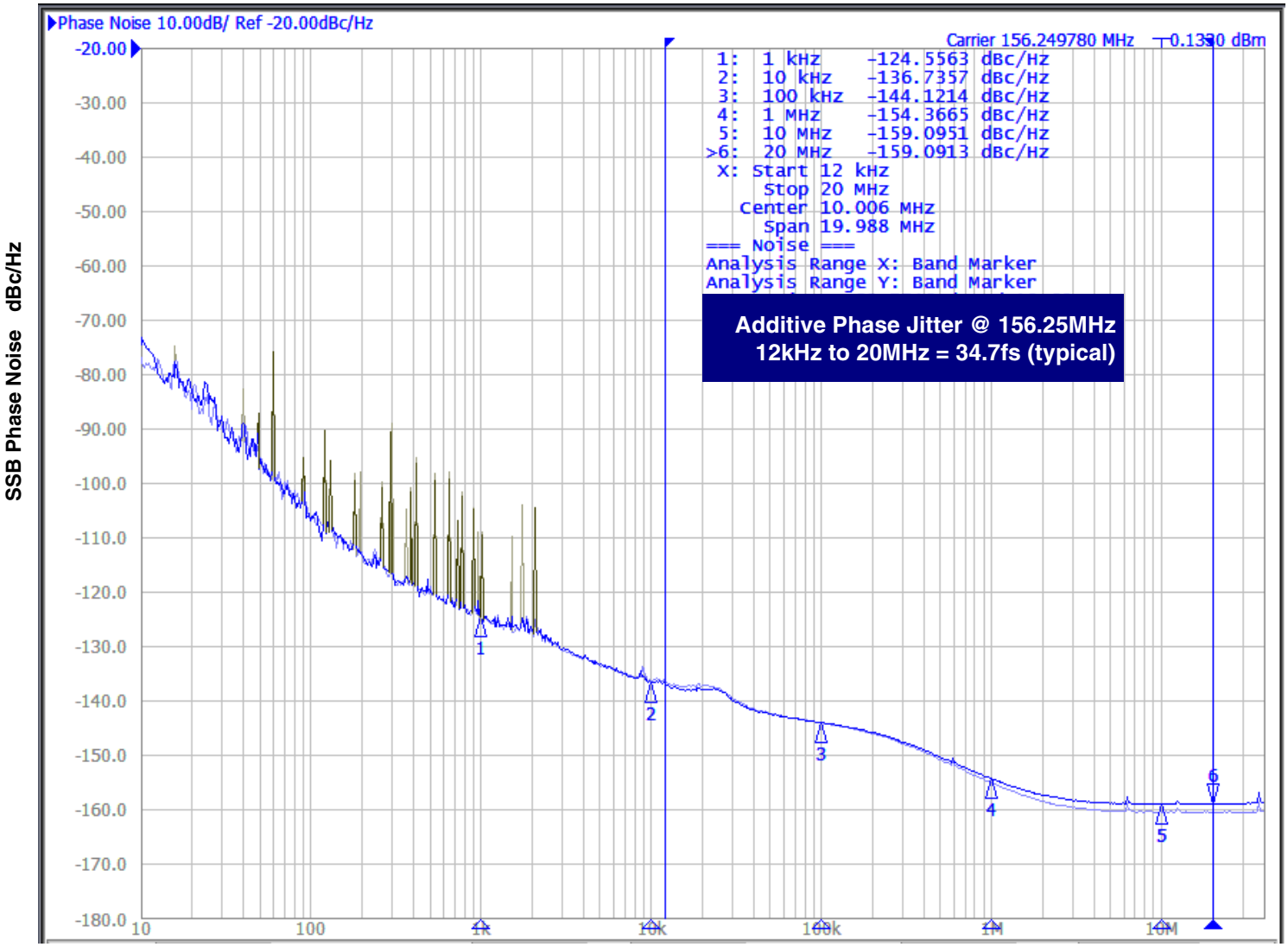
## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.




As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

The additive phase jitter for this device was measured using an IDT Clock Driver 8T49NS010 as an input source and Agilent E5052 phase noise analyzer.

# Applications Information

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, 1kΩ resistors can be tied from CLK to ground and nCLK to $V_{DD}$.

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

#### LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVCMOS Output (REFOUT)

If LVCMOS output is not used, then disable the output and it can be left floating.

#### LVPECL and HCSL Outputs

All unused output pairs can be left floating. We recommend that there is no trace attached.

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

## Crystal Input Interface

The 8T39S04A has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. In addition, the recommended 12pF parallel resonant crystal tuning is shown in *Figure 2.*The optimum C1 and C2 values can be slightly adjusted for different board layouts.

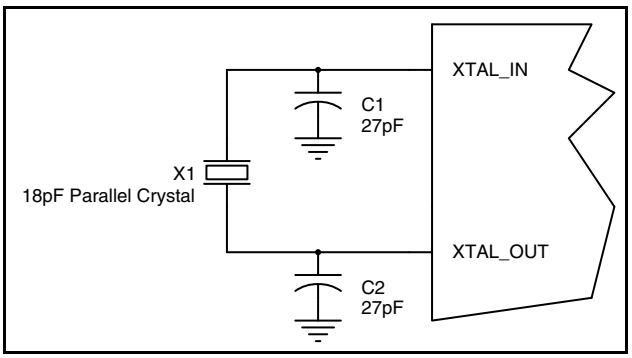



**Figure 1. Crystal Input Interface**

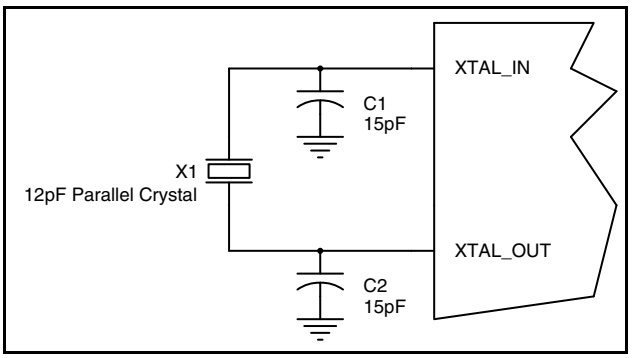



**Figure 2. Crystal Input Interface**

## Power Up Ramp Sequence

This device has multiple supply pins dedicated for different blocks. Output power supplies $V_{DDOx}$ ($V_{DDOA}$, $V_{DDOB}$, $V_{DDOREF}$) must ramp up before, or concurrently with core power supply $V_{DD}$. All power supplies must ramp up in a linear fashion and monotonically. Both $V_{DDOA}$ and $V_{DDOB}$ power supplies must be powered-up even when only one bank of outputs is in use.

## Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

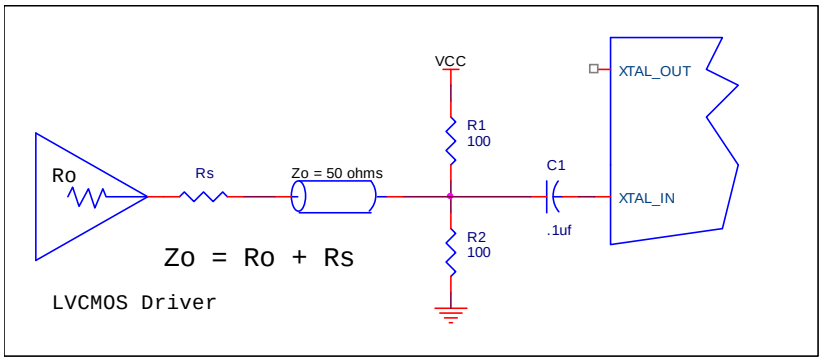



**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**

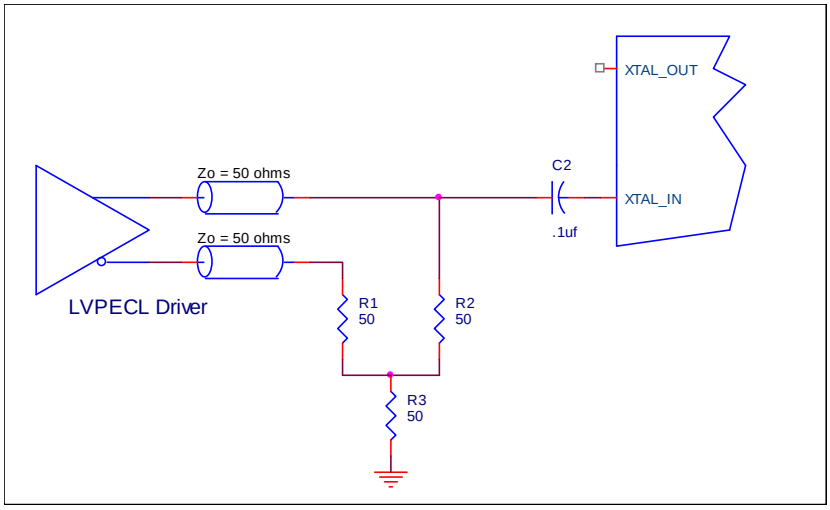



**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Wiring the Differential Input to Accept Single-Ended Levels

*Figure 4* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_1$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{DD}$ = 3.3V, R1 and R2 value should be adjusted to set $V_1$ at 1.25V. The values below are for when both the single ended swing and $V_{DD}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{DD}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

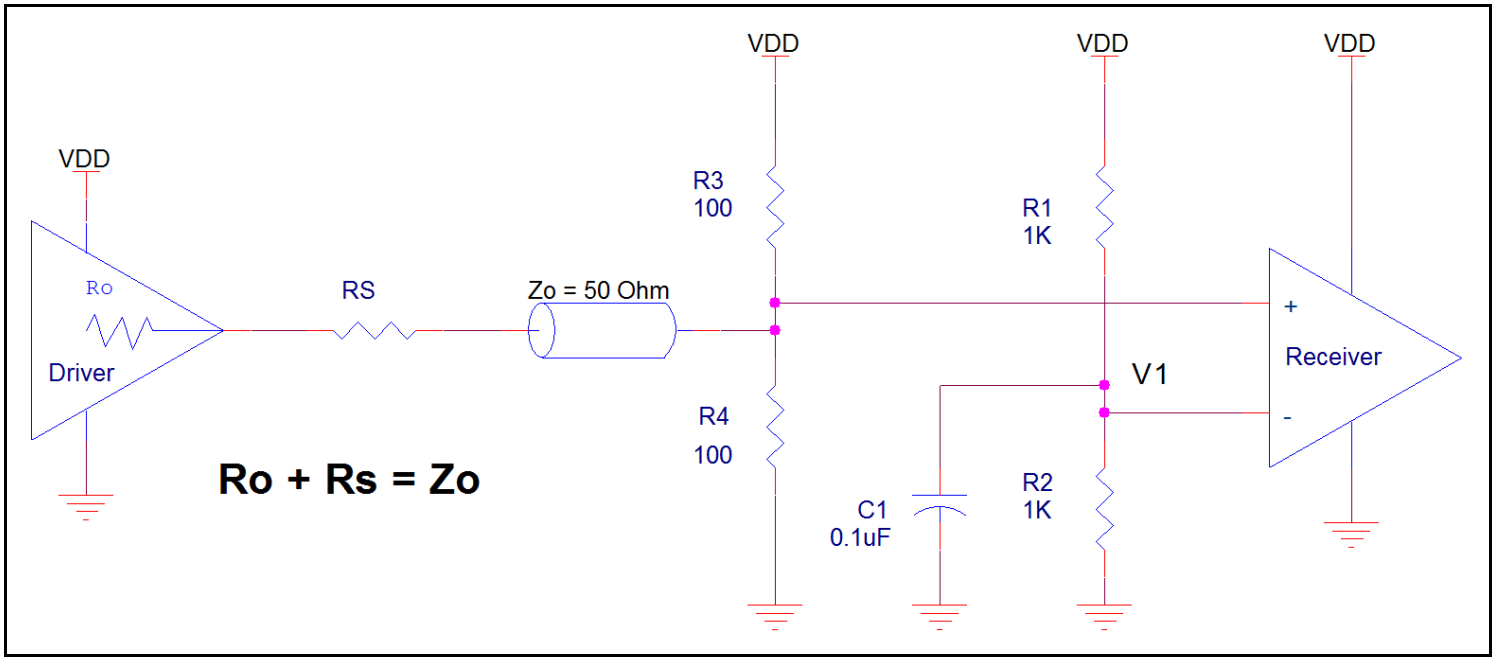



**Figure 4. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

## 3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HSTL and other differential signals. Both differential inputs must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 5A to 5E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 5A, the input termination applies for IDT open emitter HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.

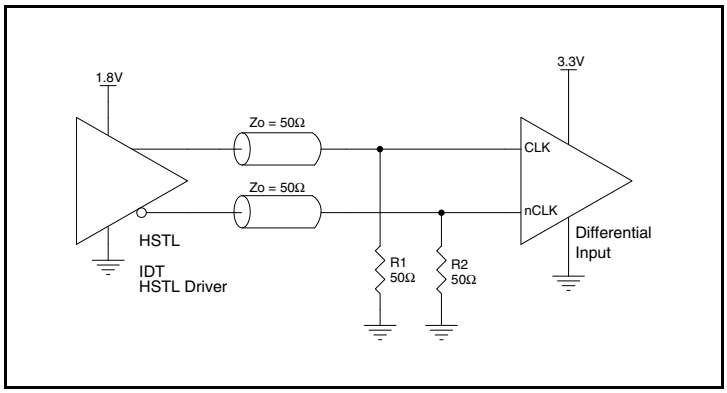



**Figure 5A. CLK/nCLK Input Driven by an IDT Open Emitter HSTL Driver**

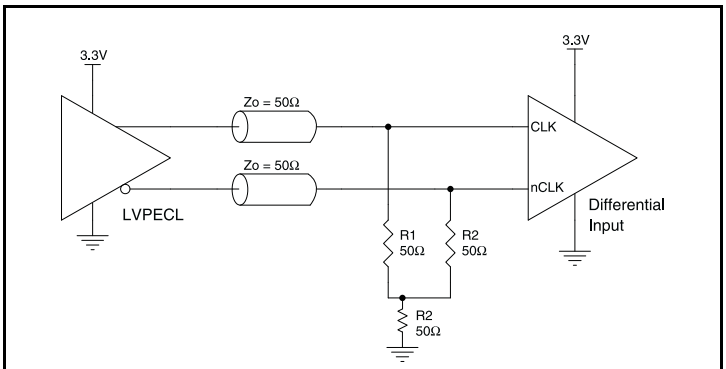



**Figure 5B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

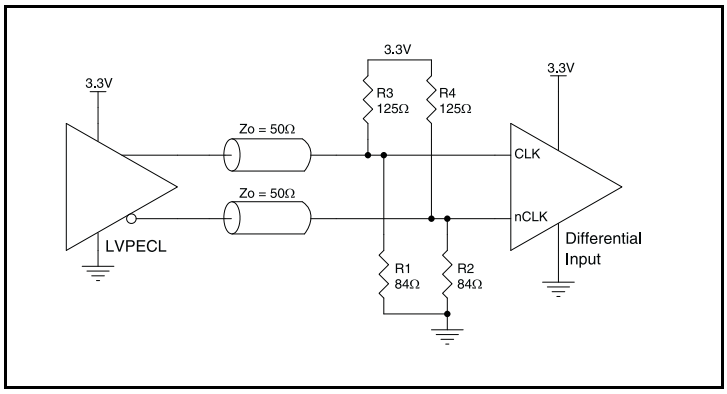



**Figure 5C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

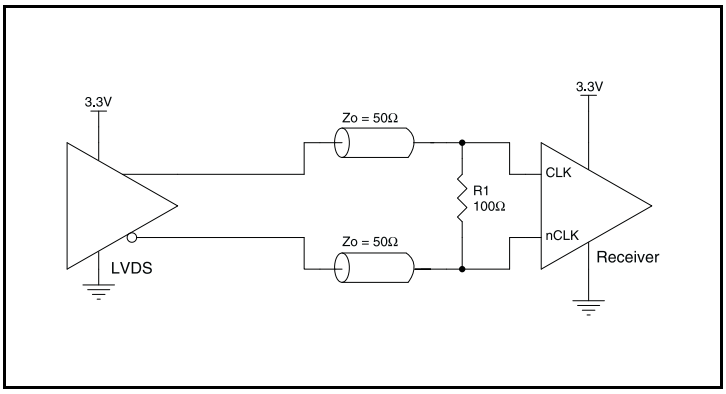



**Figure 5D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

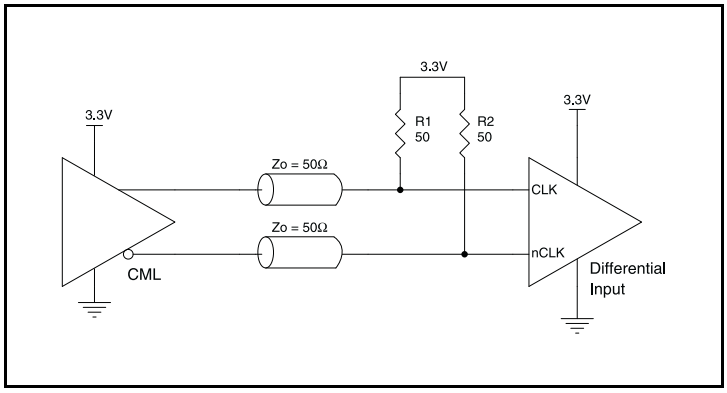



**Figure 5E. CLK/nCLK Input Driven by an IDT Open Collector CML Driver**

## 2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 6A to 6E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 6A, the input termination applies for IDT open emitter HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.

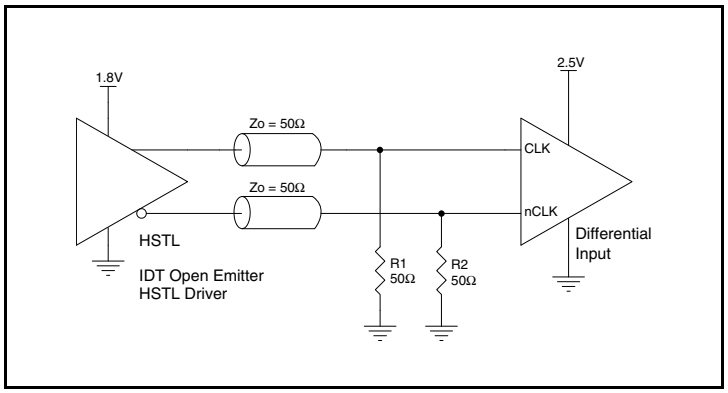



**Figure 6A. CLK/nCLK Input Driven by an IDT Open Emitter HSTL Driver**

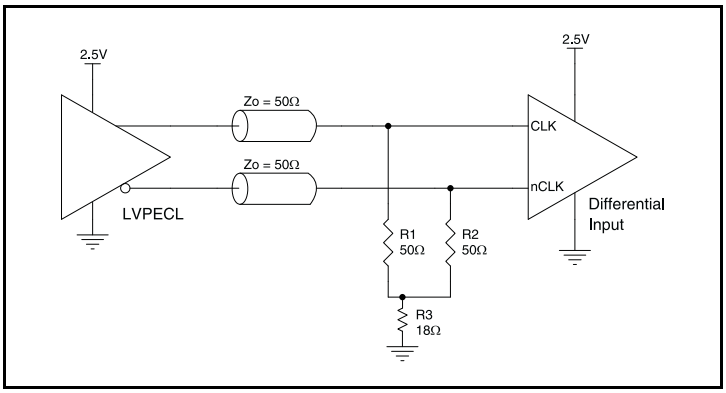



**Figure 6B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver**

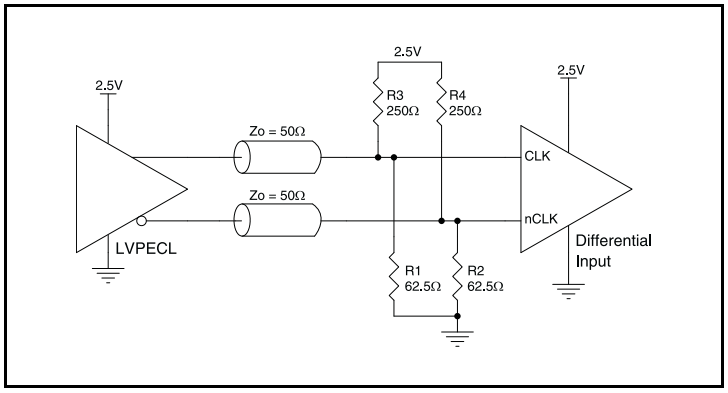



**Figure 6C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver**

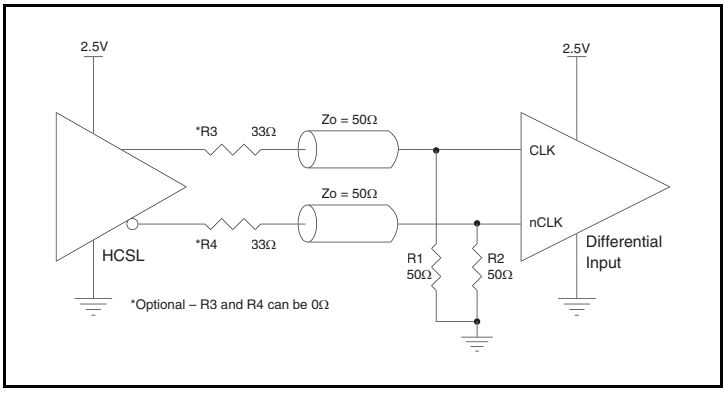



**Figure 6D. CLK/nCLK Input Driven by a 2.5V HCSL Driver**

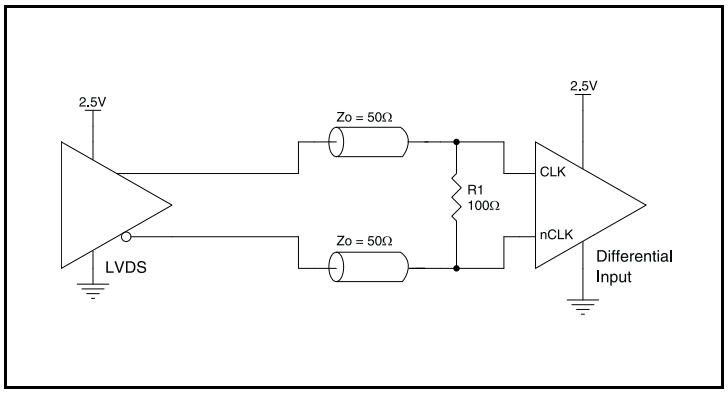



**Figure 6E. CLK/nCLK Input Driven by a 2.5V LVDS Driver**

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ($Z_T$) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ($Z_0$) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 7A* can be used with either type of output structure. *Figure 7B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

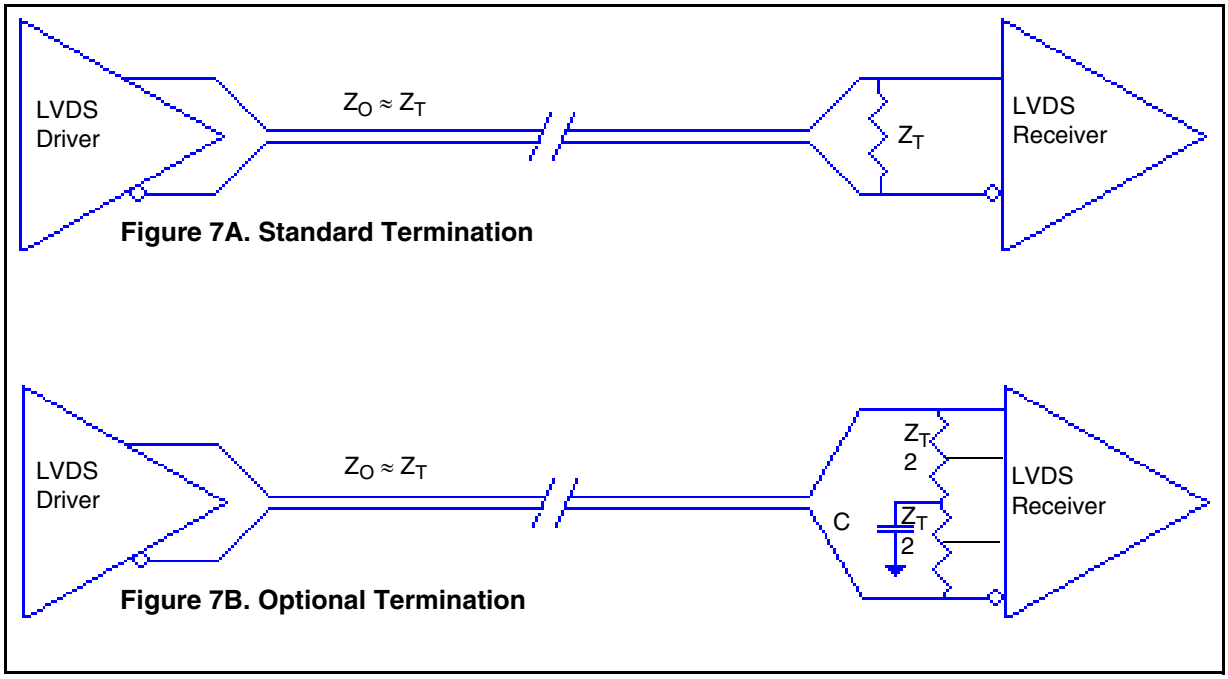



**Figure 7A. Standard Termination**

**Figure 7B. Optional Termination**

**LVDS Termination**

## Termination for 3.3V LVPECL Outputs

The clock topology shown below is a typical termination for LVPECL outputs. The two different terminations mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

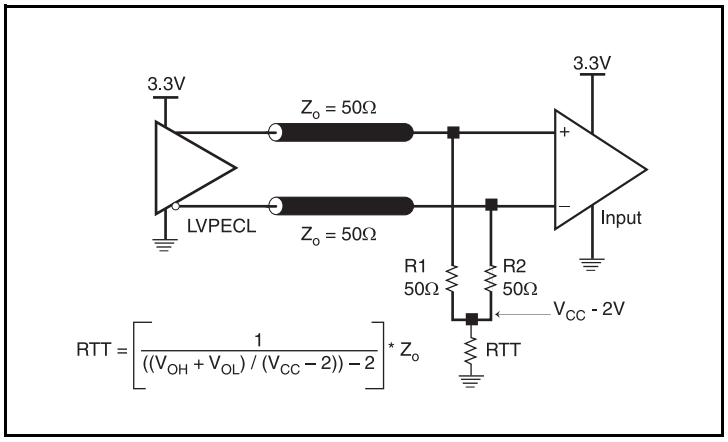



**Figure 8A. 3.3V LVPECL Output Termination**

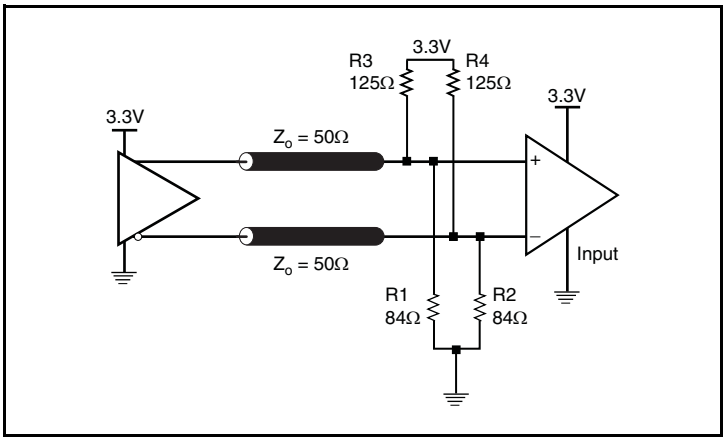



**Figure 8B. 3.3V LVPECL Output Termination**

## Termination for 2.5V LVPECL Outputs

*Figure 9A* and *Figure 9B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{DDO} - 2V$. For $V_{DDO} = 2.5V$, the $V_{DDO} - 2V$ is very close to ground level. The R3 in Figure 9B can be eliminated and the termination is shown in *Figure 9C.*

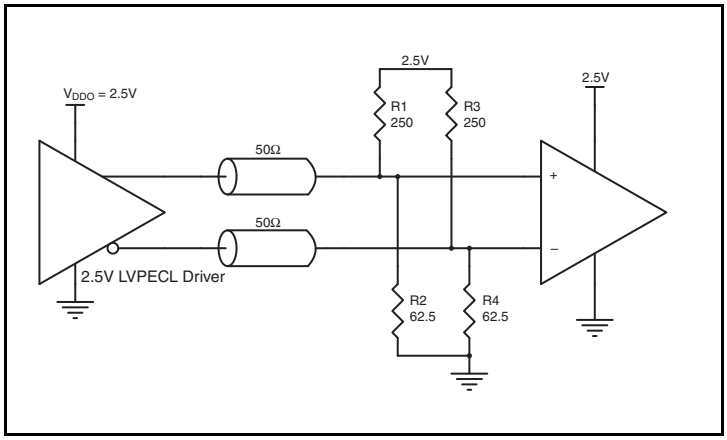



**Figure 9A. 2.5V LVPECL Driver Termination Example**

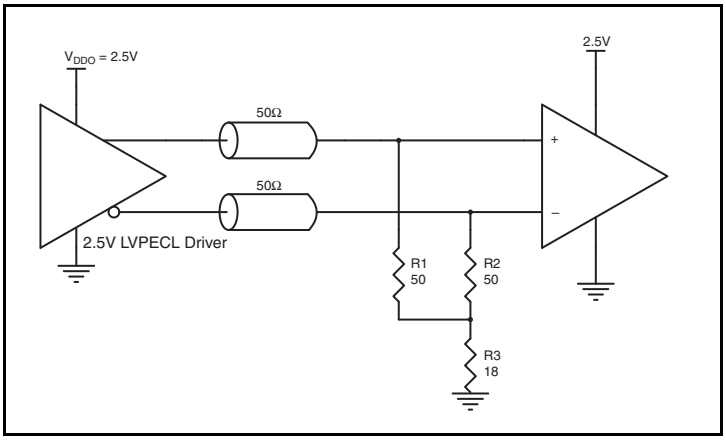



**Figure 9B. 2.5V LVPECL Driver Termination Example**

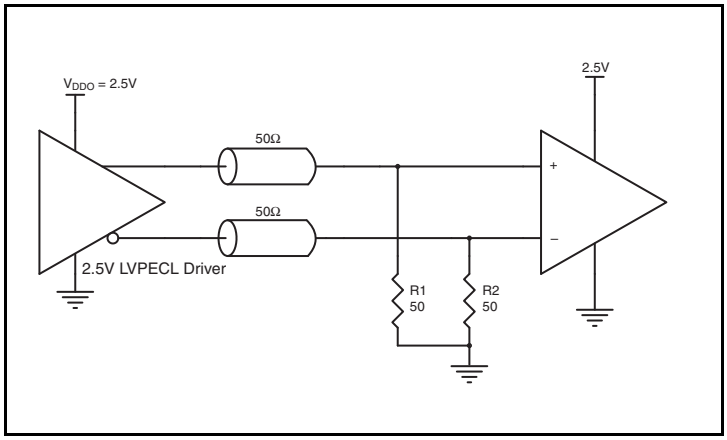



**Figure 9C. 2.5V LVPECL Driver Termination Example**

## Recommended Termination

*Figure 10A* is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

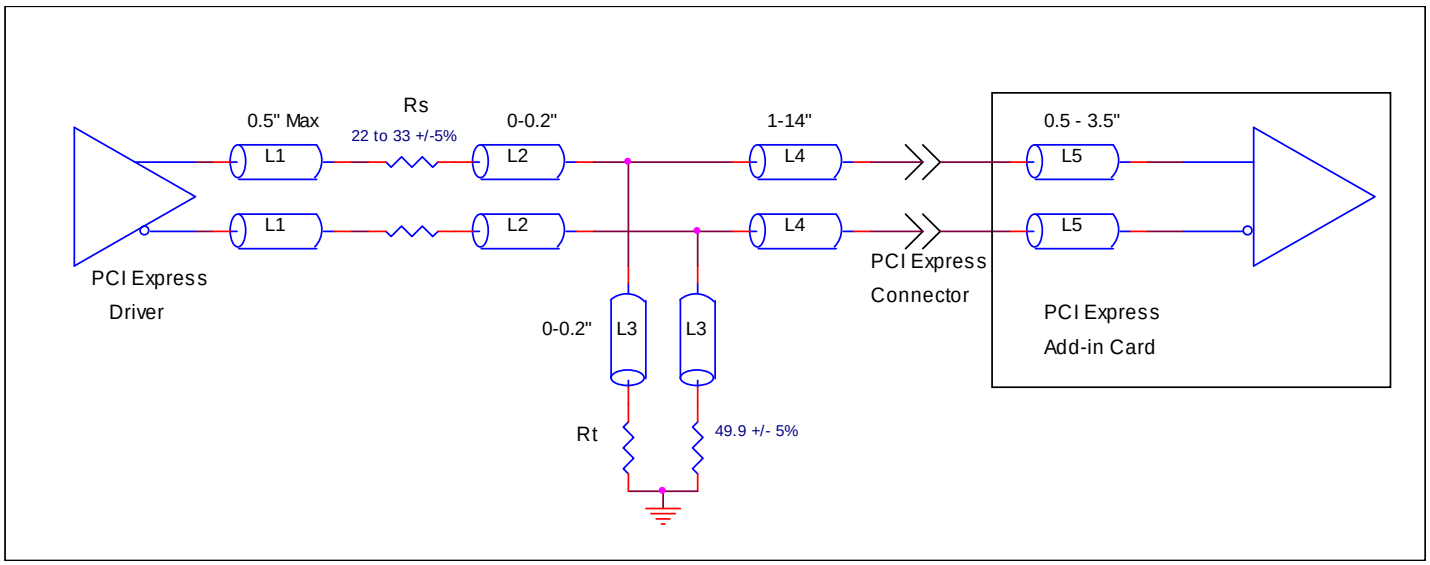



**Figure 10A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)**

*Figure 10B* is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

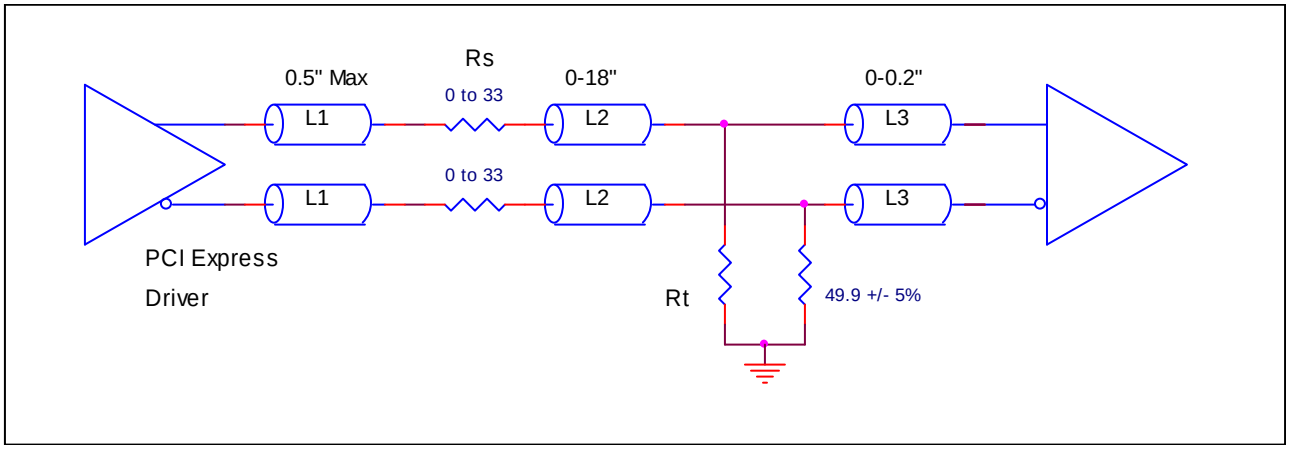



**Figure 10B. Recommended Termination (where a point-to-point connection can be used)**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 11.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

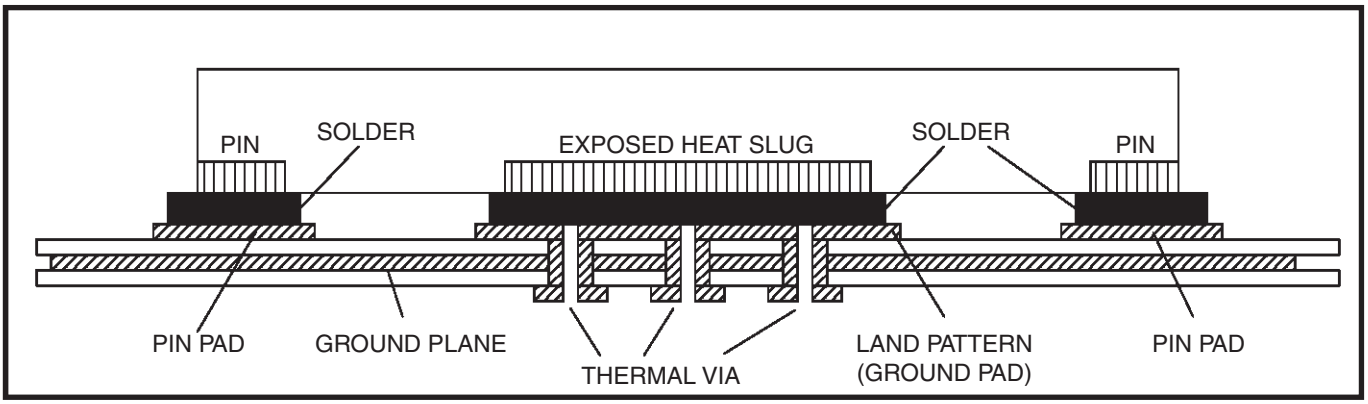



**Figure 11. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

# Power Considerations

This section provides information on power dissipation and junction temperature for the 8T39S04A. Equations and example calculations are also provided.

**LVPECL Power Considerations**

**1. Power Dissipation.**

The total power dissipation for the 8T39S04A is the sum of the core power plus the power dissipated due to outputs switching. The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

$I_{EE_MAX}$ = 130mA.

- Power $(core)_{MAX} = I_{EE_MAX} * V_{DD_MAX}$ = 3.465V * 130mA = **450.45mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**

If all outputs are loaded, the total power is 4 * 32mW = **128mW**

Max LVPECL Power Dissipation = 450.45mW + 128mW = **578.45mW**

**LVCMOS Output Power Dissipation**

- Static Power Dissipation:
  Power $(static)_{MAX} = V_{DDOREF_MAX} * I_{DDREF_MAX}$ = 3.465V * 2mA = **6.93mW**
  ($I_{DDREF_MAX}$ = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power $(Dynamic)_{MAX} = C_{PD} * F_{MAX} * N * V_{DDOREF}^2$ = 5.3pF * 250MHz * 1 * $3.465^2$ = **15.9mW**
- LVCMOS Power Dissipation = 6.93mW + 15.9mW = **22.84mW**

Total Power Dissipation = 578.45mW + 22.84mW = **601mW**

**2. Junction Temperature.**

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 7 below. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.601W * 39.5°C/W = 108.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance $\theta_{JA}$ for 32-Lead VFQFN**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 39.5°C/W | 34.5°C/W | 31.0°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 12.*

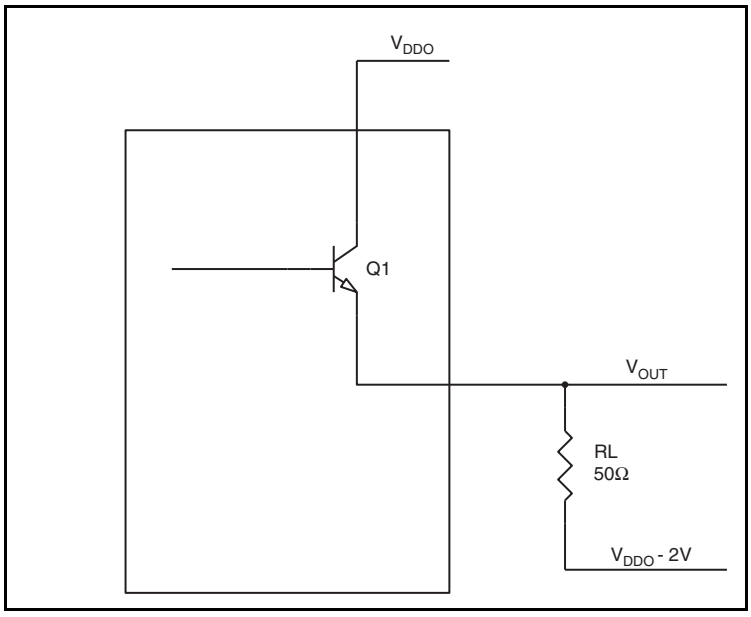



**Figure 12. LVPECL Driver Circuit and Termination**

To calculate power dissipation due to outputs switching, use the following equations which assume a 50Ω load, and a termination voltage of $V_{DDO}$ – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{DDO_MAX} - 0.8V}$
  $(V_{DDO_MAX} - V_{OH_MAX}) = \mathbf{0.8V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{DDO_MAX} - 1.6V}$
  $(V_{DDO_MAX} - V_{OL_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{DDO_MAX} – 2V))/R_L] * (V_{DDO_MAX} – V_{OH_MAX}) = [(2V – (V_{DDO_MAX} – V_{OH_MAX}))/R_L] * (V_{DDO_MAX} – V_{OH_MAX}) = [(2V – 0.8V)/50Ω] * 0.8V =$ **19.80mW**

$Pd_L = [(V_{OL_MAX} – (V_{DDO_MAX} – 2V))/R_L] * (V_{DDO_MAX} – V_{OL_MAX}) = [(2V – (V_{DDO_MAX} – V_{OL_MAX}))/R_L] * (V_{DDO_MAX} – V_{OL_MAX}) = [(2V – 1.6V)/50Ω] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = 32mW

# Power Considerations

This section provides information on power dissipation and junction temperature for the 8T39S04A. Equations and example calculations are also provided.

**LVDS Power Considerations**

**1. Power Dissipation.**

The total power dissipation for the 8T39S04A is the sum of the core power plus the power dissipated due to outputs switching. The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

$I_{DD_MAX}$ = 95mA

$I_{DDO_MAX}$ = 90mA

- Maximum LVDS Power Dissipation = $V_{DD_MAX}$ * ($I_{DD_MAX}$ + $I_{DDO_MAX}$) = 3.465V * (95mA + 90mA) = **641mW**

**LVCMOS Output Power Dissipation**

- Static Power Dissipation:
  Power (static)$_{_MAX}$ = $V_{DDOREF_MAX}$ * $I_{DDREF_MAX}$ = 3.465V * 2mA **= 6.93mW**
  ($I_{DDREF_MAX}$ = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power (Dynamic)$_{_MAX}$ = $C_{PD}$ * $f_{MAX}$ * N * $V_{DDOREF}^2$ = 5.3pF * 250MHz * 1 * $3.465^2$ = **15.9mW**
- LVCMOS Power Dissipation = 6.93mW + 15.9mW = **22.84mW**

Total Power Dissipation = 641mW + 22.84mW = **663.9mW**

**2. Junction Temperature.**

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 7. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.664W * 39.5°C/W = 111.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

# Power Considerations

This section provides information on power dissipation and junction temperature for the 8T39S04A. Equations and example calculations are also provided.

**HCSL Power Considerations**

**1. Power Dissipation.**

The total power dissipation for the IDT8T39S04AI is the sum of the core power plus the power dissipated due to outputs switching. The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

$I_{DD_MAX}$ = 95mA

$I_{DDO_MAX}$ = 60mA (application frequency = 250MHz)

- Power (core)$_{MAX}$ = $V_{DD_MAX}$ * ($I_{DD_MAX}$ + $I_{DDO_MAX}$) = 3.465V * (95mA + 60mA) = **537.1mW**
- Power (outputs)$_{MAX}$ = **44.5mW/Loaded Output pair**

If all outputs are loaded, the total power is 4 * 44.5mW = **178mW**

Max HCSL Power Dissipation = 537.1mW + 178mW = 715.1mW

**LVCMOS Output Power Dissipation**

- Static Power Dissipation:
  Power (static)$_{MAX}$ = $V_{DDOREF_MAX}$ * $I_{DDREF_MAX}$ = 3.465V * 2mA **= 6.93mW**
  ($I_{DDREF_MAX}$ = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power (Dynamic)$_{MAX}$ = $C_{PD}$ * $f_{MAX}$ * N * $V_{DDOREF}^2$ = 5.3pF * 250MHz * 1 * $3.465^2$ = **15.9mW**
- LVCMOS Power Dissipation = 6.93mW + 15.9mW = **22.84mW**

Total Power Dissipation = 715.1mW + 22.84mW = **737.9mW**

**2. Junction Temperature.**

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 7. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.738W * 39.5°C/W = 114.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**3. Calculations and Equations.**

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 13.*

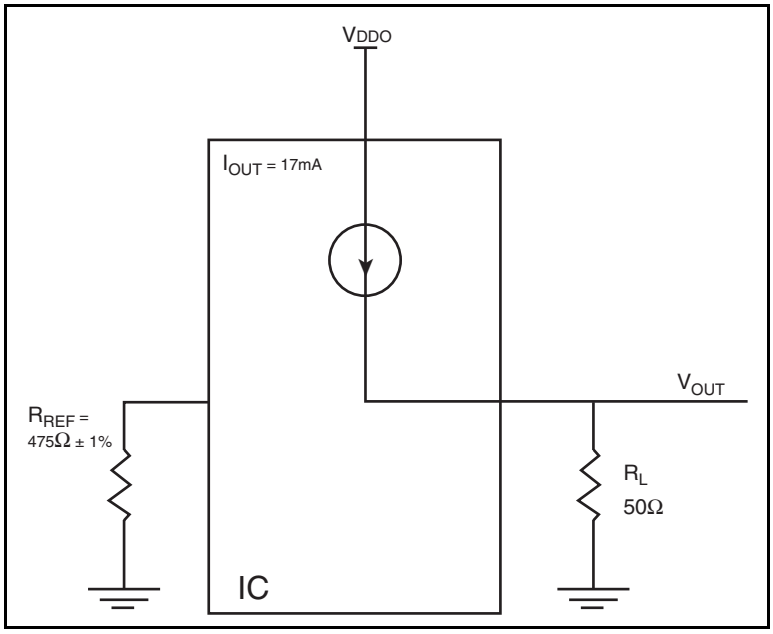



**Figure 13. HCSL Driver Circuit and Termination**

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when $V_{DDO_MAX}$.

Power = $(V_{DDO_MAX} - V_{OUT}) * I_{OUT}$,
since $V_{OUT} - I_{OUT} * R_L$

$= (V_{DDO_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

# Reliability Information

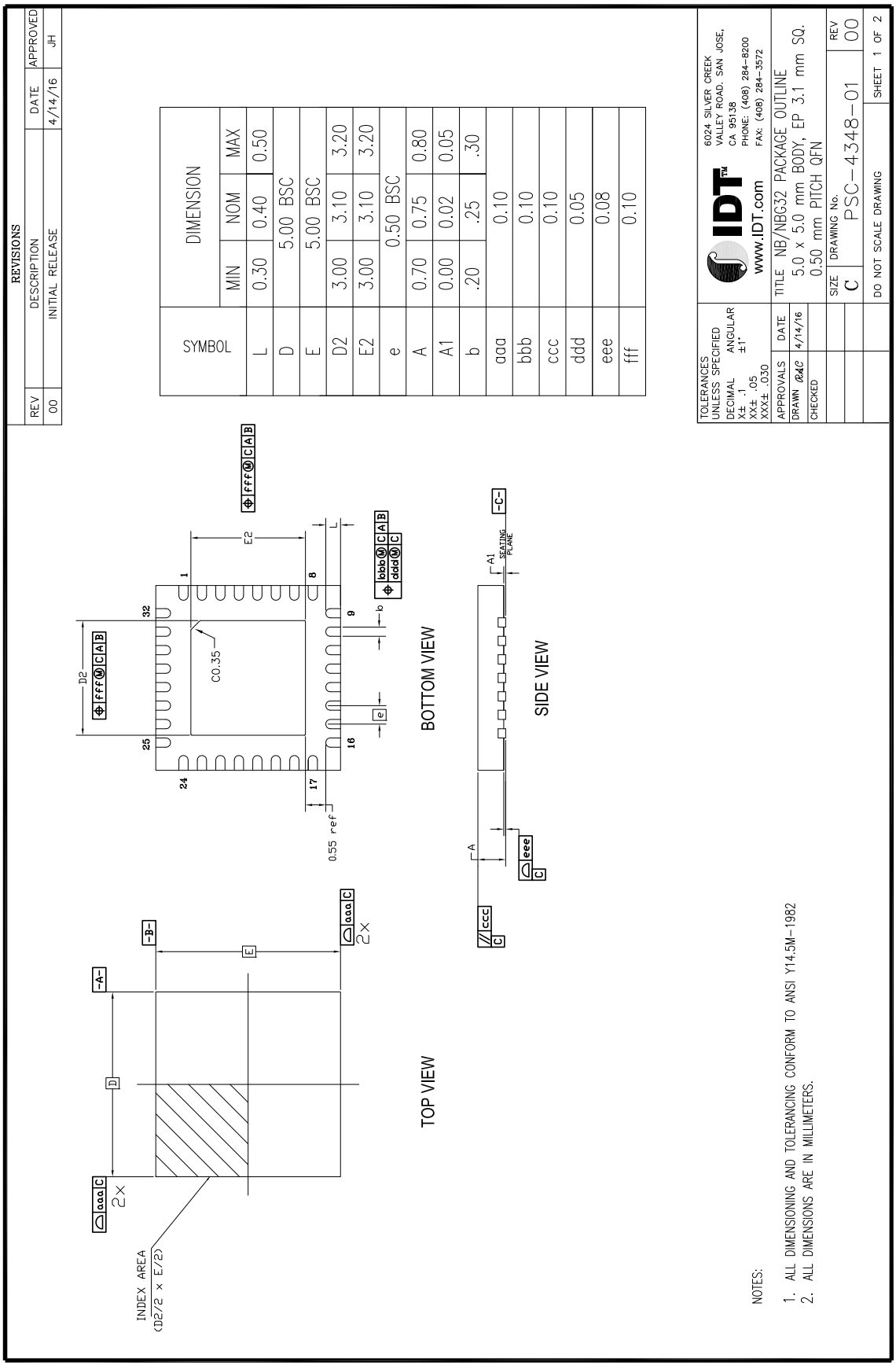
**Table 8. $\theta_{JA}$ vs. Air Flow Table for a 32-Lead VFQFN**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 39.5°C/W | 34.5°C/W | 31.0°C/W |

## Transistor Count

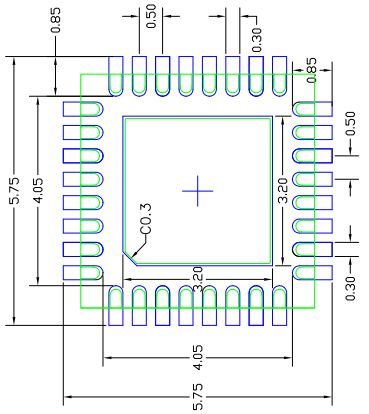
The transistor count for 8T39S04A is: 10,283

# 32-Lead VFQFN Package Outline and Package Dimensions



## 32-Lead VFQFN Package Outline and Package Dimensions, continued

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 4/14/16 | JH |




RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | |
|---|---|---|
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| APPROVALS DATE<br>DRAWN RAC 4/14/16<br>CHECKED | TITLE NB/NBG32 PACKAGE OUTLINE<br>5.0 x 5.0 mm BODY, EP 3.1 mm SQ.<br>0.50 mm PITCH QFN | |
| | SIZE C<br>DRAWING No. PSC-4348-01<br>DO NOT SCALE DRAWING | REV 00<br>SHEET 2 OF 2 |

# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8T39S04ANBGI | IDT8T39S04ANBGI | 32-Lead VFQFN, Lead-Free | Tray | -40°C to 85°C |
| 8T39S04ANBGI8 | IDT8T39S04ANBGI | 32-Lead VFQFN, Lead-Free | Tape & Reel | -40°C to 85°C |

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