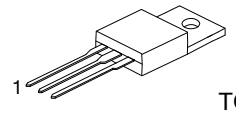
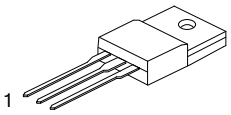
800V N-CHANNEL MOSFET



TO-220



TO-220F1

■ DESCRIPTION

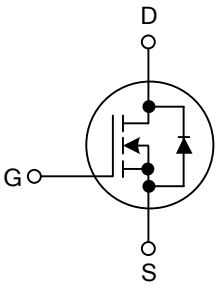
The UTC **8N80** is an N-channel mode Power FET, it uses UTC's advanced technology to provide costumers planar stripe and DMOS technology. This technology allows a minimum on-state resistance, superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **8N80** is generally applied in high efficiency switch mode power supplies.

■ FEATURES

* Typically 35 nC Low Gate Charge
* 8A, 800V, $R_{DS(on)}$ = 1.55Ω @V_{GS} = 10 V
* Typically 13 pF Low Crss
* Improved dv/dt Capability
* Fast Switching Speed
* 100% Avalanche Tested
* RoHS–Compliant Product

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
8N80L-TA3-T	8N80G-TA3-T	TO-220	G	D	S	Tube
8N80L-TF1-T	8N80G-TF1-T	TO-220F1	G	D	S	Tube

Note: G: GND, D: Drain, S: Source

8N80G-TA3-T (1)Packing Type (2)Package Type (3)Halogen Free	(1) T: Tube (2) TA3: TO-220, TF1: TO-220F1 (3) G: Halogen Free, L: Lead Free

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■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	800	V
Gate-Source Voltage	V_{GSS}	±30	V
Drain Current (Continuous) (T_C=25°C)	I_D	8	A
Drain Current (Pulsed) (Note 1)	I_{DM}	32	A
Avalanche Current (Note 1)	I_{AR}	8	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	850	mJ
Repetitive Avalanche Energy (Note 1)	E_{AR}	17.8	mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5	V/ns
Total Power Dissipation (T_C=25°C)	P_D	178	W
Linear Derating Factor above T_C=25°C		1.43	W/°C
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-55~+150	°C

Note: 1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 25mH, I_{AS} = 8A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 8A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	°C/W
Junction to Case	θ_{JC}	0.7	°C/W

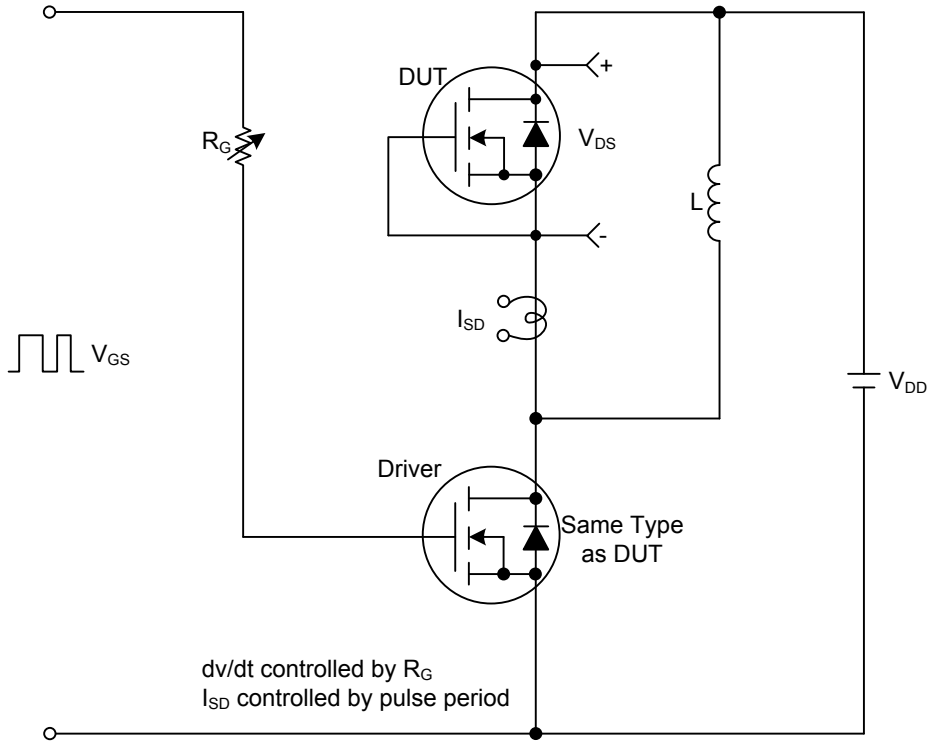
■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

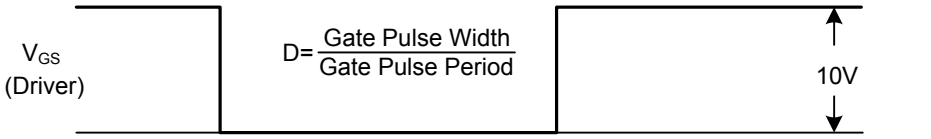
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	800			V
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	Reference to 25°C, I_D=250μA		0.5		V/°C
Drain-Source Leakage Current	I_{DSS}	V_{DS}=800V, V_{GS}=0V			10	μA
		V_{DS}=640V, T_C=125°C			100	
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	3.0		5.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=4A		0.94	1.55	Ω
Forward Transconductance (Note 1)	g_{FS}	V_{DS}=50V, I_D=4A		5.6		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		1580	2050	pF
Output Capacitance	C_{OSS}			135	175	pF
Reverse Transfer Capacitance	C_{RSS}			13	17	pF
SWITCHING PARAMETERS (Note 1, Note 2)						
Total Gate Charge	Q_G	V_{GS}=10V, V_{DS}=640V, I_D=8A		35	45	nC
Gate to Source Charge	Q_{GS}			10		nC
Gate to Drain Charge	Q_{GD}			14		nC
Turn-ON Delay Time	$t_{D(ON)}$	V_{DD}=400V, I_D=8A, R_G=25Ω		40	90	ns
Rise Time	t_R			110	230	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			65	140	ns
Fall-Time	t_F			70	150	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				8	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				32	A
Drain-Source Diode Forward Voltage	V_{SD}	I_S=8A, V_{GS}=0V			1.4	V
Reverse Recovery Time (Note 1)	t_{RR}	I_S=8A, V_{GS}=0V, dI_F/dt=100A/μs		690		ns
Reverse Recovery Charge (Note 1)	Q_{RR}			8.2		μC

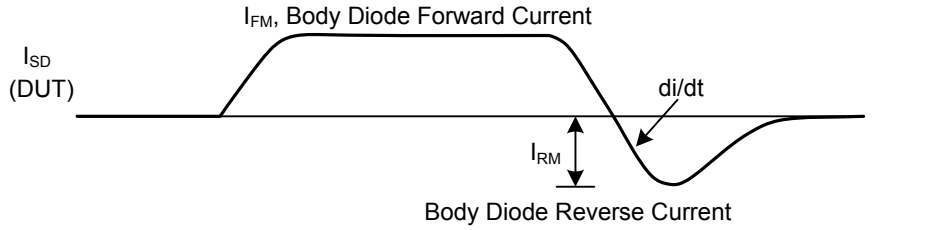
Note: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Essentially independent of operating temperature

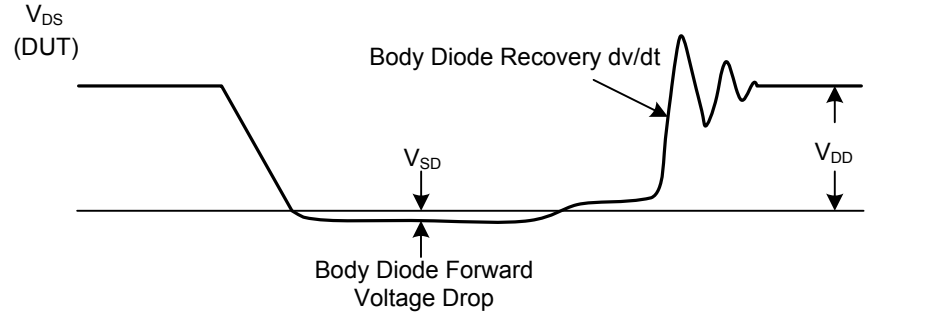
■ TEST CIRCUITS AND WAVEFORMS

Peak Diode Recovery dv/dt Test Circuit & Waveforms



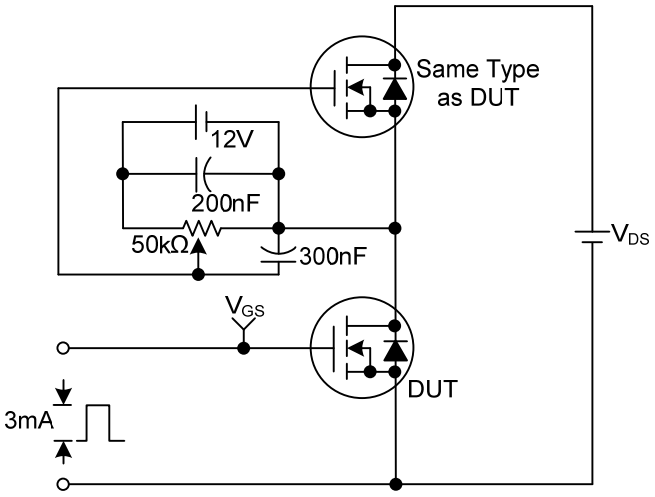




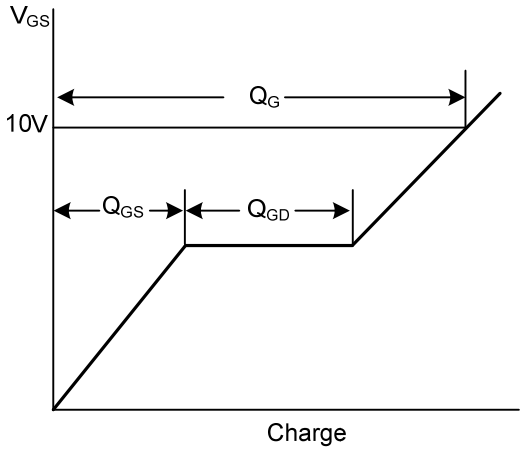


■ TEST CIRCUITS AND WAVEFORMS

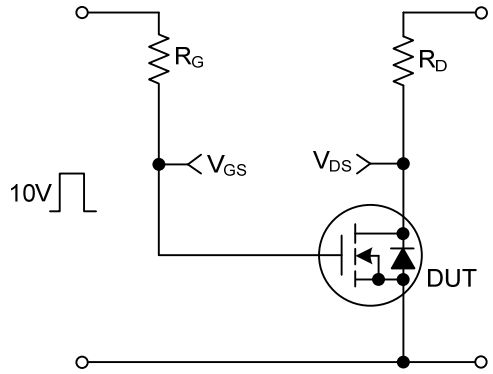
Gate Charge Test Circuit



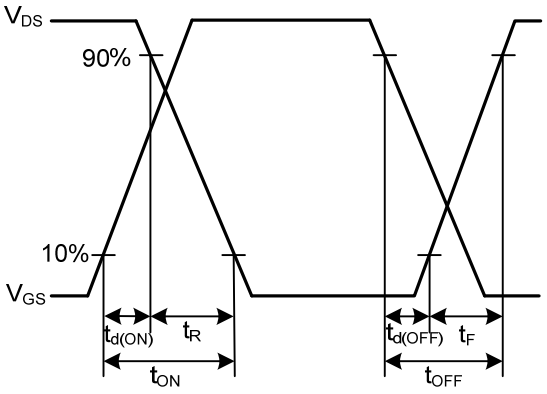
Gate Charge Waveforms



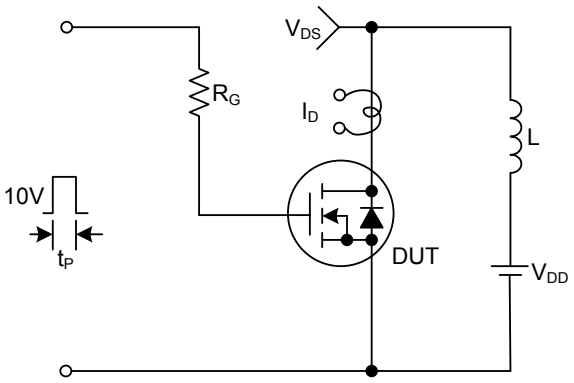
Resistive Switching Test Circuit



Resistive Switching Waveforms

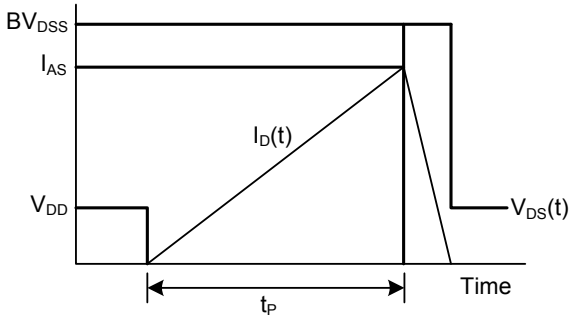


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

$$E_{AS}=\frac{1}{2}LI_{AS}^{2}\frac{BV_{DSS}}{BV_{DSS}-V_{DD}}$$



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