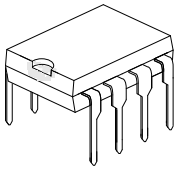
POWER FACTOR CORRECTOR



DIP-8

■ DESCRIPTION

The UTC **8561** is a Power Factor Corrector, which can work in wide input voltage range applications (from 85V ~ 265V) with an excellent THD. It has very low start up current (about 50 uA) and a disable function on the ZCD pin, which is designed to keep lower current consumption in stand by mode.

The device is operating in transition mode, and is able to drive a Power MOS or IGBT with a ± 400mA current for sourcing and sinking.

■ FEATURES

* 1% Precision (@ T_J = 25°C) Internal Reference Voltage
* Output Overvoltage Protection
* Very Low Power Start-Up Current
* Very Low Operating Supply Current
* Current Sense Filter On Chip
* Disable Function (with ZCD Pin)
* Transition Mode Operation
* Gate Driving Current: ± 400mA

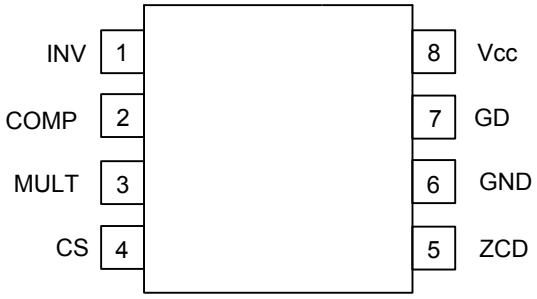
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free Plating	Halogen Free		
8561L-D08-T	8561G-D08-T	DIP-8	Tube

8561G-D08-T (1)Packing Type (2)Package Type (3)Halogen Free	(1) T: Tube (2) D08: DIP-8 (3) G: halogen Free, L: Lead Free Plating

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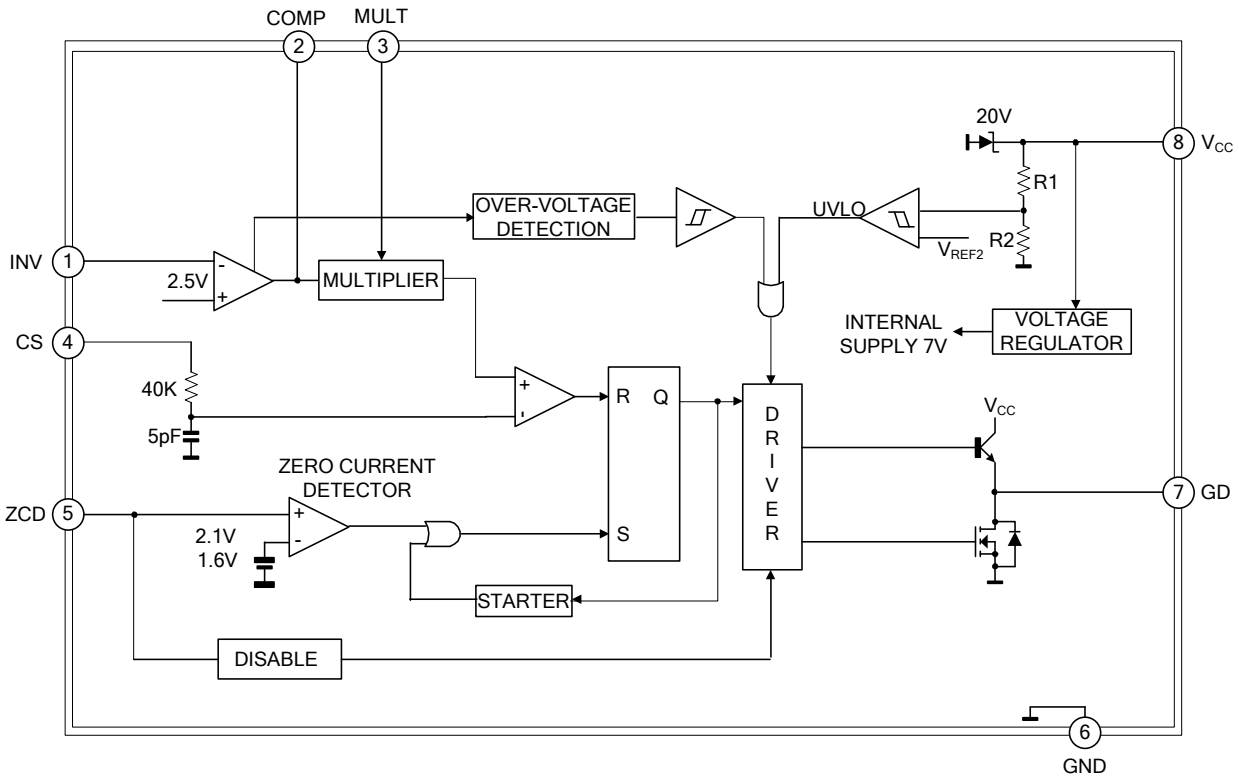
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO	PIN NAME	DESCRIPTION
1	INV	Inverting input of the error amplifier.
2	COMP	Output of the error amplifier.
3	MULT	Input of the multiplier stage.
4	CS	Input of the current sense stage.
5	ZCD	Input of the zero current detection.
6	GND	Ground.
7	GD	Gate driver output.
8	V_{CC}	Voltage supply.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Analog Inputs & Outputs	INV, COMP MULT	-0.3 ~ 7	V
Current Sense Input	CS	-0.3 ~ 7	V
Iq+Iz (I_{GD} = 0)	IV_{CC}	30	mA
Output Totem Pole Peak Current (2ms)	I_{GD}	±700	mA
Zero Current Detector	ZCD	50 (source) -10 (sink)	mA mA
Power Dissipation	P_D	0.65	W
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (V_{CC}=14.5V, Ta=-25°C ~ 125°C, unless otherwise specified)

PARAMETER	PIN	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE SECTION							
Operating Range	8	V_{CC}	after turn-on	11		18	V
Turn-ON Threshold	8	$V_{CC(ON)}$		11	12	13	V
Turn-OFF Threshold	8	$V_{CC(OFF)}$		8.7	9.5	10.3	V
Hysteresis	8	Hys		2.2	2.5	2.8	V
SUPPLY CURRENT SECTION							
Start-up Current	8	$I_{START-U}$	before turn-on (V_{CC}=11V)	20	50	90	μA
Quiescent Current	8	Iq			2.6	4	mA
Operating Supply Current	8	I_{CC}	C_L=1nF @ 70KHz		4	5.5	mA
			In OVP condition V_{pin1}=2.7V		1.4		mA
Quiescent Current	8	Iq	V_{PIN5}≤150mA, V_{CC}>$V_{CC\ off}$		1.4		mA
	8		V_{PIN5}≤150mV, V_{CC}<V_{CC} off	20	50	90	μA
Zener Voltage	8	V_Z	I_{CC}=25mA	18	20	30	V
ERROR AMPLIFIER SECTION							
Voltage Feedback Input Threshold	1	V_{INV}	Ta=25°C	2.465	2.5	2.535	V
			12V<V_{CC}<18V	2.44		2.56	V
Line Regulation			V_{CC}=12 ~ 18V		2	5	mV
Input Bias Current	1	I_{INV}			-100	-1000	uA
Voltage Gain		G_V	Open loop	60	80		dB
Gain Bandwidth		G_B			1		MHz
Source Current	2	I_{COMP}	V_{COMP}=4V, V_{INV}=2.4V	-2	-4	-8	mA
Sink Current			V_{COMP}=4V, V_{INV}=2.6V	2.5	4.5		mA
Upper Clamp Voltage	2	V_{COMP}	I_{SOURCE}=0.5mA		5.8		V
Lower Clamp Voltage			I_{sink}=0.5mA		2.25		V
MULTIPLIER SECTION							
Linear Operating Voltage	3	V_{MULT}		0~ 3	0 ~ 3.5		V
Output Max.Slope		$\frac{\triangle V_{CS}}{\triangle V_{mult}}$	V_{MULT}=from 0V ~ 0.5V V_{COMP}=Upper ClamVoltage	1.65	1.9		
Gain		K	V_{MULT}=1V, V_{COMP}=4V	0.45	0.6	0.75	1/V
CURRENT SENSE COMPARATOR							
Current Sense Reference Clamp	4	V_{CS}	V_{MULT}=2.5V V_{COMP}=Upper Clamp Voltage	1.6	1.7	1.8	V
Input Bias Current	4	I_{CS}	V_{OS}=0		-0.05	-1	μA
Delay to Output	4	$t_{d(H-L)}$			200	450	ns
Current Sense Offset	4				0	15	mV

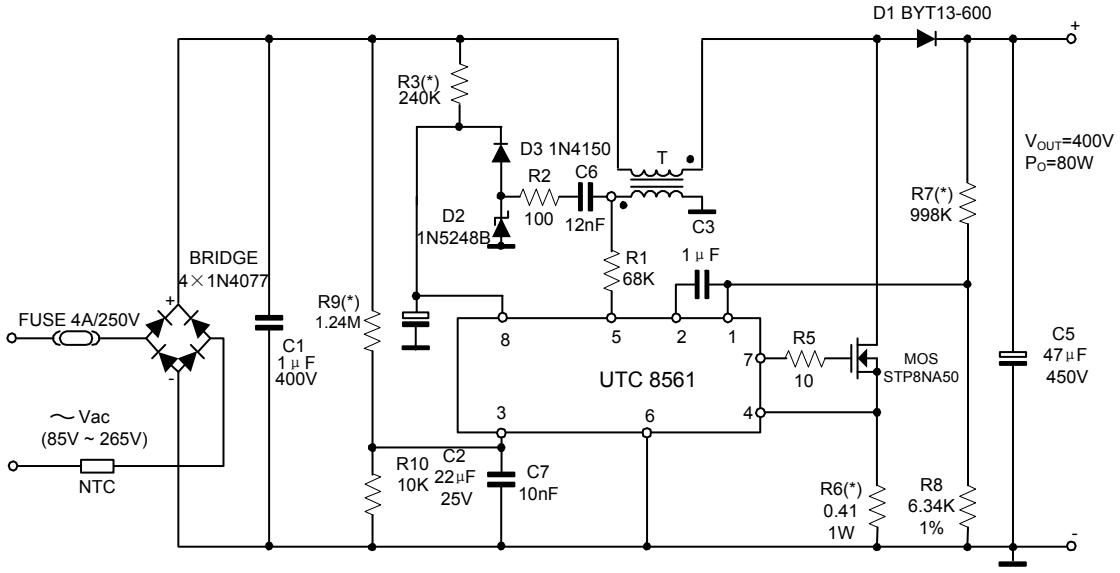
■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	PIN	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ZERO CURRENT DETECTOR							
Input Threshold Voltage Rising Edge (Note)	5	V_{ZCD}			2.1		V
Hysteresis (Note)				0.3	0.5	0.7	V
Upper Clamp Voltage	5	V_{ZCD}	I_{ZCD}=20μA	4.5	5.0	6.8	V
Upper Clamp Voltage	5	V_{ZCD}	I_{ZCD}=3mA	4.7	5.1	7	V
Lower Clamp Voltage	5	V_{ZCD}	I_{ZCD}=3mA	0.3	0.65	1	V
Sink Bias Current	5	I_{ZCD}	1V≦V_{ZCD}≦4.5V		2		μA
Source Current Capability	5	I_{ZCD}		-3		-10	mA
Sink Current Capability	5	I_{ZCD}		3		10	mA
Disable threshold	5	V_{DIS}			200	300	mV
Restart Current After Disable	5	I_{ZCD}	V_{ZCD}<V_{dis}, V_{CC}>V_{COFF}		-200	-300	μA
OUTPUT SECTION							
Dropout Voltage	7	V_{GD}	$I_{GDsource}$=200mA		1.2	2	V
			$I_{GDsource}$=20mA		0.7	1	V
			I_{GDsink}=200mA			1.5	V
			I_{GDsink}=20mA			0.3	V
Output Voltage Rise Time	7	t_R	C_L=1nF		40	100	ns
Output Voltage Fall Time	7	t_F	C_L=1nF		40	100	ns
IGD Sink Current	7	$I_{GD(OFF)}$	V_{CC}=3.5V, V_{GD}=1V	5	10		mA
OUTPUT OVERVOLTAGE SECTION							
OVP Triggering Current	2	I_{OVP}		35	40	45	μA
Static OVP Threshold				2.1	2.25	2.4	V
RESTART TIMER							
Start Timer		t_{START}		70	150	400	μs

Note: Parameter guaranteed by design, not tested in production.

■ TYPICAL APPLICATION CIRCUIT

(80W, Wide-range Mains)



(*) R3 = 2×120KΩ
R6 = 0.82Ω /2
R7 = 2×499KΩ, 1%
R9 = 2×620KΩ

TRANSFORMER
T: core THOMSON-CSF B1ET2910A(ETD29×16×10mm)OR EQUIVALENT (OREGA 473201A8)
primary 90T of Litz wire 10×0.2mm
secondary 7T of #27 AWG (0.15mm)
gap 1.25mm for a total primary inductance of 0.8mH

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