General Description

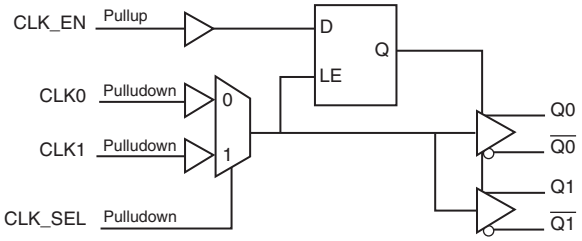
The 8535-21 is a low skew, high performance 1-to-2 LVCMOS/LVTTL-to-3.3V LVPECL fanout buffer. The 8535-21 has two single-ended clock inputs. The single-ended clock input accepts LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The clock enable is internally synchronized to eliminate runt clock pulses on the output during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the 8535-21 ideal for those applications demanding well defined performance and repeatability.

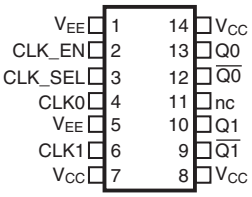
Features

- Two differential 3.3V LVPECL outputs
- Selectable CLK0 or CLK1 inputs for redundant and multiple frequency fanout applications
- CLK0 or CLK1 can accept the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 266MHz
- Translates LVCMOS and LVTTL levels to 3.3V LVPECL levels
- Output skew: 20ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 1.6ns (maximum)
- Additive phase jitter, RMS: 0.03ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in lead-free (RoHS 6)

Block Diagram



Pin Assignment



8535-21
14 Lead TSSOP
4.40mm x 5.0mm x 0.925mm package body
G Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 5	V_{EE}	Power		Negative supply pins.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced low, $\overline{Qx}$ outputs are forced high. LVCMOS/LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS/LVTTL interface levels.
4, 6	CLK0, CLK1	Input	Pulldown	Single-ended clock inputs. LVCMOS/LVTTL interface levels.
7, 8, 14	V_{CC}	Power		Power supply pins.
9, 10	$\overline{Q1}$, Q1	Output		Differential output pair. LVPECL interface levels.
11	nc	Unused		No connect.
12, 13	$\overline{Q0}$, Q0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

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Function Tables

Table 3A. Control Input Function Table

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0, Q1**	**$\overline{Q0}$, $\overline{Q1}$**
0	0	CLK0	Disabled; Low	Disabled; High
0	1	CLK1	Disabled; Low	Disabled; High
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLK0 and CLK1 inputs as described in Table 3B.

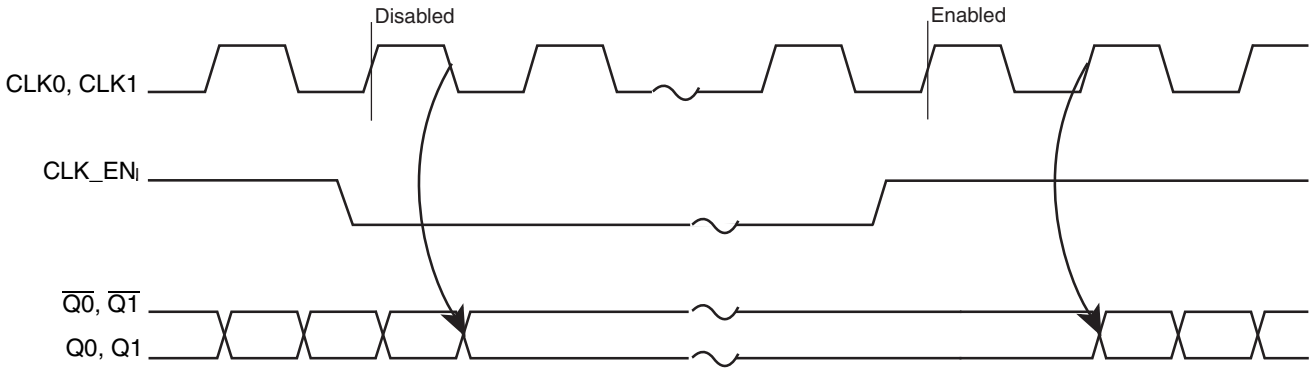


Figure 1. CLK_EN Timing Diagram

Table 3B. Clock Input Function Table

Inputs	Outputs	
CLK0 or CLK1	**Q0, Q1**	**$\overline{Q0}$, $\overline{Q1}$**
0	LOW	HIGH
1	HIGH	LOW

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	93.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				50	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	CLK0, CLK1		-0.3		1.3	V
		CLK_EN, CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	CLK0, CLK1, CLK_SEL	V_{CC} = V_{IN} = 3.465			150	µA
		CLK_EN	V_{CC} = V_{IN} = 3.465			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, CLK_SEL	V_{CC} = 465V, V_{IN} = 0V	-5			µA
		CLK_EN	V_{CC} = 465V, V_{IN} = 0V	-150			µA

Table 4C. LVPECL DC Characteristics, V_{CC} = 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	µA
V_{OL}	Output Low Current; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	µA
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 266MHz	1.0		1.6	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2	156.25MHz, Integration Range: 12kHz – 20MHz		0.03		ps
*t*sk(o)	Output Skew; NOTE 3, 4				20	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5				300	ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	300		600	ps
odc	Output Duty Cycle	$f \leq$ 200MHz	45		55	%

NOTE: All parameters measured at $f \leq$ 266MHz unless noted otherwise.

NOTE 1: Measured from V_{CC}/2 of the input to the differential output crossing point. The part does not add jitter.
NOTE 2: Driving only one input clock.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at V_{CC}/2 of the input to the differential output crossing point.

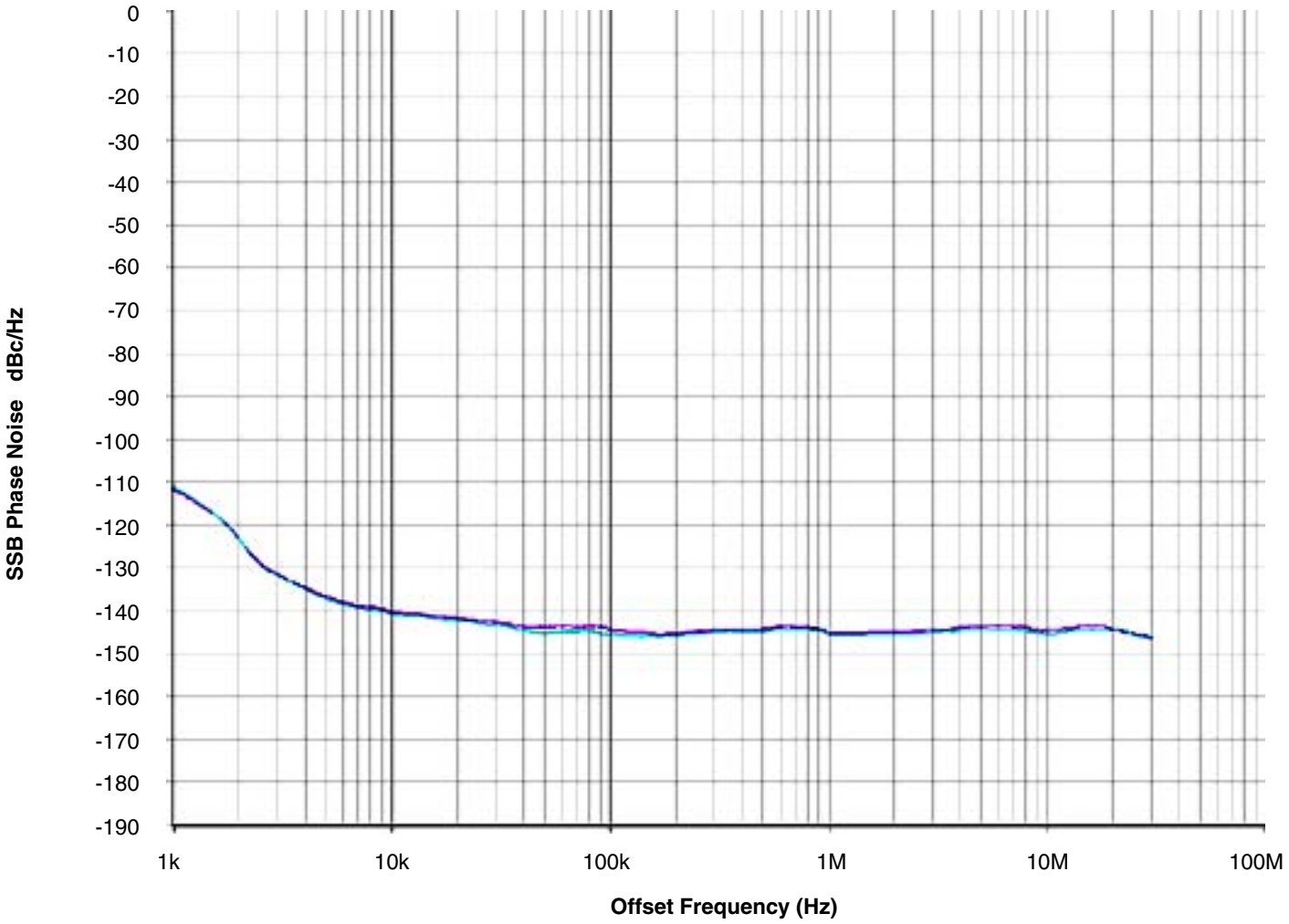
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

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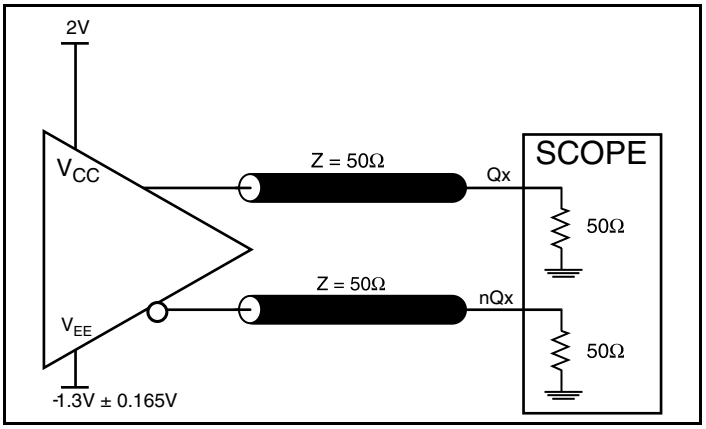
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

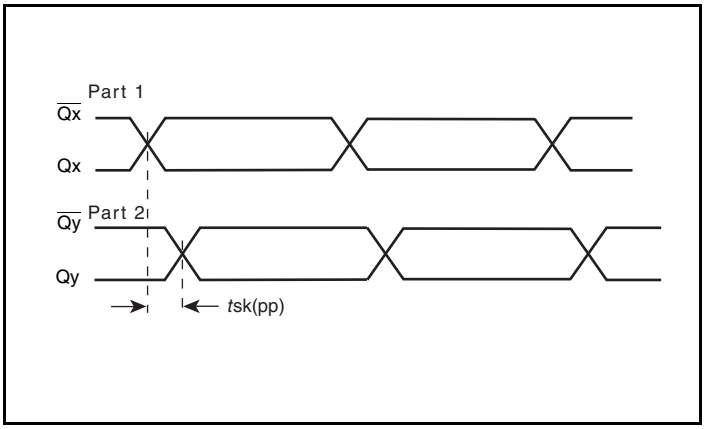


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

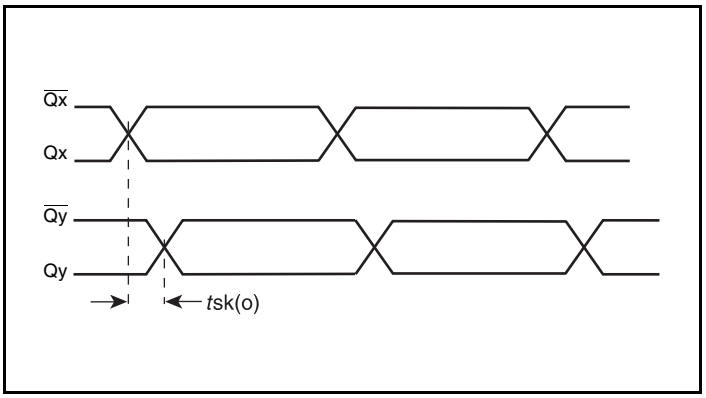
Parameter Measurement Information



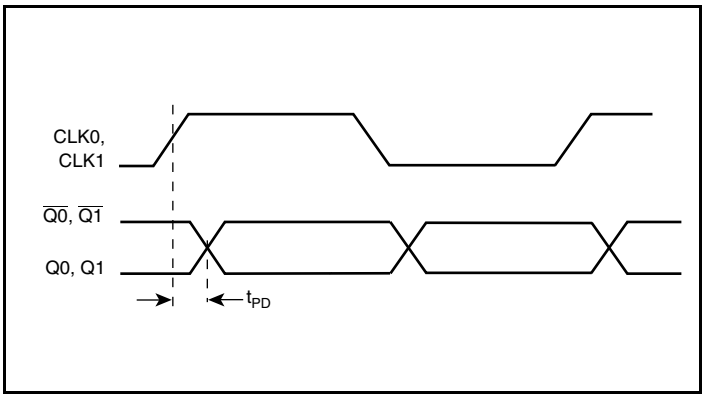
3.3V LVPECL Output Load AC Test Circuit



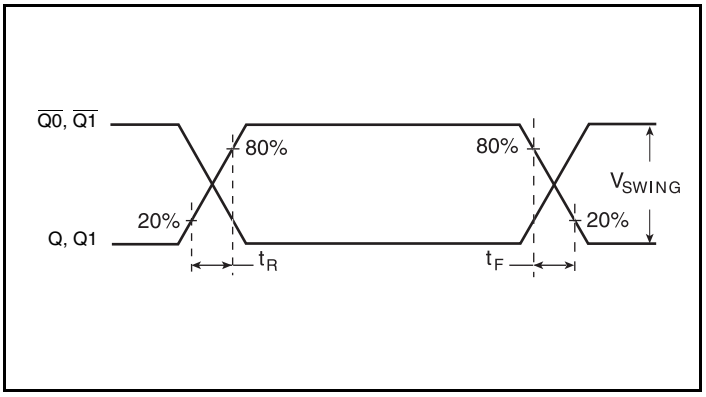
Part-to-Part Skew



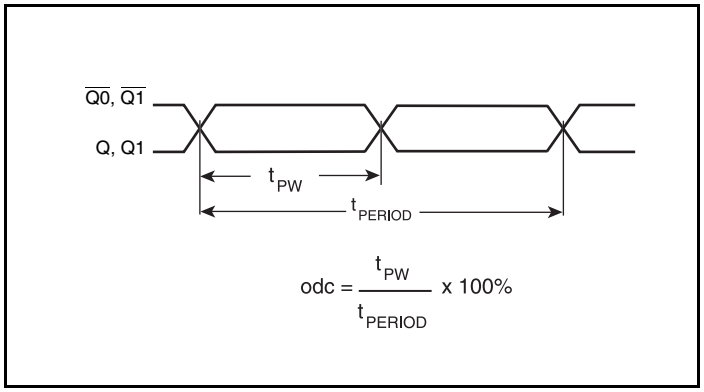
Output Skew



Propagation Delay



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

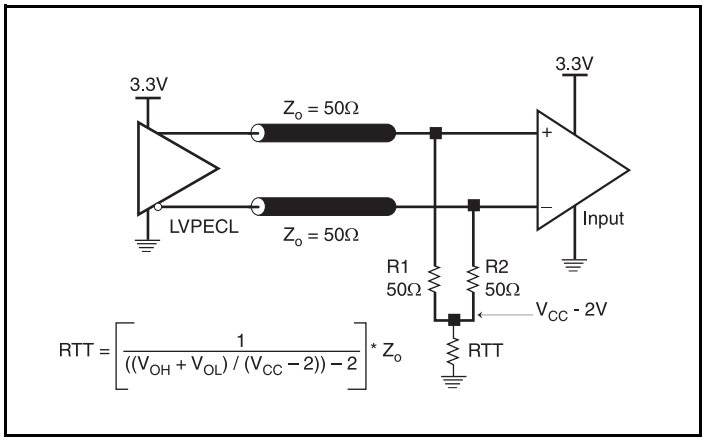


Figure 2A. 3.3V LVPECL Output Termination

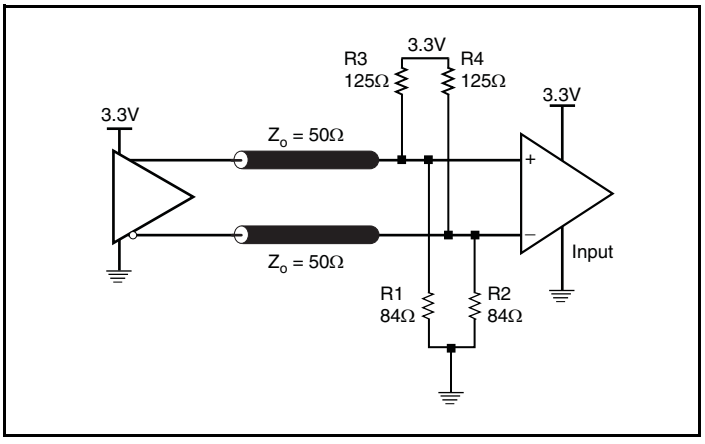


Figure 2B. 3.3V LVPECL Output Termination

Schematic Example

Figure 3 shows a schematic example of the 8535-21. The decoupling capacitors should be physically located near the power pin. For 8535-21, the unused clock outputs can be left floating.

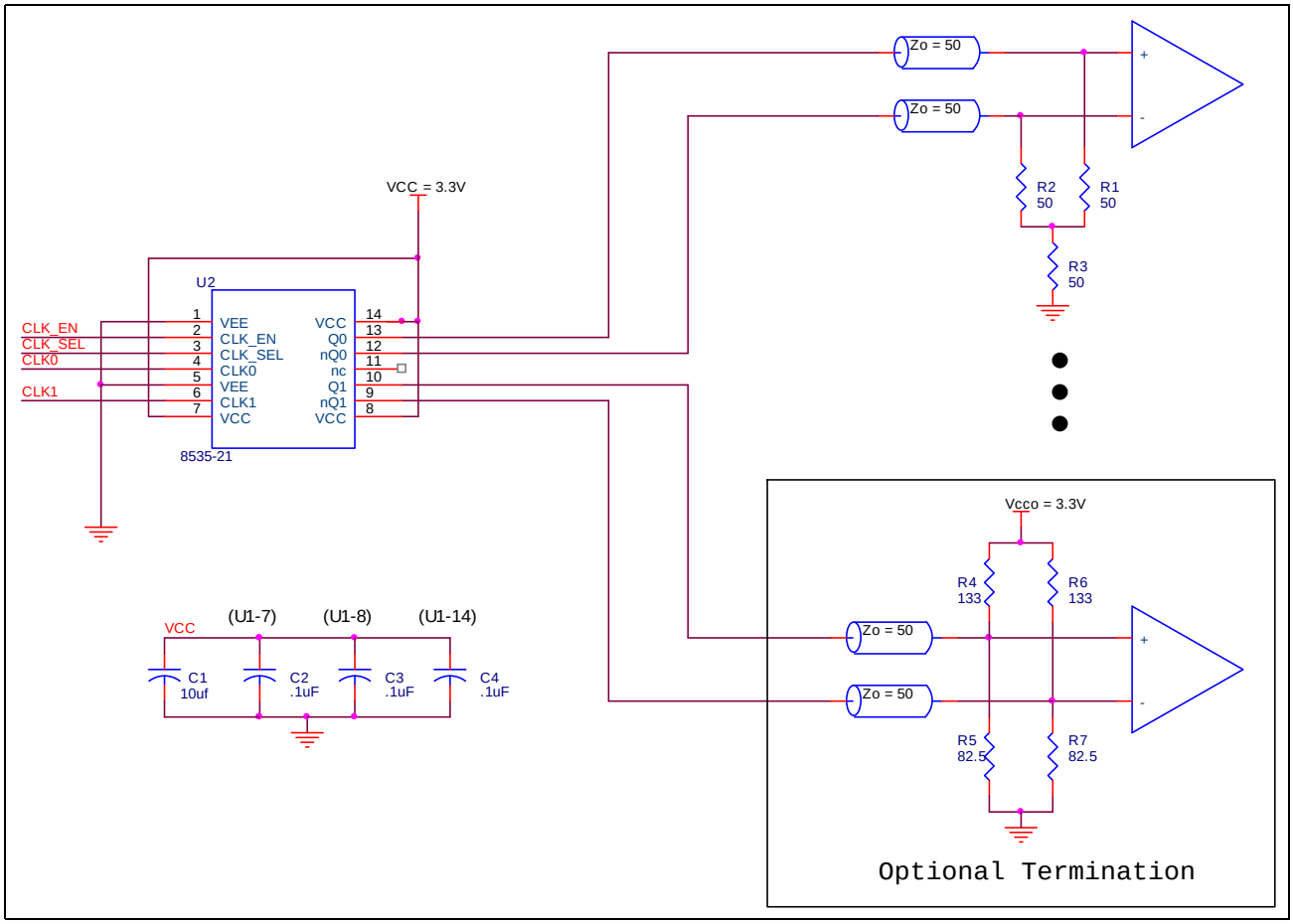


Figure 3. 8535-21 LVPECL Buffer Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8535-21.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8535-21 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.465V * 50mA = **173.25mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power$_{_MAX}$ (3.3V, with all outputs switching) = 173.25mW + 60mW = **233.25mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and it directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 85.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.233W * 85.5°C/W = 90°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resitance θ_{JA} for 48 Lead TQFP, Forced Convection

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	146.4°C/W	125.2°C/W	112.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	93.2°C/W	85.5°C/W	81.2°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

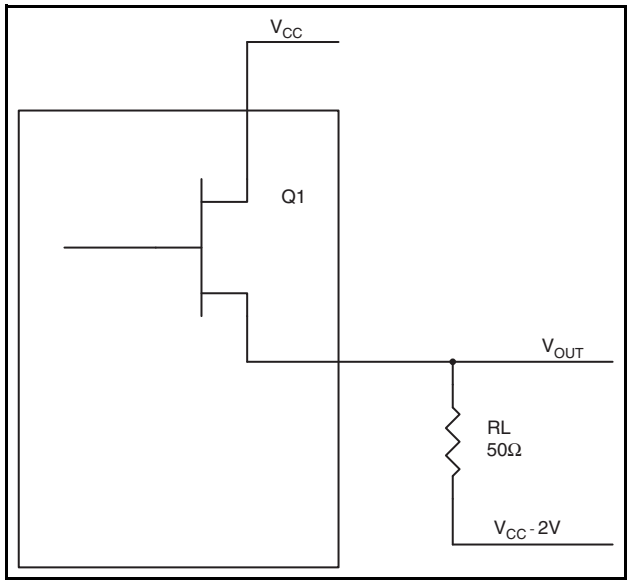


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} – 0.9V}$
  $(V_{CC_MAX} – V_{OH_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} – 1.7V}$
  $(V_{CC_MAX} – V_{OL_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) = [(2V - (V_{CC_MAX} – V_{OH_MAX}))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) = [(2V – (V_{CC_MAX} – V_{OL_MAX}))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 14 Lead TSSOP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	146.4°C/W	125.2°C/W	112.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	93.2°C/W	85.5°C/W	81.2°C/W

Transistor Count

The transistor count for 8535-21 is: 412

Package Outline and Package Dimension

Package Outline - G Suffix for 14 Lead TSSOP

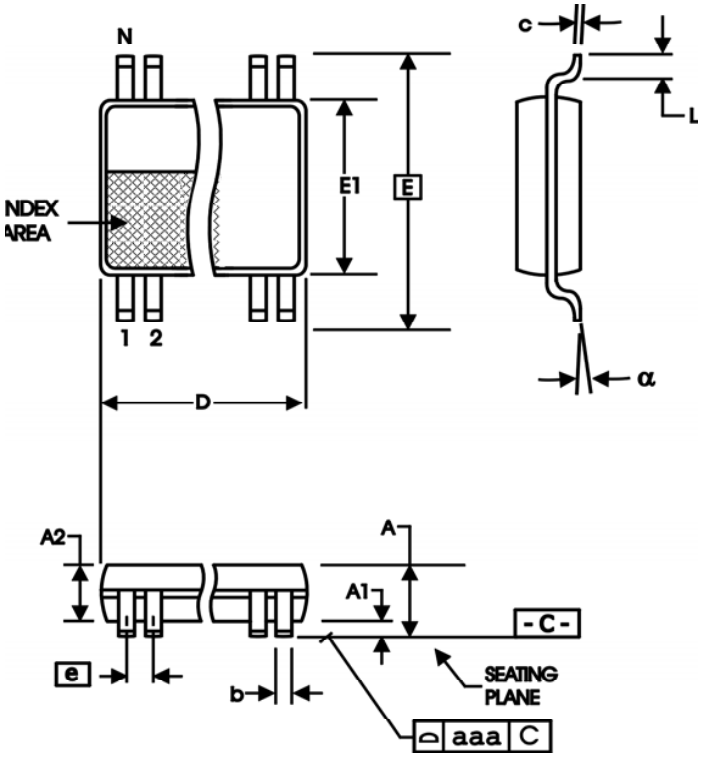


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	14	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8535AG-21LF	8535A21L	14 Lead TSSOP, Lead-Free	Tube	0°C to 70°C
ICS8535AG-21LFT	8535A21L	14 Lead TSSOP, Lead-Free	Tape & Reel	0°C to 70°C

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Features Section - added lead-free bullet.	12/5/05
		8	Added Recommendations for Unused Input and Output Pins.	
	T9	14	Ordering Information Table - added lead-free part number, marking and note.	
A	T9	13	Ordering Information Table - added lead-free marking.	6/4/07
B		1	General Description: deleted *HiperClocks* logo and reference. Features: updated RoHS bullet.	12/8/15
	T5	5	AC Characteristics Table: added general note.	
	T9	13	Ordering Information Table: deleted leaded part rows and note. Deleted all *HiperClocks* references throughout the datasheet. Deleted “ICS” prefix from part number.	

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