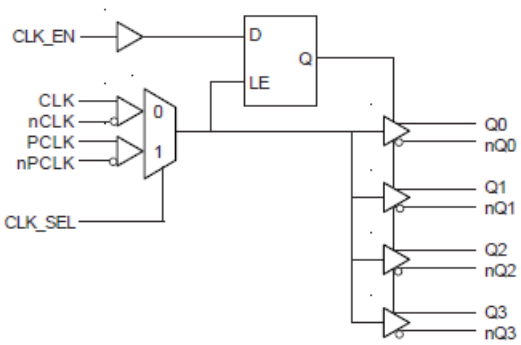
## General Description

The 8533-01 is a low skew, high performance 1-to-4 Differential-to-3.3V LVPECL Fanout Buffer. The 8533-01 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. Guaranteed output and part-to-part skew characteristics make the 8533-01 ideal for those applications demanding well defined performance and repeatability.

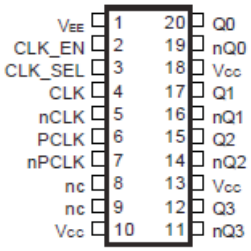
## Features

- Four differential 3.3V LVPECL outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 650MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 30ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 1.4ns (maximum)
- Additive phase jitter, RMS: 0.06ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package
- Industrial temperature information available upon request

## Block Diagram




## Pin Assignment




**8533-01**
**20-Lead TSSOP**
6.5mm x 4.4mm x 0.92mm package body
**G Package**
Top View

**Table 1. Pin Descriptions**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | $V_{EE}$ | Power | | Negative supply pin. |
| 2 | CLK_EN | Input | Pullup | Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels. |
| 3 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects differential PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVCMOS / LVTTL interface levels. |
| 4 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 5 | nCLK | Input | Pullup | Inverting differential clock input. |
| 6 | PCLK | Input | Pulldown | Non-inverting differential LVPECL clock input. |
| 7 | nPCLK | Input | Pullup | Inverting differential LVPECL clock input. |
| 8, 9 | nc | Unused | | No connect. |
| 10, 13, 18 | $V_{CC}$ | Power | | Positive supply pins. |
| 11, 12 | nQ3, Q3 | Output | | Differential output pair. LVPECL interface levels. |
| 14, 15 | nQ2, Q2 | Output | | Differential output pair. LVPECL interface levels. |
| 16, 17 | nQ1, Q1 | Output | | Differential output pair. LVPECL interface levels. |
| 19, 20 | nQ0, Q0 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**Table 2. Pin Characteristics**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

**Table 3A. Control Input Function Table**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| CLK_EN | CLK_SEL | Selected Source | Q0:Q3 | nQ0:nQ3 |
| 0 | 0 | CLK, nCLK | Disabled; LOW | Disabled; HIGH |
| 0 | 1 | PCLK, nPCLK | Disabled; LOW | Disabled; HIGH |
| 1 | 0 | CLK, nCLK | Enabled | Enabled |
| 1 | 1 | PCLK, nPCLK | Enabled | Enabled |

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.
In the active mode, the state of the outputs are a function of the CLK , nCLK and PCLK, nPCLK inputs as described in Table 3B.

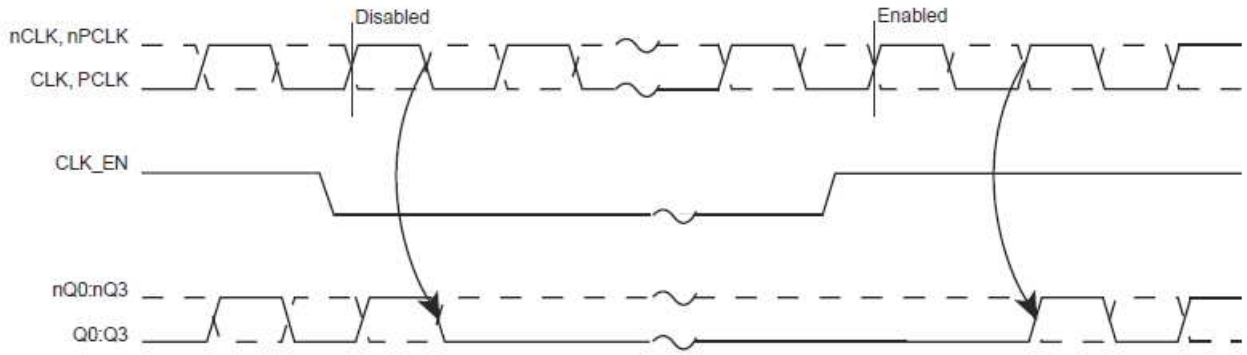



**Figure 1. CLK_EN Timing Diagram**

**Table 3B. Clock Input Function Table**

| Inputs | | Outputs | | Input to Output Mode | Polarity |
|---|---|---|---|---|---|
| CLK or PCLK | nCLK or nPCLK | Q0:Q3 | nQ0:nQ3 | | |
| 0 | 1 | LOW | HIGH | Differential to Differential | Non Inverting |
| 1 | 0 | HIGH | LOW | Differential to Differential | Non Inverting |
| 0 | Biased; NOTE 1 | LOW | HIGH | Single Ended to Differential | Non Inverting |
| 1 | Biased; NOTE 1 | HIGH | LOW | Single Ended to Differential | Non Inverting |
| Biased; NOTE 1 | 0 | HIGH | LOW | Single Ended to Differential | Inverting |
| Biased; NOTE 1 | 1 | LOW | HIGH | Single Ended to Differential | Inverting |

NOTE 1: Please refer to the Application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$ | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**Table 4A. Power Supply DC Characteristics,** $V_{CC}$ = 3.3V±5%, TA = 0°C to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 50 | mA |

**Table 4B. LVCMOS / LVTTL DC Characteristics,** $V_{CC}$ = 3.3V±5%, TA = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{EE}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | CLK_EN | $V_{IN} = V_{CC}$ = 3.465V | | | 5 | µA |
| | | CLK_SEL | $V_{IN} = V_{CC}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK_EN | $V_{IN}$ = 0V, $V_{CC}$ = 3.465V | -150 | | | µA |
| | | CLK_SEL | $V_{IN}$ = 0V, $V_{CC}$ = 3.465V | -5 | | | µA |

**Table 4C. Differential DC Characteristics,** $V_{CC}$ = 3.3V±5%, TA = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | nCLK | $V_{CC} = V_{IN}$ = 3.465V | | | 5 | µA |
| | | CLK | $V_{CC} = V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | nCLK | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| | | CLK | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE}$ + 0.5 | | $V_{CC}$ - 0.85 | V |

NOTE 1: For single ended applications, the maximum input voltage for CLK and nCLK is $V_{CC}$ + 0.3V.
NOTE 2: Common mode voltage is defined as $V_{IH}$.

**TABLE 4D. LVPECL DC CHARACTERISTICS,** $V_{CC}$ = 3.3V±5%, TA = 0°C TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | PCLK | $V_{CC} = V_{IN}$ = 3.465V | | | 150 | µA |
| | | nPCLK | $V_{CC} = V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | PCLK | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nPCLK | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.3 | | 1 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE}$ + 1.5 | | $V_{CC}$ | V |
| $V_{OH}$ | Output High Voltage; NOTE 3 | | | $V_{CC}$ - 1.4 | | $V_{CC}$ - 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 3 | | | $V_{CC}$ - 2.0 | | $V_{CC}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | | 0.6 | | 1.0 | V |

NOTE 1: Common mode voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications the maximum input voltage for PCLK and nPCLK is $V_{CC}$ + 0.3V.
NOTE 3: Outputs terminated with 50Ω to $V_{CC}$ - 2V.

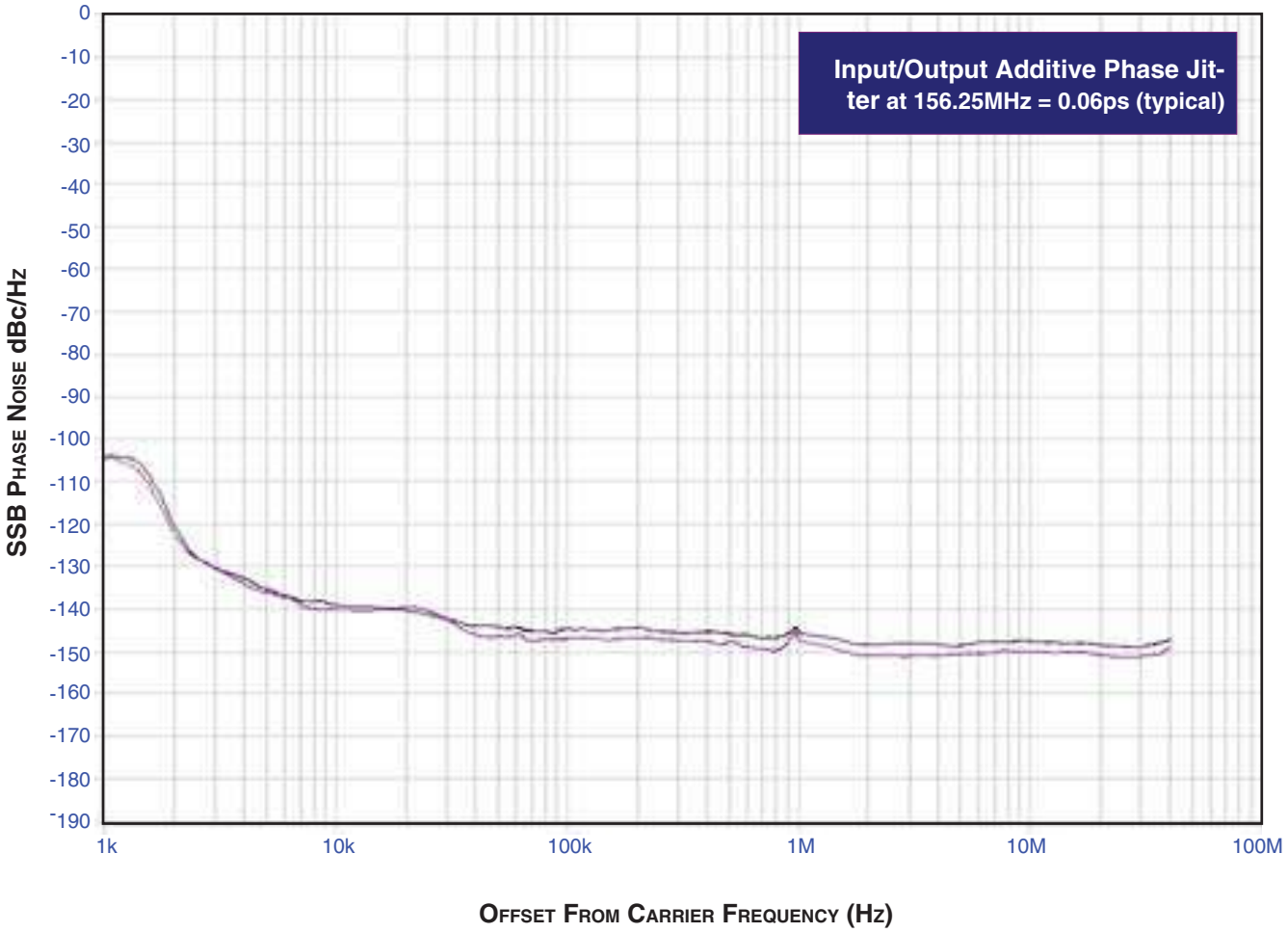
**TABLE 5. AC CHARACTERISTICS,** $V_{CC}$ = 3.3V±5%, TA = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 650 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | $f \leq$ 650MHz | 1.0 | | 1.4 | ns |
| *t*sk(o) | Output Skew; NOTE 2, 4 | | | | 30 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 150 | ps |
| *t*jit | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5 | | | 0.06 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% @ 50MHz | 300 | | 700 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

All parameters measured at 500MHz unless noted otherwise.
The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Driving only one input clock.

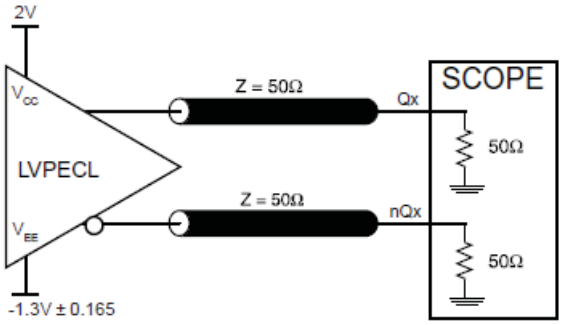
## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

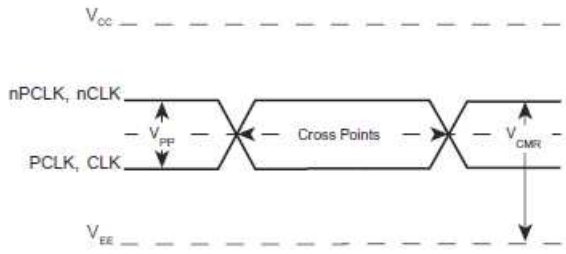



As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

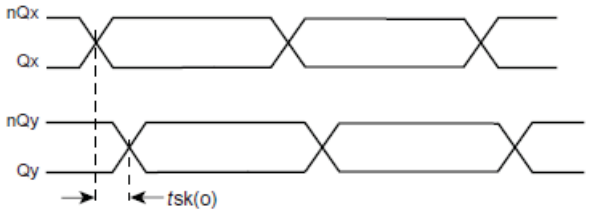
# Parameter Measurement Information



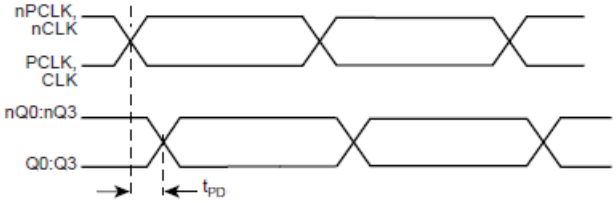

**3.3V Output Load AC Test Circuit**



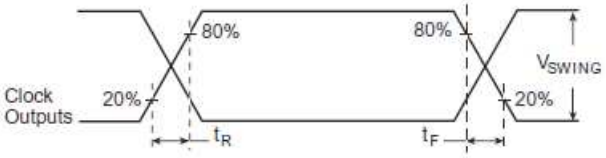

**Differential Input Level**



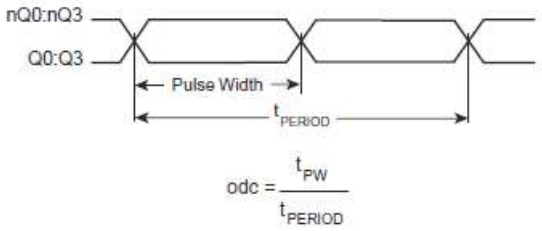

**Output Skew**




**Propagation Delay**




**Output Rise/Fall Time**




**Output Duty Cycle/Pulse Width/Period**

# Application Information

## Wiring the Differential Input to Accept Single Ended Levels

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{CC}$/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC}$ = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

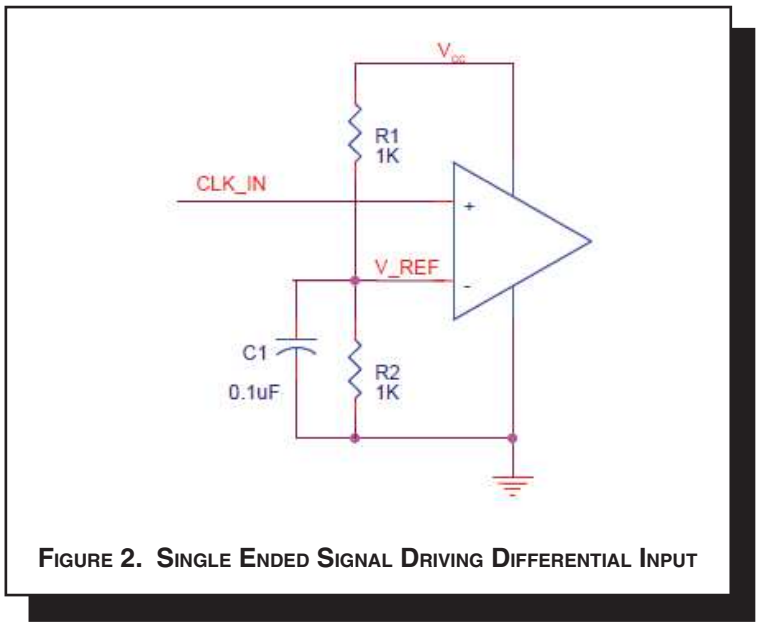



**Figure 2. Single Ended Signal Driving Differential Input**

## Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

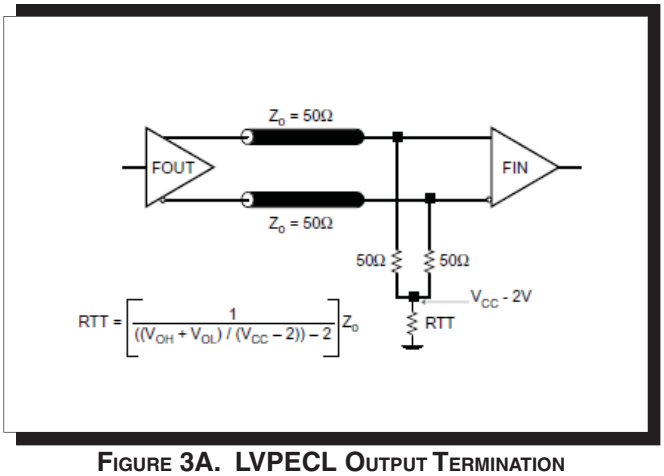



**Figure 3A. LVPECL Output Termination**

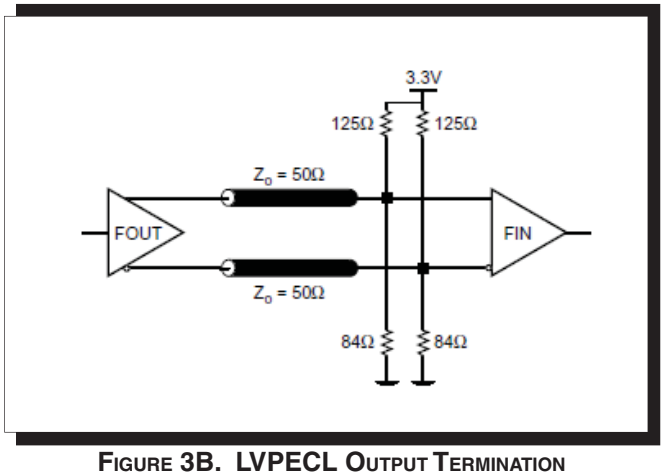



**Figure 3B. LVPECL Output Termination**

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. Figures 4A to 4E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

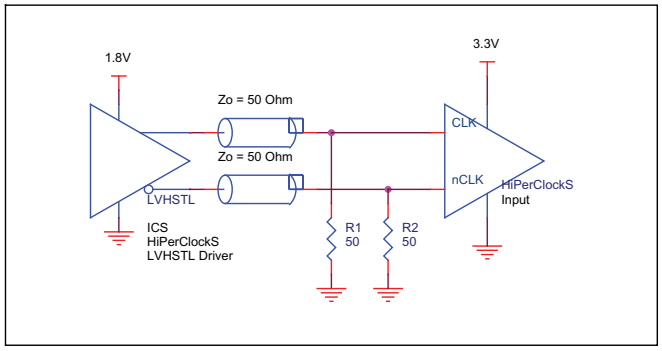



**Figure 4A. CLK/nCLK Input Driven by LVHSTL Driver**

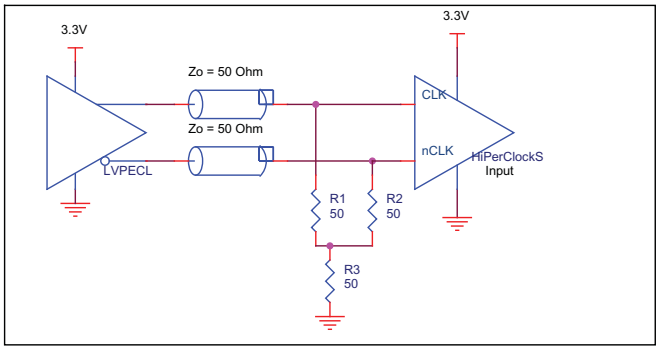



**Figure 4B. CLK/nCLK Input Driven by 3.3V LVPECL Driver**

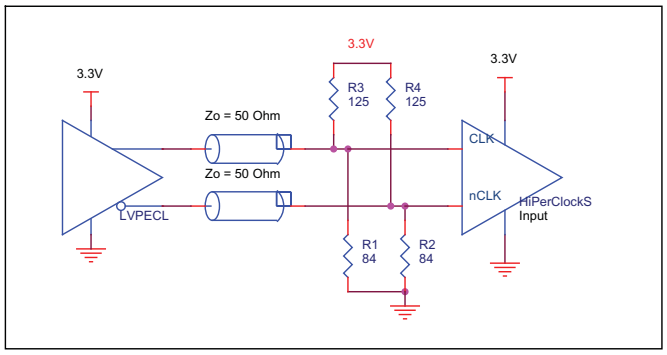



**Figure 4C. CLK/nCLK Input Driven by 3.3V LVPECL Driver**

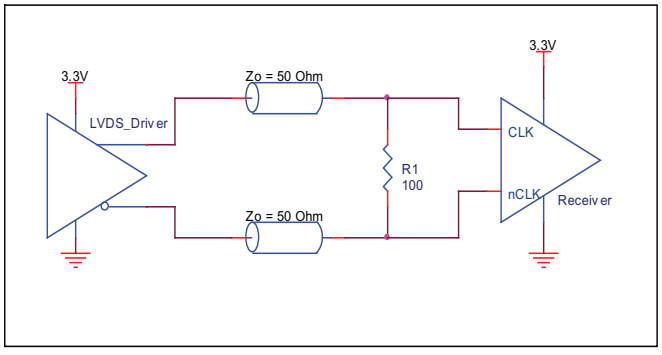



**Figure 4D. CLK/nCLK Input Driven by 3.3V LVDS Driver**

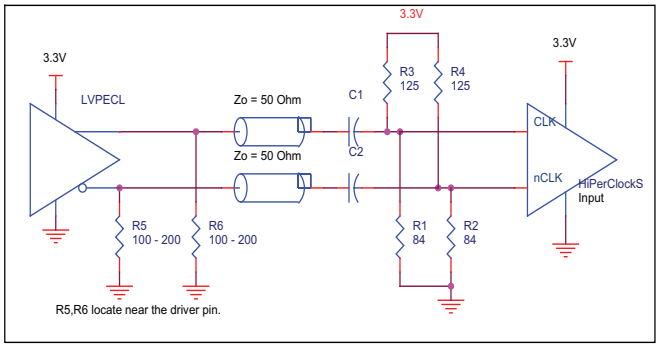



**Figure 4E. CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple**

## LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 5A to 5F* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

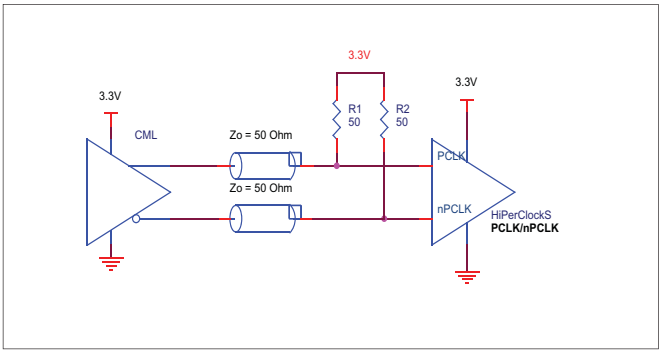



**Figure 5A. PCLK/nPCLK Input Driven by an Open Collector CML Driver**

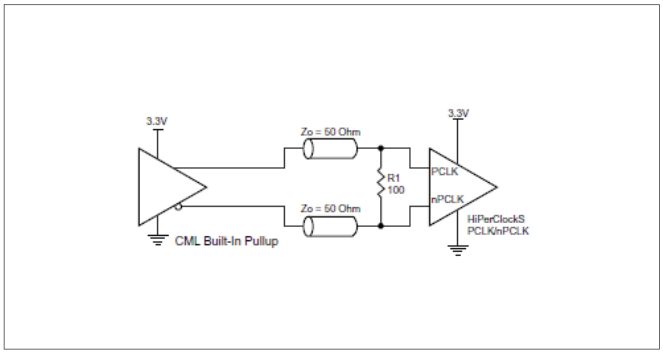



**Figure 5B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver**

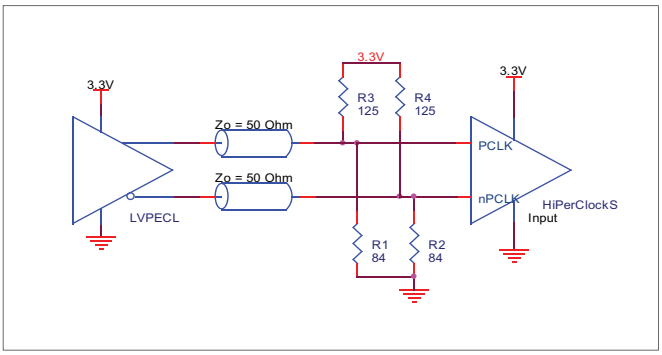



**Figure 5C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**

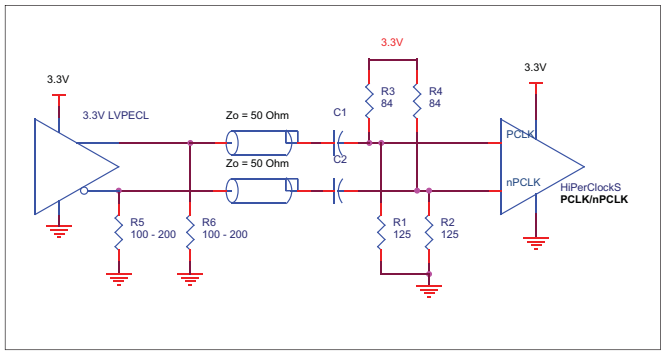



**Figure 5D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**

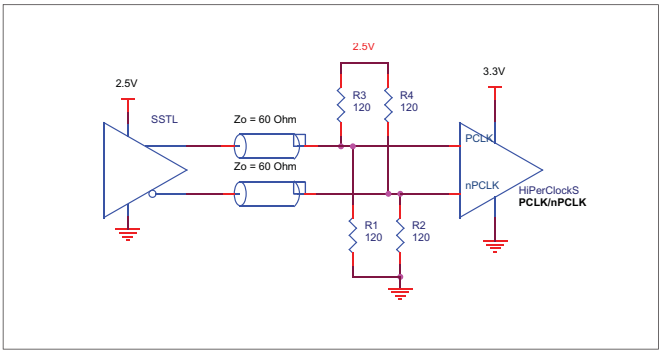



**Figure 5E. PCLK/nPCLK Input Driven by an SSTL Driver**

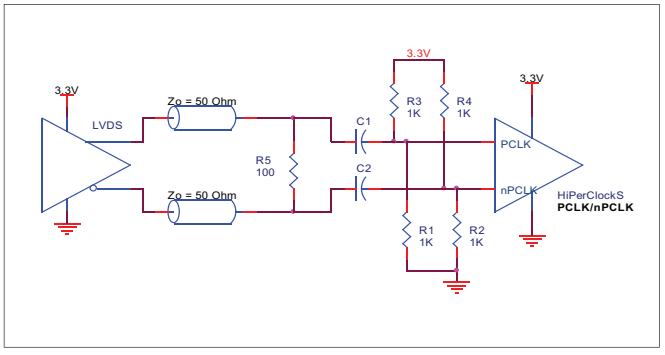



**Figure 5F. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver**

# Power Considerations

This section provides information on power dissipation and junction temperature for the 8533-01.
Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the 8533-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.
**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC_MAX}$ * $I_{EE_MAX}$ = 3.465V * 50mA = **173.3mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

  **Total Power$_{_MAX}$** (3.465V, with all outputs switching) = 173.3mW + 120mW = **293.3mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.293W * 66.6°C/W = 89.5°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**Table 6. Thermal Resistance $\theta_{JA}$ for 20-pin TSSOP, Forced Convection**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | 0 | 200 | 500 |
|---|---|---|---|
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

*3. Calculations and Equations.*

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

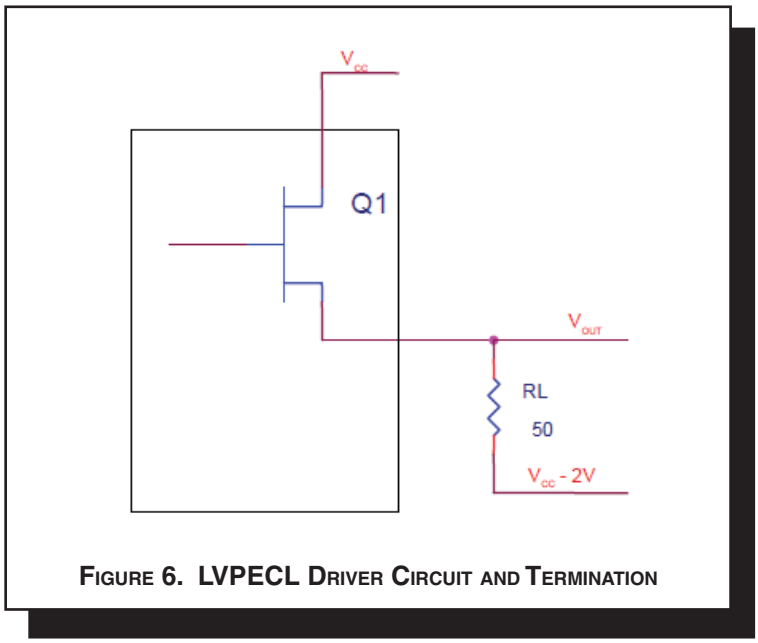



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination
voltage of $V_{CC}$ - 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} – 0.9V}$

  $(V_{CC_MAX} - V_{OH_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} – 1.7V}$

  $(V_{CC_MAX} - V_{OL_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

# Reliability Information

**Table 7. $\theta_{JA}$ vs. Air Flow Table for 20 Lead TSSOP**

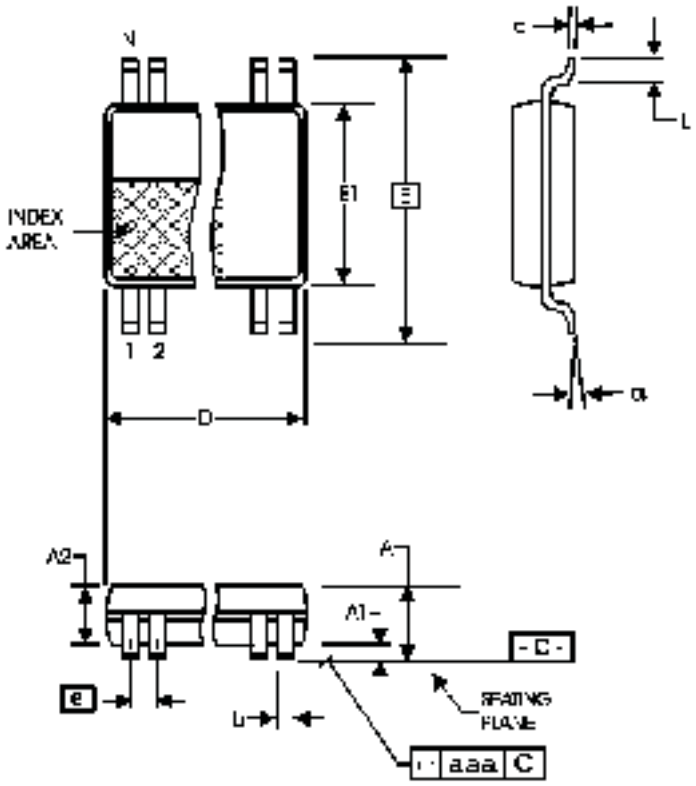
| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### Transistor Count

The transistor count for 8533-01 is: 404

## Package Outline - G Suffix for 20 Lead TSSOP




### Table 8. Package Dimensions

| SYMBOL | Millimeters | |
|---|---|---|
| | Minimum | Maximum |
| N | 20 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-153

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8533AG-01LN | ICS8533A01LN | 20 lead “Lead Free Annealed” TSSOP | Tube | 0°C to +70°C |
| 8533AG-01LNT | ICS8533A01LN | 20 lead “Lead Free Annealed” TSSOP | Tape and Reel | 0°C to +70°C |
| 8533AG-01LF | ICS8533A01LF | 20 lead “Lead Free” TSSOP | Tube | 0°C to +70°C |
| 8533AG-01LFT | ICS8533A01LF | 20 lead “Lead Free” TSSOP | Tape and Reel | 0°C to +70°C |

| REVISION HISTORY SHEET | | | | |
|---|---|---|---|---|
| **Rev** | **Table** | **Page** | **Description of Change** | **Date** |
| B | 4C<br><br><br>4D<br>5 | 4<br><br><br>5<br>5 | $V_{PP}$ values changed from 0.1 Min. to 0.15 Min.<br>$V_{CMR}$ values changed from 0.13 Min., 1.3 Max. to 1.5 Min, $V_{CC}$ Max.<br>Deleted $V_{IH}$ and $V_{IL}$ rows.<br>$t_R$ values changed from 100 Min. to 300 Min, and added 700 Max.<br>$t_F$ values changed from 100 Min., 600 Max. to 300 Min. to 700 Max.<br>For $t_R$ and $t_F$ rows changed test conditions from 30% to 70% to 20% to 80%.<br>tjit(cc) values changed 150 Max. to 0 Max. | 5/22/01 |
| B | 5 | 5 | Deleted $t_S$ and $t_H$ rows. | 6/4/01 |
| B | 4D | 5 | $V_{PP}$ values changed from 0.15 Min., 1.3 Max. to 0.3 Min., 1 Max.<br>$V_{CMR}$ values changed from 1.5 Min., to $V_{EE}$ + 1.5 Min. | 6/28/01 |
| C | 4B<br>5 | 4<br>5 | $V_{IH}$ values changed from 3.765 Max. to $V_{CC}$ + 0.3 Max.<br>Deleted tjit(cc) row. | 10/15/01 |
| C | | 6, 7 | Revised Parameter Measurement diagrams. | 10/18/01 |
| C | | 3 | Updated Figure 1, CLK_EN Timing Diagram. | 11/1/01 |
| C | | 8 | Added Termination for LVPECL Outputs section. | 5/28/02 |
| C | | 6 | Output Load Test Circuit diagram - corrected VEE equation to read,<br>$V_{EE}$ = -1.3V ± 0.165V from $V_{EE}$ = -1.3V ± 0.135V. | 10/03/02 |
| D | <br>T2<br><br>T4D<br>T5 | 1<br>2<br>4<br>5<br>5<br>6<br>8<br>9<br>10 | Added RMS Jitter to Features section.<br>Pin Characteristics Table - changed $C_{IN}$ 4pF max. to 4pF typical.<br>Changed Outputs Absolute Maximum Rating.<br>LVPECL Table - changed VSWING 0.85V max. to 1.0V max.<br>AC Characteristics Table - added RMS jitter.<br>Added Additive Phase Jitter Section.<br>Updated LVPECL Output Termination diagrams.<br>Added Differential Clock Input Interface.<br>Added LVPECL Clock Input Interface.<br>Updated format throughout data sheet. | 10/12/03 |
| D | T9 | 15 | Added Lead Free Annealed part number to Ordering Information table. | 2/9/04 |
| D | <br>T9 | 10<br>15 | Updated LVPECL Clock Input Interface section.<br>Ordering Information Table - added Lead Free part number. | 6/17/04 |
| E | T4D<br><br><br><br><br>T9 | 5<br><br>11 - 12<br><br><br>15 | LVPECL DC Characteristics Table -corrected $V_{OH}$ max. from $V_{CC}$ - 1.0V to $V_{CC}$- 0.9V.<br>Power Considerations - corrected power dissipation to reflect $V_{OH}$ max in Table 4D.<br>Ordering Information Table - added lead-free note. | 4/12/07 |
| F | T9 | 15<br>17 | Updated datasheet's header/footer with IDT from ICS.<br>Removed ICS prefix from Part/Order Number column.<br>Added Contact Page. | 8/4/10 |
| F | T9 | 15 | Removed ICS from part numbers where needed.<br>Ordering Information - removed quantity in tape and reel. Deleted LF note below table.<br>Updated header and footer | 1/19/16 |

**Corporate Headquarters**
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

**Sales**
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

**Tech Support**
www.idt.com/go/support

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