82562G 10/100 Mbps Platform LAN Connect (PLC)

Networking Silicon

Datasheet

Product Features

- IEEE 802.3 10BASE-T/100BASE-TX compliant physical layer interface
- IEEE 802.3u Auto-Negotiation support
- Digital Adaptive Equalization control
- Link status interrupt capability
- XOR tree mode support
- 3-port LED support (speed, link and activity)
- 10BASE-T auto-polarity correction
- LAN Connect Interface
- Diagnostic loopback mode
- 1:1 transmit transformer ratio support
- Low power (less than 300 mW in active transmit mode)
- Reduced power in “unplugged mode” (less than 50 mW)
- Automatic detection of “unplugged mode”
- 3.3 V device
- Lead-free[1] 48-pin Shrink Small Outline Package for both leaded and lead-free designs. (Devices that are lead-free are marked with a circled “e3” and have the product code prefix: LUxxxxxx).

[1] This device is lead-free. That is, lead has not been intentionally added, but lead may still exist as an impurity at <1000 ppm. The Material Declaration Data Sheet, which includes lead impurity levels and the concentration of other Restriction on Hazardous Substances (RoHS)-banned materials, is available at:
`ftp://download.intel.com/design/packtech/material_content_IC_Package.pdf#pagemode=bookmarks`
In addition, this device has been tested and conforms to the same parametric specifications as previous versions of the device.

For more information regarding lead-free products from Intel Corporation, contact your Intel Field Sales representative.

Additional Features

- The 82562G PLC supports drop-in replacement with the 82562ET. If it is not used as a drop-in replacement, strapping options enable new operating modes:
  - —LED support for three logic configurations.
  - —LAN disable function using one pin.
  - —Increased transmit strength.
- The receive BER performance increases the margin for cable length.
- Return Loss performance is improved.

Revision 1.3
April 2005

Revision History

Revision	Revision Date	Description
1.0	October 2004	Initial release (confidential status).
1.1	November 2004	• Updated lead-free device information. • Updated Table 1 and Table 2 to reflect correct hardware configurations and LED logic functionality. • Corrected signal names to match design guide and reference schematics.
1.2	January 2005	• Added a note for PHY signals RBIAS100 and RBIAS10 to Section 4.3.
1.3	April 2005	• Added internal/external pull-up/pull-down resistor values to the Hardware Configuration table and signal definition tables for TESTEN, ISOL_EXEC, ISOL_TI, ISOL_TCK, and ADV10/LAN_DISABLE#

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The 82562G PLC may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at http://www.intel.com.

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1.0 Introduction

This document is applicable to the Intel® 82562G 10/100 Mbps Platform LAN Connect device, a member of the 82562G Fast Ethernet device family.

1.1 Overview

The Intel® 82562G 10/100 Mbps Platform LAN Connect is a highly-integrated device designed for 10 or 100 Mbps Ethernet systems. It is based on the IEEE 10BASE-T and 100BASE-TX standards. The IEEE 802.3u standard for 100BASE-TX defines networking over two pairs of Category 5 unshielded twisted pair cable or Type 1 shielded twisted pair cable.

The 82562G complies with the IEEE 802.3u Auto-Negotiation standard and the IEEE 802.3x Full Duplex Flow Control standard. The 82562G also includes a PHY interface compliant to the current platform LAN connect interface.

1.2 References

- IEEE 802.3 Standard for Local and Metropolitan Area Networks, Institute of Electrical and Electronics Engineers.
- 82562ET(EM) and 82562GT(G) LAN on Motherboard Design Guide. Intel Corporation.
- Intel® I/O Controller Hub 6 (ICH6) Family External Design Specification (EDS), Volume 1, Revision 1.5V1. Intel Corporation.
- Intel® I/O Controller Hub 6 (ICH6) Family External Design Specification (EDS), Volume 2, Revision 1.5V2. Intel Corporation.
- LAN Connect Interface Specification. Intel Corporation.
- I/O Control Hub 2, 3, and 4 EEPROM Map and Programming Information. Intel Corporation.
- I/O Control Hub 5, 6, and 7 EEPROM Map and Programming Information. Intel Corporation.

Programming information can be obtained through your local Intel representatives.

1.3 Product Codes

The product ordering code for the 82562G is: EP82562G.

The product ordering code for the 82562G lead-free version is: LU82562G.

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2.0 82562G Architectural Overview

The 82562G PLC is a 3.3 V device in a 48-pin Shrink Small Outline Package (SSOP) that is designed to work only in Data Terminal Equipment (DTE) mode. In normal operating mode, the 82562G incorporates all active circuitry required to interface with the Intel® ICHx device with an integrated 10/100 Mbps LAN controller. The 82562G supports a direct interface to all Media Access Control (MAC) components that meet the Platform LAN connect interface specification. Figure 1 shows a block diagram of the 82562G architecture.

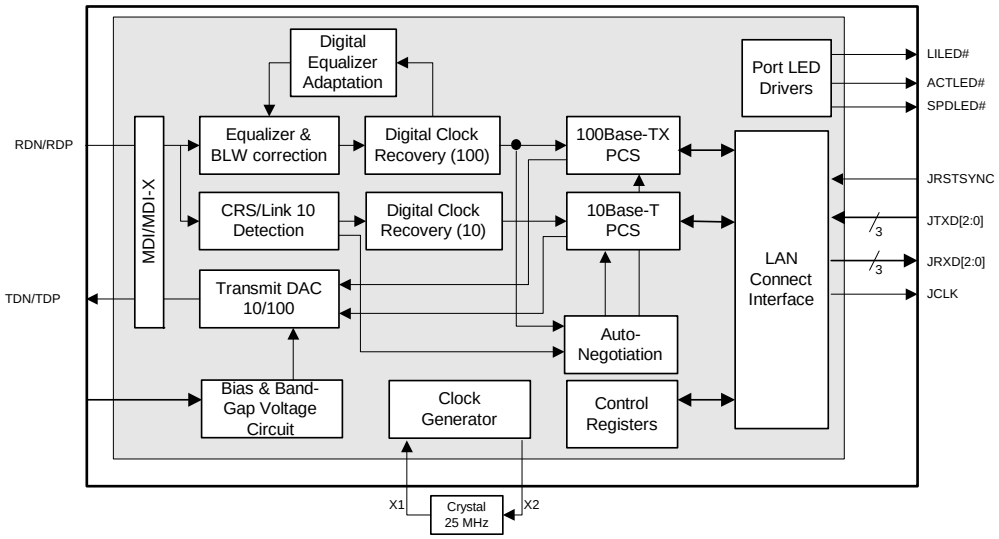


Figure 1. 82562G PLC Block Diagram

2.1 LAN Connect Interface

The 82562G supports a LAN Connect Interface (LCI) as specified in the LCI Specification. The LAN Connect is the I/O Control Hub 2 (ICH2) interface to the 82562G. The LCI uses an 8-pin interface, which reduces the pin count from 15, for an Media Independent Interface (MII) PHY. In addition, its signaling protocol provides greater functionality, such as dynamic power reduction, from a PLC in comparison to a standard MII PHY.

Figure 2 shows how the 82562G can be used in a 10/100 Mbps ICHx design.

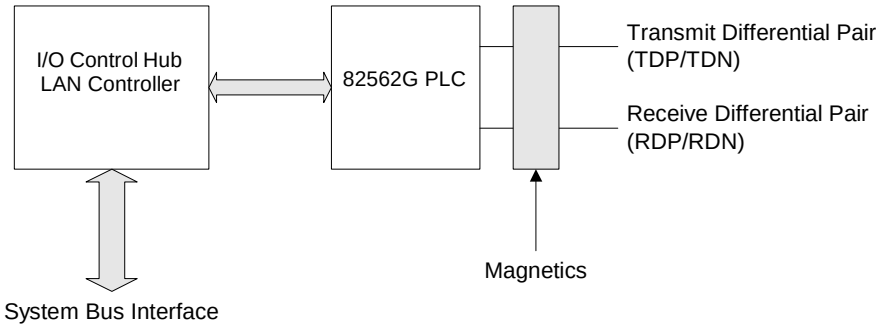


Figure 2. 82562G PLC 10/100 Mbps Ethernet Solution

2.1.1 Reset/Synchronize Operations

The Reset/Synchronize signal used by the LAN Connect Interface is driven by the ICHx integrated LAN device. It has two functions:

- Synchronize. When this pin is activated synchronously for only one LAN connect clock, it is used for synchronization between the ICHx integrated LAN and PHY on LAN connect word boundaries.
- Reset. When this pin is asserted beyond one LAN connect clock, the 82562G uses this signal as a reset signal. To ensure a reset of the 82562G, the reset should remain active for at least 500 µs.

2.1.2 Reset Considerations

When the 82562G Reset signal (JRSTSYNC) is asserted for at least 500 µs, all internal circuits are reset. The 82562G can also be reset by setting the MII register Reset bit equal to 1 (Register 0, bit 15).

The 82562G filters out JRSTSYNC pulses with a width of less than 200 ns to distinguish between a reset and synchronize pulse. Again, the Reset signal should be longer than 500 µs to reset the 82562G.

2.1.3 LAN Connect Clock Operations

The 82562G drives the Platform LAN Connect clock (JCLK) at one of two possible frequencies depending upon its operation speed. When the 82562G is in 100BASE-TX mode it drives JCLK at 50 MHz. When the 82562G is in 10BASE-T mode it drives JCLK at 5 MHz. The LAN Connect clock does not stop during normal operation under any conditions. In reduced power mode, the 82562G drives JCLK at 5 MHz, which is required for proper filtering of incoming packets for applications such as Wake on LAN (WoL).

2.2 Hardware Configuration

Four pins, Test Enable (TESTEN), Test Clock (ISOL_TCK), Test Input (ISOL_TI), and Test Execute (ISOL_EXEC), define the general operation of the 82562G. Table 1 lists the pin settings for the different modes of operation.

Table 1. 82562G Hardware Configuration

TESTEN	ISOL_TCK	ISOL_TI	ISOL_EXEC	Mode	Comments
0	0	0	0	82562G family Mode 0: • LEDs are 82562E-compatible (“A” configuration) • LAN_DISABLE# pin is used as ADV10 (auto-negotiation advertise 10M only) Alternative Mode: drop-in replacement for existing 82562E-based designs	The ISOL_TCK, ISOL_TCI, and ISOL_EXEC, and ADV10/ LAN_DISABLE# pins have internal 10 K Ω pull-down resistors and should not be connected for Mode 0 (refer to Table 2). For the alternative 82562E drop-in replacement mode, pins may optionally be used as a LAN disable.
0	0	1	1	82562G family Mode 1: • LEDs are in configuration B • LAN_DISABLE# pin is single pin LAN disable (tri-state and full power down function)	The ISOL_TCK pin has an internal 10 K Ω pull-down resistor and should not be connected for Mode 1 (refer to Table 2).
0	1	1	1	Isolate	Tri-state and power down.
1	0	1	0	Testing Mode	
1	0	0	0	XOR Tree	Board testing plus tri-state.
1	0	0	1	82562G family Mode 2: Same as 0011 except that LEDs are in configuration C	The ISOL_TCK and ISOL_TI pins have 10 K Ω internal pull-down resistors and should not be connected for Mode 2 (refer to Table 2).
1	0	1	1	82562G family Mode 3: Same as 0011 except enhance Tx rise and fall times.	The ISOL_TCK pin has an internal 10 K Ω pull-down resistor and should not be connected for Mode 3.
1	1	0	0	82562G family Mode 4: Same as 1001 except Enhance Tx rise and fall times.	The ISOL_TI and ISOL_EXEC pins have internal 10 K Ω pull-down resistors and should not be connected for Mode 4.

Table 1. 82562G Hardware Configuration

TESTEN	ISOL _TCK	ISOL _TI	ISOL_ EXEC	Mode	Comments
1	1	0	1	Reserved	The ISOL_TI pin has an internal 10 K Ω pull-down resistor and should not be connected.
1	1	1	0	Reserved Testing	The ISOL_EXEC pin has an internal 10 K Ω pull-down resistor and should not be connected.
1	1	1	1	Power-down Mode	Tri-state and power down.

NOTE: Combinations not shown in Table 1 are reserved and should not be used.

Table 2. LED Logic Functionality

Mode/Configuration	ACTLED#	SPDLED#	LILED#
Configuration A: 82562ET-compatible	Activity	Speed 100 Mb	Asserted if valid link is present at 10 Mb or 100 Mb
Configuration B: Intel GbE mode	Activity	Link and Speed 100 Mb	Asserted if valid link is present at 10 Mb or 100 Mb
Configuration C: Alternative mode	Activity	Link and Speed 100 Mb	Link and Speed 10 Mb

3.0 Performance Enhancements

3.1 New Usage Modes: 1, 2, 3, and 4

82562G supports several new features that offer design flexibility and reduced BOM cost compared to the 82562ET PLC device. To implement these new features, a board design must include the proper pull-up and/or pull-down strapping resistor options. Refer to the *82562GT/82562GZ/82562GX/82562G LAN on Motherboard Design Guide* for more information. Table 3 lists the four new modes.

Table 3. Usage Modes 1, 2, 3, and 4

Mode	Benefit
Mode 0: 82562ET compatible.	No BOM changes necessary for equivalent performance to 82562ET.
Mode 1: LED configuration B and single-pin LAN disable.	Usability and reduced BOM cost.
Mode 2: Same as mode 1, except LED configuration C.	Usability and reduced BOM cost.
Mode 3: LED configuration B, Single Pin LAN Disable, and enhanced Tx mode[a]	Usability, reduced BOM cost, and stronger Tx drive strength. Refer to Section 3.1.2.
Mode 4: Same as mode 3, except LED configuration C. See table note a.	Usability, reduced BOM cost, and stronger Tx drive strength. Refer to Section 3.1.2.

a. Only use this mode if advised to do so by an Intel representative to compensate for board design issues affecting IEEE compliance.

3.1.1 Pin Usage for Modes 1, 2, 3, and 4

To use modes 1, 2, 3, or 4, the following pins need to be reviewed (refer to Table 1):

- ISOL_TCK
- ISOL_TI
- ISOL_EX
- TESTEN
- ADV10/LAN_DISABLE# and supporting circuits
- ACTLED#, SPDLED#, and LILED# and supporting circuits

3.1.2 Enhanced Tx Mode

The enhanced Tx mode speeds up the rise and fall times of the 100 Mb signal. This was done so the 82562G can have improved IEEE PHY conformance requirements over a more capacitive Analog Front End (AFE); usually caused by long traces or differential switches that customers use, usually on mobile platforms. However, running an 82562G device in enhanced mode increases the radiated emissions seen from the LAN solution. The increase in radiated emissions may or may not impact the DUT's ability to pass regulatory requirements, as it will depend largely on the design of the AFE. The enhanced mode should only be used when 100Base-TX rise/fall times cannot be met in the normal 82562G mode. Consult an Intel representative if you are considering using this mode.

4.0 82562G Signal Descriptions

4.1 Signal Type Definitions

Type	Name	Description
I	Input	Input pin to the 82562G.
O	Output	Output pin from the 82562G.
I/O	Input/Output	Multiplexed input and output pin to and from the 82562G.
MLT	Multi-level analog I/O	Multi-level analog pin used for input and output.
B	Bias	Bias pin used for ground connection through a resistor or an external voltage reference.
DPS	Digital Power Supply	Digital power or ground pin for the 82562G.
APS	Analog Power Supply	Analog power or ground pin for the 82562G.

4.2 Twisted Pair Ethernet (TPE) Pins

Pin Name	Pin Number	Type	Description
TDP TDN	10 11	MLT	**Transmit Differential Pair.** The transmit differential pair sends serial bit streams to the unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T (Manchester) mode and a three-level signal in 100BASE-TX mode (MLT-3). These signals directly interface with the isolation transformer.
RDP RDN	15 16	MLT	**Receive Differential Pair.** The receive differential pair receive the serial bit stream from an unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T mode (Manchester) or a three-level signal in 100BASE-TX mode (MLT-3). These signals directly interface with an isolation transformer.

4.3 External Bias Pins

Pin Name	Pin Number	Type	Description
RBIAS10	4	B	**Reference Bias Resistor (100 Mbps).** This pin should be connected to a pull-down resistor.[a]
RBIAS100	5	B	**Reference Bias Resistor (10 Mbps).** This pin should be connected to a pull-down resistor.[a]

a. Based on some board designs, RBIAS100 and RBIAS10 values may need to be increased/decreased to compensate for high/low MDI transmit amplitude. See the *82562G/GT and 82562ET/EM LAN on Motherboard Design Guide* for more information.

4.4 Clock Pins

Pin Name	Pin Number	Type	Description
X1	46	I	**Crystal Input Clock.** X1 and X2 can be driven by an external 25 MHz crystal of 30 PPM or better. Otherwise, X1 is driven by an external metal-oxide semiconductor (MOS) level 25 MHz oscillator when X2 is left floating.
X2	47	O	**Crystal Output Clock.** X1 and X2 can be driven by an external 25 MHz crystal of 30 PPM or better.

4.5 Platform LAN Connect Interface Pins

Pin Name	Pin Number	Type	Description
JCLK	39	O	**LAN Connect Clock.** The LAN Connect Clock is driven by the 82562G on two frequencies depending on operation speed. When the 82562G is in 100BASE-TX mode, JCLK drives a 50 MHz clock. Otherwise, JCLK drives a 5 MHz clock for 10BASE-T. The JCLK does not stop during normal operation.
JRSTSYNC	42	I	**Reset/Synchronize.** This is a multiplexed pin and is driven by the Media Access Control (MAC) layer device. Its functions are: • Reset. When this pin is asserted beyond one LAN Connect clock period, the 82562G uses this signal Reset. To ensure reset of the 82562G, the Reset signal should remain active for at least 500 µs. • Synchronize. When this pin is activated synchronously, for only one LAN Connect clock period, it is used to synchronize the MAC and PHY on LAN Connect word boundaries.
JTXD[2:0]	45, 44, 43	I	**LAN Connect Transmit Data.** The LAN Connect transmit pins are used to transfer data from the MAC device to the 82562G. These pins are used to move transmitted data and real time control and management data. They also transmit out of band control data from the MAC to the PHY. The pins should be fully synchronous to JCLK.
JRXD[2:0]	37, 35, 34	O	**LAN Connect Receive Data.** The LAN Connect receive pins are used to transfer data from the 82562G to the MAC device. These pins are used to move received data and real time control and management data. They also move out of band control data from the PHY to the MAC. These pins are synchronous to JCLK.

4.6 LED Pins

Pin Name	Type	Description
LILED#	O	**Link Integrity LED.** The LILED# signal has three logic modes. The LED configurations are listed in Table 2, “LED Logic Functionality”.
ACTLED#	O	**Activity LED.** The LED is active low and the Activity LED signal indicates either receive or transmit activity. When no activity is present, the LED is off. The Activity LED will flicker when activity is present. The flicker rate depends on the activity load. If Address Matching mode is enabled by the MAC, this pin will also indicate address match events on previously received frames.
SPDLED#	O	**Speed LED.** The SPDLED# signal has three logic modes. The LED configurations are listed in Table 2, “LED Logic Functionality”.

4.7 Miscellaneous Control Pins

Pin Name	Type	Description
ADV10/ LAN_DISABLE#	I	**Advertise 10 Mbps Only.** The Advertise 10 Mbps Only signal is asserted high, and the 82562G advertises only 10BASE-T technology during Auto-Negotiation processes in this state. Otherwise, the 82562G advertises all of its technologies. Note: ADV10 has an internal 10 K Ω pull-down resistor. **LAN Disable in 82562G Mode.** In the 82562G operating mode, this pin is used as a LAN disable signal. When it is driven low, the device is fully powered down.
ISOL_TCK	I	**Test Clock.** The Test Clock signal sets the device into asynchronous test mode in conjunction with the Test Input, Test Execute and Test Enable pins (refer to Table 1, “82562G Hardware Configuration”). In the manufacturing test mode, it acts as the test clock. Note: ISOL_TCK has an internal 10 K Ω pull-down resistor.
ISOL_TI	I	**Test Input.** The Test Input signal sets the device into asynchronous test mode in conjunction with the Test Clock, Test Execute and Test Enable pins (refer to Table 1, “82562G Hardware Configuration”). In the manufacturing test mode, it acts as the test data input pin. Note: ISOL_TI has an internal 10 K Ω pull-down resistor.
ISOL_EXEC	I	**Test Execute.** The Test Execute signal sets the device into asynchronous test mode in conjunction with the Test Clock, Test Input, and Test Enable pins (refer to Table 1, “82562G Hardware Configuration”). In the manufacturing test mode, it places the command that was entered through the TI pin in the instruction register. Note: ISOL_EXEC has an internal 10 K Ω pull-down resistor.
TOUT	O	**Test Output.** The Test Output pin is used for Boundary XOR scan output. In the manufacturing test mode, it acts as the test output port.
TESTEN	I	**Test Enable.** The Test Enable pin is used to enable test mode and should be externally pulled up to V_{CC} using a 200 Ω resistor to allow XOR Tree test mode.

4.8 Power and Ground Connections

Pin Name	Pin Number	Type	Description
VCC VCCP VCCA VCCA2 VCCT	1, 25 36, 40 2, 7, 9, 12, 14, 17	DPS	**Digital 3.3 V Power.** These pins should be connected to the main digital power supply.
VSS VSSP VSSA VSSA2	8, 13, 18 24, 48 33, 38 3 6	DPS	**Digital Ground.** These pins should be connected to the main digital ground.
VCCR	19, 23	APS	**Analog Power.**
VSSR	20, 22	APS	**Analog Ground.** These pins should not be isolated from the main digital.

5.0 Physical Layer Interface Functionality

The 82562G supports a direct glueless interface to all components that comply with the LAN Connect specification.

5.1 100BASE-TX Mode

5.1.1 100BASE-TX Transmit Blocks

The transmit subsection of the 82562G accepts 3 bit wide data from the LAN Connect unit. Another subsection passes data unconditionally to the 4B/5B encoder.

The 4B/5B encoder accepts nibble-wide data (4 bits) from the CSMA unit and compiles it into 5-bit-wide parallel symbols. These symbols are scrambled and serialized into a 125 Mbps bit stream, converted by the analog transmit driver into a MLT-3 waveform format, and transmitted onto the Unshielded Twisted Pair (UTP) or Shielded Twisted Pair (STP) wire.

5.1.1.1 100BASE-TX 4B/5B Encoder

The 4B/5B encoder complies with the IEEE 802.3u 100BASE-TX standard. Four bits are encoded according to the transmit 4B/5B lookup table. The lookup table matches a 5-bit code to each 4-bit code. The table below illustrates the 4B/5B encoding scheme associated with the given symbol.

Table 4. 4B/5B Encoder

Symbol	5B Symbol Code	4B Nibble Code
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
I	11111	Inter Packet Idle Symbol (No 4B)

Symbol	5B Symbol Code	4B Nibble Code
J	11000	1st Start of Packet Symbol 0101
K	10001	2nd Start of Packet Symbol 0101
T	01101	1st End of Packet Symbol
R	00111	2nd End of Packet Symbol and Flow Control
V	00000	INVALID
V	00001	INVALID
V	00010	INVALID
V	00011	INVALID
H	00100	INVALID
V	00101	INVALID
V	00110	INVALID
V	01000	INVALID
V	01100	INVALID
V	10000	Flow Control S
V	11001	INVALID

5.1.1.2 100BASE-TX Scrambler and MLT-3 Encoder

Data is scrambled in 100BASE-TX in order to reduce electromagnetic emissions during long transmissions of high-frequency data codes. The scrambler logic accepts 5 bits from the 4B/5B encoder block and presents the scrambled data to the MLT-3 encoder. The 82562G implements the 11-bit stream cipher scrambler as adopted by the ANSI XT3T9.5 committee for UTP operation. The cipher equation used is:

$$X[n] = X[n-11] + X[n-9] \pmod 2$$

The MLT-3 encoder receives the scrambled Non-Return to Zero (NRZ) data stream from the scrambler and encodes the stream into MLT-3 for presentation to the driver. MLT-3 is similar to NRZ1 coding, but three levels are output instead of two. The three output levels are positive, negative and zero. When an NRZ “0” arrives at the input of the encoder, the last output level is maintained (either positive, negative or zero). When an NRZ “1” arrives at the input of the encoder, the output steps to the next level. The order of steps is negative-zero-positive-zero which continues periodically. Refer to IEEE 802.3 Specification for details.

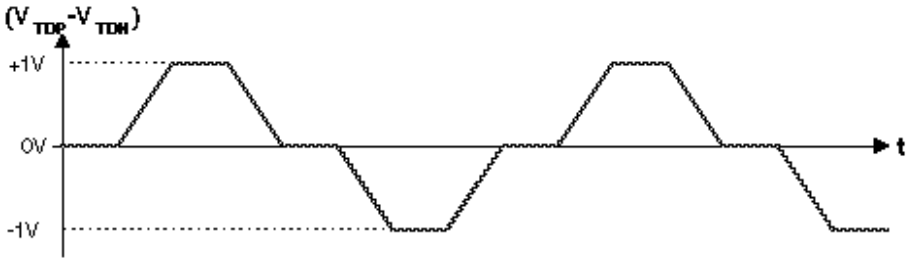
5.1.1.3 100BASE-TX Transmit Framing

The 82562G does not differentiate between the fields of the MAC frame containing preamble, start of frame delimiter, data and Cyclic Redundancy Check (CRC). The 82562 encodes the first byte of the preamble as the “JK” symbol, encodes all other pieces of data according to the 4B/5B lookup table, and adds the “TR” code after the end of the packet. The 82562 scrambles and serializes the data into a 125 Mbps stream, encodes it as MLT-3, and drives it onto the wire.

5.1.1.4 Transmit Driver

The transmit differential lines are implemented with a digital slope controlled current driver that meets Twisted Pair Physical Media Device (TP-PMD) specifications. Current is sunk from the isolation transformer by the transmit differential pins. The conceptual transmit differential waveform for 100 Mbps is illustrated in the following figure.

Figure 3. Conceptual Transmit Differential Waveform



The magnetics module external to the 82562G converts I_{TDP} and I_{TDN} to 2.0 V_{PP}, as required by the TP-PMD specification. The same magnetics used for 100BASE-TX mode can also work in 10BASE-T mode.

5.1.2 100BASE-TX Receive Blocks

The receive subsection of the 82562G accepts 100BASE-TX MLT-3 data on the receive differential pair. Due to the advanced digital signal processing design techniques employed, the 82562G will accurately receive valid data from Category 5 (CAT5) UTP and Type 1 STP cable of length well in excess of 100 meters.

5.1.2.1 Adaptive Equalizer

The distorted MLT-3 signal at the end of the wire is restored by the equalizer. The equalizer performs adaptation based on the shape of the received signal, equalizing the signal to meet superior data dependent jitter performance.

5.1.2.2 Receive Clock and Data Recovery

The clock recovery circuit uses advanced digital signal processing technology to compensate for various signal jitter causes. The circuit recovers the 125 MHz clock and data and presents the data to the MLT-3 decoder.

5.1.2.3 MLT-3 Decoder, Descrambler, and Receive Digital Section

The 82562G first decodes the MLT-3 data, and then the descrambler reproduces the 5B symbols originated in the transmitter. The descrambling is based on synchronization to the transmission of the 11-bit Linear Feedback Shift Register (LFSR) during an idle phase. The data is decoded at the 4B/5B decoder. After the 4B symbols are obtained, the 82562G outputs the receive data to the CSMA unit.

In 100BASE-TX mode, the 82562G can detect errors in receive data in a number of ways. Any of the following conditions is considered an error:

- Link integrity fails in the middle of frame reception.
- The start of stream delimiter “JK” symbol is not fully detected after idle.
- An invalid symbol is detected at the 4B/5B decoder.
- Idle is detected in the middle of a frame (before “TR” is detected).

5.2 10BASE-T Mode

5.2.1 10BASE-T Transmit Blocks

5.2.1.1 10BASE-T Manchester Encoder

After the 2.5 MHz clocked data is serialized in a 10 Mbps serial stream, the 20 MHz clock performs the Manchester encoding. The Manchester code always has a mid-bit transition. The boundary transition occurs only when the data is the same from bit to bit. For example, if the value is 11b, then the change is from low to high within the boundary.

5.2.1.2 10BASE-T Driver and Filter

Since 10BASE-T and 100BASE-TX have different filtration needs, both filters are implemented inside the chip. The 82562G supports both technologies through one pair of transmit differential pins and by externally sharing the same magnetics.

In 10 Mbps mode the line drivers use a pre-distortion algorithm to improve jitter tolerance. The line drivers reduce their drive level during the second half of “wide” (100 ns) Manchester pulses and maintain a full drive level during all narrow (50 ns) pulses and the first half of the wide pulses. This reduces line overcharging during wide pulses, a major source of jitter.

5.2.2 10BASE-T Receive Blocks

5.2.2.1 10BASE-T Manchester Decoder

The 82562G performs Manchester decoding and timing recovery in 10BASE-T mode. The Manchester encoded data stream is decoded from the receive differential pair. This data is transferred to the controller at 2.5 MHz/nibble. The high-performance circuitry of the 82562G exceeds the IEEE 802.3 jitter requirements.

5.2.2.2 10BASE-T Twisted Pair Ethernet (TPE) Receive Buffer and Filter

In 10 Mbps mode, data is expected to be received on the receive differential pair after passing through isolation transformers. The filter is implemented inside the 82562G for supporting single magnetics that are shared with the 100BASE-TX side. The input differential voltage range for the Twisted Pair Ethernet (TPE) receiver is greater than 585 mV and less than 3.1 V. The TPE receive buffer distinguishes valid receive data, link test pulses, and the idle condition, according to the requirements of the 10BASE-T standard.

The following line activity is determined to be inactive and is rejected as invalid data:

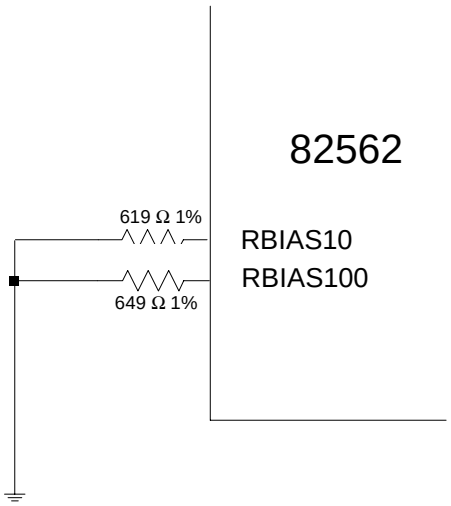
- Differential pulses of peak magnitude less than 300 mV.
- Continuous sinusoids with a differential amplitude less than 6.2 V_{PP} and frequency less than 2 MHz.
- Sine waves of a single cycle duration starting with 0° or 180° phase that have a differential amplitude less than 6.2 V_{PP} and a frequency of at least 2 MHz and not more than 16 MHz. These single-cycle sine waves are discarded only if they are preceded by 4 bit times (400 ns) of silence.

All other activity is determined to be either data, link test pulses, Auto-Negotiation fast link pulses, or the idle condition.

5.3 Analog References

The 82562G has two inputs, RBIAS100 and RBIAS10, that require external resistor connections to set biases for its internal analog section. The input pins are sensitive to the resistor value and experimentation is required to determine the correct values for any given layout. Note that the values listed in Figure 4 are starting values. Also, resistors of 1% tolerance should be used.

Figure 4. Analog References



5.4 Dynamic Reduced Power & Auto Plugging Detection

The 82562G can be configured to support a dynamic reduced power mode. This mode reduces power consumption of the 82562G when LAN activity is not present. The reduced power mode decreases power consumption from 300 mW to about 50 mW and is based on automatic detection of cable plugging. If the 82562G is configured to support dynamic power reduction, it enters the reduced power mode whenever a cable is not connected to the device. In reduced power mode, the 82562G shuts off the link circuits, except the circuit used for the automatic plugging detection. On the LAN Connect side, the entire interface remains active, including full access to all Media Independent Interface (MII) registers. In this mode, the 82562G switches to the 10 Mbps speed interface (5 MHz for LAN Connect). Thus, the reduced power mode is fully transparent to driver.

5.4.1 Auto Plugging Detection

The 82562G senses the link all the time. If it detects loss of any link activity for more than 6.6 seconds, it indicates to the Media Access Controller (MAC) an “unplugged state” by resetting the SQL LAN Connect control bit. If the 82562G is in reduced power mode and link activity is detected, the 82562G notifies the MAC (in less than 1 second) that it is in a “plugged state” by setting the SQL LAN Connect control bit. Link activity detection is based on energy detection.

5.4.2 Dynamic Reduced Power

The 82562G can be configured to support dynamic reduced power. In the dynamic reduced power mode, the 82562G transitions to reduced power mode when an unplugged state is detected. The 82562G will only return to full power if the reduced power bit on the LAN Connect is reset and a plugged state is detected. However, if the 82562G is not configured to support dynamic reduced power, the 82562G operates according to the LAN Connect power-down bit (in other words, the 82562G operates in reduced power mode only if the LAN Connect power-down bit is set).

5.4.3 Configuration

The dynamic reduced power mode is configured through bit 13 of register 16. The default value is disabled (0). The status of the 82562G can be read through bits 10:9 of register 16. When the 82562G is in reduced power mode, these two bits are set to 1b.

Table 5. Register 16 (10 Hexadecimal): PLC Status, Control and Address Data

Bit	Name	Description	Read/Write
13	Dynamic Reduced Power Down	0 = Automatic reduced power down enabled 1 = Automatic reduced power down disabled (default)	Read/Write
10	100BASE-TX Power Down	The 100BASE-TX Power Down bit indicates the power state. 0 = Normal operation (default) 1 = Power down	Read Only
9	10BASE-T Power Down	The 10BASE-T Power Down bit indicates the power state. 0 = Normal operation (default) 1 = Power down	Read Only

The 82562G PLC can enter a reduced power state manually through bit 11 of register 0. This bit is ORed with the LAN Connect power down bit, which allows the 82562G to enter a reduced power state.

Table 6. Register 0: Control Data

Bit	Name	Description	Read/Write
11	Reduced Power Down	0 = Reduced power down disabled (normal operation; default) 1 = Reduced power down enabled	Read/Write

6.0 Platform LAN Connect Registers

The following subsections describe PHY registers that are accessible through the LAN Connect management frame protocol.

Acronyms mentioned in the registers are defined as follows:

- SC: Self cleared.
- RO: Read only.
- RW: Read/Write.
- E: EEPROM setting affects content.
- LL: Latch low.
- LH: Latch high.

6.1 Medium Dependent Interface (MDI) Registers 0 through 7

6.1.1 Register 0: Control Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15	Reset	This bit sets the status and control register of the PHY to their default states and is self-clearing. The PHY returns a value of one until the reset process has completed and accepts a read or write transaction. 0 = Normal operation 1 = PHY Reset	0	RW SC
14	Loopback	This bit enables loopback of transmit data nibbles to the receive data path. The PHY receive circuitry is isolated from the network. Note that this may cause the descrambler to lose synchronization and produce 560 ns of “dead time.” Note also that the loopback configuration bit takes priority over the Loopback MDI bit. 0 = Loopback disabled (normal operation) 1 = 1 = Loopback enabled	0	RW
13	Speed Selection	This bit is valid on read and controls speed when Auto-Negotiation is disabled. 0 = 10 Mbps 1 = 100 Mbps	1	RW
12	Auto-Negotiation Enable	This bit enables Auto-Negotiation. Bits 13 and 8, Speed Selection and Duplex Mode, respectively, are ignored when Auto-Negotiation is enabled. 0 = Auto-Negotiation disabled 1 = Auto-Negotiation enabled	1	RW
11	Reduced Power Down	This bit sets the PHY into a low power mode. 0 = Power down disabled (normal operation) 1 = Power down enabled	0	RW

Bit(s)	Name	Description	Default	R/W
10	Isolate	This bit allows the PHY to isolate the medium independent interface. The PHY is disconnected from the LAN Connect block on both the transmit and receive side. 0 = Normal operation 1 = Isolates internal medium independent interface	0	RW
9	Restart Auto-Negotiation	This bit restarts the Auto-Negotiation process and is self-clearing. 0 = Normal operation 1 = Restart Auto-Negotiation process	0	RW SC
8	Duplex Mode	This bit controls the duplex mode when Auto-Negotiation is disabled. When Auto-Negotiation is enabled this bit is read only and always equals 1b. When the PHY is placed in Loopback mode, the behavior of the PHY shall not be affected by the status of this bit. 0 = Half Duplex 1 = Full Duplex	0	RW/ RO
7	Collision Test	This bit is not used in the 82562G and has a default value of 1b. (If it is used in other devices, it forces a collision in response to the assertion of the transmit enable signal.)	1	RW
6:0	Reserved	These bits are reserved and should be set to 0b.	0	RW

6.1.2 Register 1: Status Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15	Reserved	This bit is reserved and should be set to 0b.	0	RO
14	100BASE-TX Full-duplex	This bit enables 100BASE-TX full-duplex operation and is dependent on ADV10. If ADV10 is active, the default value is 0. 0 = PHY unable to perform full-duplex 100BASE-TX 1 = PHY able to perform full-duplex 100BASE-TX	1	RO
13	100 Mbps Half-duplex	This bit enables 100BASE-TX half-duplex operation and is dependent on ADV10. If ADV10 is active, the default value is 0. 0 = PHY unable to perform half-duplex 100BASE-TX 1 = PHY able to perform half-duplex 100BASE-TX	1	RO
12	10 Mbps Full-duplex	This bit enables 10BASE-T full duplex operation. 0 = PHY unable to perform full-duplex 10BASE-T 1 = PHY able to perform full-duplex 10BASE-T	1	RO
11	10 Mbps Half-duplex	This bit enables 10BASE-T half-duplex operation. 0 = PHY unable to perform half-duplex 10BASE-T 1 = PHY able to perform half-duplex 10BASE-T	1	RO
10:7	Reserved	These bits are reserved and should be set to 0b.	0	RO
6	Management Frames Preamble Suppression	This bit allows the 82562G to receive management frames with suppressed preamble. 0 = PHY will not accept management frames with preamble suppressed 1 = PHY will accept management frames with preamble suppressed	0	RO

Bit(s)	Name	Description	Default	R/W
5	Auto-Negotiation Complete	This bit reflects status of the Auto-Negotiation process. 0 = Auto-Negotiation process has not completed 1 = Auto-Negotiation process completed	0	RO
4	Remote Fault	0 = No remote fault condition detected 1 = Remote fault condition detected	0	RO
3	Auto-Negotiation Ability	This bit reflects the PHY's Auto-Negotiation ability status. 0 = PHY is unable to perform Auto-Negotiation 1 = PHY is able to perform Auto-Negotiation	1	RO
2	Link Status	This bit reflects link status. 0 = Invalid link detected 1 = Valid link established	0	RO LL
1	Jabber Detect	This bit is used only in 10BASE-T mode. 0 = No jabber condition detected 1 = Jabber condition detected	0	RO LH
0	Extended Capability	This bit enables the extended register capabilities. 0 = Extended register capabilities disabled 1 = Extended register capabilities enabled	1	RO

6.1.3 Register 2: PHY Identifier Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	PHY ID (high byte)	Value: 02A8 hexadecimal	--	RO

6.1.4 Register 3: PHY Identifier Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	PHY ID (low byte)	Value: 0330 hexadecimal for 82562G PLC (and 82562GZ)	--	RO
15:0	PHY ID (low byte)	Value: 0310 hexadecimal for 82562G	--	RO

6.1.5 Register 4: Auto-Negotiation Advertisement Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15	Next Page	This bit is a constant 0, transmit primary capability data page.	0	RO
14	Reserved	This bit is reserved and should be set to 0b.	0	RO

Bit(s)	Name	Description	Default	R/W
13	Remote Fault	0 = No remote fault 1 = Indicate link partner's remote fault	0	RW
12:5	Technology Ability Field	Technology Ability Field is an 8-bit field containing information indicating supported technologies specific to the selector field value.	00101111	RW
4:0	Selector Field	The Selector Field is a 5-bit field identifying the type of message to be sent by Auto-Negotiation. This field is read only and contains a value of 00001b, IEEE Standard 802.3.	00001	RO

6.1.6 Register 5: Auto-Negotiation Link Partner Ability Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15	Next Page	This bit reflects the PHY's link partner's Next Page ability.	--	RO
14	Acknowledge	This bit is used to indicate that the 82562G has successfully received its link partner's Auto-Negotiation advertising ability.	--	RO
13	Remote Fault	This bit reflects the PHY's link partner's Remote Fault condition.	--	RO
12:5	Technology Ability Field	This bit reflects the PHY's link partner's Technology Ability Field.	--	RO
4:0	Selector Field	This bit reflects the PHY's link partner's Selector Field.	--	RO

6.1.7 Register 6: Auto-Negotiation Expansion Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:5	Reserved	These bits are reserved and should be set to 0.	0	RO
4	Parallel Detection Fault	This bit clears itself on read. 0 = No fault detected via parallel detection 1 = Fault detected via parallel detection (multiple link fault occurred)	0	RO SC LH
3	Link Partner Next Page Able	0 = Link Partner is not Next Page able 1 = Link Partner is Next Page able	0	RO
2	Next Page Able	0 = 0 = Local drive is not Next Page able 1 = Local drive is Next Page able	0	RO
1	Page Received	This bit clears itself on read. 0 = New Page not received 1 = New Page received	0	RO SC LH
0	Link Partner Auto-Negotiation Able	0 = Link Partner is not Auto-Negotiation able 1 = Link Partner is Auto-Negotiation able	0	RO

6.2 MDI Registers 8 through 15

Registers 8 through 15 are reserved for IEEE.

6.3 MDI Registers 16 through 31

6.3.1 Register 16: PHY Status and Control Register Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:14	Reserved	These bits are reserved and should be set to 00b.	00	RW
13	Reduced Power Down Disable	This bit disables the automatic reduced power down. 0 = Enable automatic reduced power down 1 = Disable automatic reduced power down	1	RW
12	Reserved	This bit is reserved and should be set to 0b.	0	RW
11	Receive De-Serializer In-Sync Indication	This bit indicates status of the 100BASE-TX Receive De-Serializer In-Sync.	--	RO
10	100BASE-TX Power-Down	This bit indicates the power state of 100BASE-TX PHY unit. 0 = Normal operation 1 = Power-down	1	RO
9	10BASE-T Power-Down	This bit indicates the power state of 10BASE-T PHY unit. 0 = Normal operation 1 = Power-Down	1	RO
8	Polarity	This bit indicates 10BASE-T polarity. 0 = Normal polarity 1 = Reverse polarity	--	RO
7	Reserved	This bit is reserved and should be set to 0b.	0	RO
6:2	PHY Address	These bits contain the sampled PHY address.	--	RO
1	Speed	This bit indicates the Auto-Negotiation result. 0 = 10 Mbps 1 = 100 Mbps	--	RO
0	Duplex Mode	This bit indicates the Auto-Negotiation result. 0 = Half-duplex 1 = Full-duplex	--	RO

6.3.2 Register 17: PHY Unit Special Control Bit Definitions

Bit(s)	Name	Description	Default	R/W
15	Scrambler By-pass	0 = Normal operations 1 = By-pass scrambler	0	RW
14	By-pass 4B/5B	0 = Normal operation 1 = 4 bit to 5 bit by-pass	0	RW
13	Force Transmit H-Pattern	0 = Normal operation 1 = Force transmit H-pattern	0	RW
12	Force 34 Transmit Pattern	0 = Normal operation 1 = Force 34 transmit pattern	0	RW
11	Valid Link	0 = Normal operation 1 = 100BASE-TX valid link	0	RW
10	Symbol Error Enable	0 = Normal operation 1 = Symbol error output is enabled	0	RW
9	Carrier Sense Disable	This bit controls the receive 100 carrier sense disable function. 0 = Carrier sense enabled 1 = Carrier sense disabled	0	RW
8	Disable Dynamic Power-Down	0 = Dynamic Power-Down enabled 1 = Dynamic Power-Down disabled	0	RW
7	Auto-Negotiation Loopback	0 = Auto-Negotiation normal mode 1 = Auto-Negotiation loopback	0	RW
6	MDI Tri-State	0 = Normal operation 1 = MDI Tri-state (transmit driver tri-states)	0	RW
5	Force Polarity	0 = Normal polarity 1 = Reversed polarity	0	RW
4	Auto Polarity Disable	0 = Normal polarity operation 1 = Auto Polarity disabled	0	RW
3	Squelch Disable	0 = Normal squelch operation 1 = 10BASE-T squelch test disable	0	RW
2	Extended Squelch	1 = 10BASE-T Extended Squelch control enabled 0 = 10BASE-T Extended Squelch control disabled	0	RW
1	Link Integrity Disable	0 = Normal Link Integrity operation 1 = Link disabled	0	RW
0	Jabber Function Disable	0 = Normal Jabber operation 1 = Jabber disabled	0	RW

6.3.3 Register 18: Reserved

Bit(s)	Name	Description	Default	R/W
15:0	Reserved	These bits are reserved and should be set to a constant 0.	0	RO

6.3.4 Register 19: 100BASE-TX Receive False Carrier Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Receive False Carrier	These bits are used for the false carrier counter.	--	RO SC

6.3.5 Register 20: 100BASE-TX Receive Disconnect Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Disconnect Event	This field contains a 16-bit counter that increments for each disconnect event. The counter stops when it is full and self-clears on read	--	RO SC

6.3.6 Register 21: 100BASE-TX Receive Error Frame Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Receive Error Frame	This field contains a 16-bit counter that increments once per frame for any receive error condition (such as a symbol error or premature end of frame) in that frame. The counter stops when it is full and self-clears on read.	--	RO SC

6.3.7 Register 22: Receive Symbol Error Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Symbol Error Counter	This field contains a 16-bit counter that increments for each symbol error. The counter stops when it is full and self-clears on read. In a frame with a bad symbol, each sequential six bad symbols count as one.	--	RO SC

6.3.8 Register 23: 100BASE-TX Receive Premature End of Frame Error Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Premature End of Frame	This field contains a 16-bit counter that increments for each premature end of frame event. The counter stops when it is full and self-clears on read.	--	RO SC

6.3.9 Register 24: 10BASE-T Receive End of Frame Error Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	End of Frame Counter	This is a 16-bit counter that increments for each end of frame event. The counter stops when it is full and self-clears on read.	--	RO SC

6.3.10 Register 25: 10BASE-T Transmit Jabber Detect Counter Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:0	Jabber Detect Counter	This is a 16-bit counter that increments for each jabber detection event. The counter stops when it is full and self-clears on read.	--	RO SC

6.3.11 Register 27: PHY Unit Special Control Bit Definitions

Bit(s)	Name	Description	Default	R/W
15:6	Reserved	These bits are reserved and should be set to a constant 0.	0	RO
5	Switch Probe Mapping	This bit switches the mapping on the LEDs. The LED mapping is described below in bits 2:0, LED Switch Control. This bit should always be set to 0b.	0	RW
4	New mode	If this bit equals 0, the device is in 82562EZ (or 82562ET) mode. If this bit equals 1, the device is in 82562G mode.		RO
3	100BASE-TX Receive Jabber Disable	This bit enables the carrier sense disconnection while the PHY is in jabber mode at 100 Mbps speed.	0	RW
2:0	LED Switch Control	Value / ACTLED# / LILED# 000 / Activity / Link 001 / Speed / Collision 010 / Speed / Link 011 / Activity / Collision 100 / Off / Off 101 / Off / On 110 / On / Off 111 / On / On	000	RW

Note: This page intentionally left blank.

7.0 82562G Test Port Functionality

The 82562G's XOR Tree Test Access Port (TAP) is the access point for test data to and from the device. The port provides the ability to perform basic production level testing.

7.1 Asynchronous Test Mode

An asynchronous test mode is supported for system level design use. The modes are selected through the use of the Test Port input pins (TESTEN, ISOL_TCK, ISOL_TI and ISOL_EXEC) in static combinations. During normal operation the test pins must be pulled down through a resistor (pulling Test high enables the test mode). All other port inputs may have a pull-down at the designers discretion.

7.2 Test Function Description

The 82562G TAP mode supports several tests that can be used in board level design. These tests can help verify basic functionality and test the integrity of solder connections on the board. The tests are described in the following sections.

The XOR Tree test mode is the most useful of the asynchronous test modes. It enables the placement of the 82562G to be validated at board test. The XOR Tree was chosen for its speed advantages. Modern Automated Test Equipment (ATE) can perform a complete peripheral scan without support at the board level. This command connects all output signals of the input buffers in the device periphery into an XOR Tree scheme. All output drivers of the output-buffers, except the test output (TOUT) pin, are put into high-Z mode. These pins are driven to affect the tree's output. Any hard strapped pins will prevent the tester from scanning correctly. The XOR Tree test mode is obtained by placing the test pins in the following configuration (refer to Table 7):

TESTEN = 1

ISOL_TCK = 0

ISOL_TI = 0

ISOL_EXEC = 0.

Table 7. XOR Tree Chain Order

Chain Order	Chain
1	JTXD2
2	JTXD1
3	JTXD0
4	JRSTSYNC
5	ADV10 (LAN_DISABLE#)
6	JCLK
7	JRXD2
8	JRXD1
9	JRXD0
10	ACTLED#

Table 7. XOR Tree Chain Order

Chain Order	Chain
11	SPDLED#
12	LILED#
XOR Tree Output	TOUT

The following pins are not included in the XOR Tree chain: X1, ISOL_TCK, ISOL_EXEC, ISOL_TI and TESTEN.

8.0 Electrical and Timing Specifications

8.1 Absolute Maximum Ratings

Maximum ratings are listed below:

Case Temperature under Stress . . . . . 0° C to 135° C
Storage Temperature . . . . . -65° C to 150° C
Supply Voltage with respect to V_{SS} . . . . . -0.5 V to 3.45 V
Output Voltages . . . . . -0.50 V to 3.45 V
Input Voltages . . . . . V_{CC} to 3.45 V

Stresses above the listed absolute maximum ratings may cause permanent damage to the 82562G device. This is a stress rating only and functional operations of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.2 DC Characteristics

Table 8. General DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{CC}	Supply Voltage		3.0	3.3	3.45	V	
T	Temperature	Minimum/Maximum Case Temperature	0		85	C	
P	Power Consumption	10/100Mbps (transmitter on)		300		mW	
		Reduced Power		50		mW	
		Auto-Negotiation		200		mW	

8.2.1 X1 Clock DC Specifications

Table 9. X1 Clock DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{IL}	Input Low Voltage				0.8	V	
V_{IH}	Input High Voltage		2.0			V	
I_{ILIH}	Input Leakage Currents	$0 < V_{IN} < V_{CC}$			±10	µA	
C_I	Input Capacitance				8	pF	1

NOTES:
1. This characteristic is only characterized, not tested. It is valid for digital pins only.

8.2.2 LAN Connect Interface DC Specifications

Table 10. LAN Connect Interface DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{CCJ}	Input/Output Supply Voltage		3.0		3.45	V	
V_{IL}	Input Low Voltage		-0.5		$0.3V_{CCJ}$	V	
V_{IH}	Input High Voltage		$0.6V_{CCJ}$		V_{CCJ} + 0.5	V	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{CCJ}$			±10	µA	
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA			$0.1V_{CCJ}$	V	
V_{OH}	Output High Voltage	I_{OUT} = -500 µA	$0.9V_{CCJ}$			V	
C_{IN}	Input Pin Capacitance				8	pF	1

NOTES:
1. This characteristic is only characterized, not tested. It is valid for digital pins only.

8.2.3 LED DC Specifications

Table 11. LED DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OLLED}	Output Low Voltage	I_{OUT} = 10 mA			0.7	V	
V_{OHLED}	Output High Voltage	I_{OUT} = -10 mA	2.4			V	

8.2.4 10BASE-T Voltage and Current DC Specifications

Table 12. 10BASE-T Transmitter

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OD10}	Output Differential Peak Voltage	R_L = 100 Ω	2.2		2.8	V	1

NOTES: Current is measured between the transmit differential pins (TDP and TDN) at 3.3 V.
1. R_L is the resistive load measured across the transmit differential pins, TDP and TDN.

Table 13. 10BASE-T Receiver

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
R_{ID10}	Input Differential Resistance	DC	10			KΩ	1
V_{IDA10}	Input Differential Accept Peak Voltage	5 MHz ≤ f ≤ 10 MHz	585		3100	mV	
V_{IDR10}	Input Differential Reject Peak Voltage	5 MHz ≤ f ≤ 10 MHz			300	mV	
V_{ICM10}	Input Common Mode Voltage			$V_{CC/2}$		V	

NOTES:
1. The input differential resistance is measured across the receive differential pins, RDP and RDN.

8.2.5 100BASE-TX Voltage and Current DC Specifications

Table 14. 100BASE-TX Transmitter

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OD100}	Output Differential Peak Voltage	R_L = 100 Ω	0.95	1.0	1.05	V	1

NOTES: Current is measured between the transmit differential pins (TDP and TDN) at 3.3 V.
1. R_L is the resistive load measured across the transmit differential pins, TDP and TDN.

Table 15. 100BASE-TX Receiver

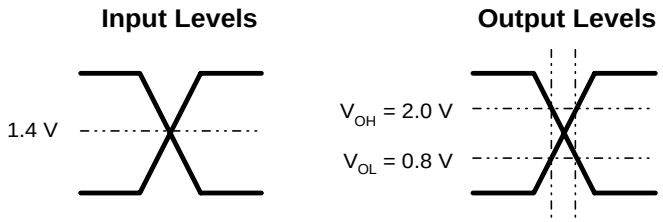
Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
R_{ID100}	Input Differential Resistance	DC	10			KΩ	1
V_{IDA100}	Input Differential Accept Peak Voltage		500		1200	mV	
V_{IDR100}	Input Differential Reject Peak Voltage				100	mV	
V_{ICM100}	Input Common Mode Voltage			$V_{CC/2}$		V	

NOTES:
1. The input differential resistance is measured across the receive differential pins, RDP and RDN.

8.3 AC Characteristics

Figure 5 defines the conditions for timing measurements. The design must guarantee proper operation for voltage swings and slew rates that exceed the specified test conditions.

Figure 5. AC Test Level Conditions

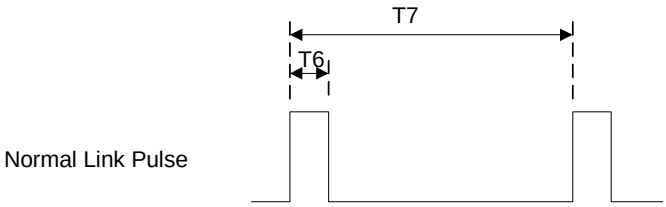


8.3.1 10BASE-T Normal Link Pulse (NLP) Timing Parameters

Table 16. Normal Link Pulse Timing Parameters

	Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
T6	T_{NLP_WID}	NLP Width	10 Mbps		100		ns	
T7	T_{NLP_PER}	NLP Period	10 Mbps	8	16	24	ms	

Figure 6. Normal Link Pulse Timings

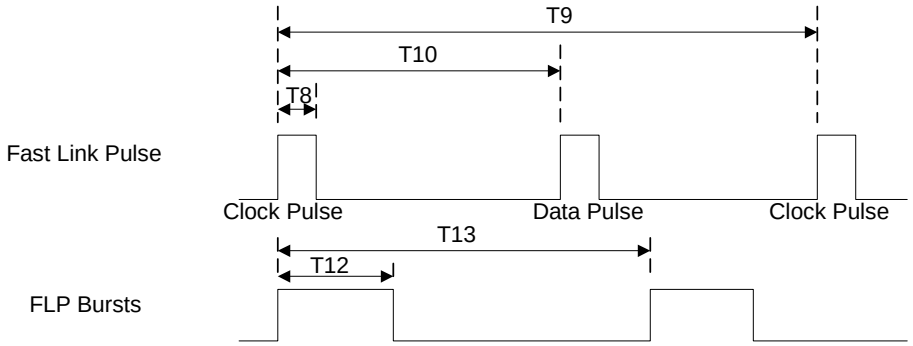


8.3.2 Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

Table 17. Fast Link Pulse Timing Parameters

	Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
T8	T_{FLP_WID}	FLP Width (clock and data)			100		ns	
T9	$T_{FLP_CLK_CLK}$	Clock Pulse to Clock Pulse Period		111	125	139	µs	
T10	$T_{FLP_CLK_DATA}$	Clock Pulse to Data Pulse Period		55.5	62.5	69.5	µs	
T11	$T_{FLP_BUR_NUM}$	Pulses in One Burst		17		33	#	
T12	$T_{FLP_BUR_WID}$	Burst Width			2		ms	
T13	$T_{FLP_BUR_PER}$	FLP Burst Period		8	16	24	ms	

Figure 7. Fast Link Pulse Timings



8.3.3 100BASE-TX Transmitter AC Specifications

Table 18. 100BASE-TX Transmitter Timing Parameters

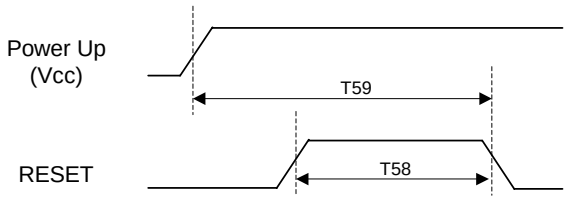
	Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
T14	T_{JIT}	TDP/TDN Differential Output Peak Jitter	HLS Data			1400	ps	

8.3.4 Reset (RSTSYNC) AC Specifications

Table 19. Reset Timing Parameters

	Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
T58	T_{RST_WID}	Reset Pulse Width		500			µs	
T59	T_{POP_RST}	Power-up to Falling Edge of Reset		1000			µs	

Figure 8. Reset Timing Parameters

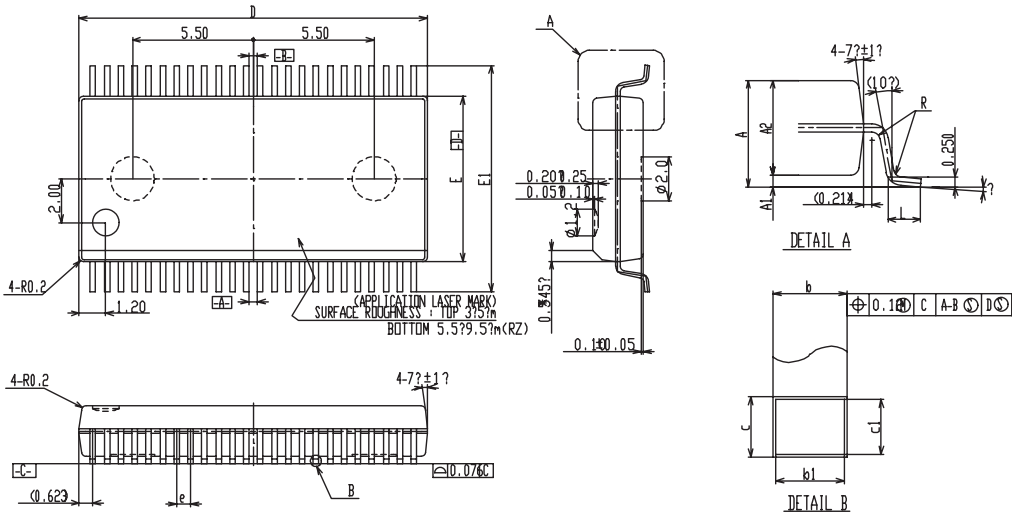


9.0 Package and Pinout Information

9.1 Package Information

The 82562G is a lead-free 48-pin Shrink Small Outline Package (SSOP) that supports leaded and lead-free designs. The Package dimensions are shown in Figure 9. More information on Intel device packaging is available in the Intel Packaging Handbook, which is available from the Intel Literature Center or your local sales office.

Figure 9. Dimension Diagram for the 82562G PLC 48-pin SSOP



SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	2.44	2.59	2.74
A1	0.20	0.30	0.40
A2	2.24	2.29	2.34
b	0.22	—	0.30
b1	0.22	0.25	0.28
c	0.18	—	0.25
c1	0.18	0.20	0.22
D	15.75	15.85	15.95
E	7.45	7.50	7.55
E1	10.16	10.285	10.41
L	0.70	0.80	0.90
e	0.635 BSC		
R	0.10	0.20	0.30
?	0?	5?	8?

NOTES)
1. ALL DIMENSIONS ARE IN MILLIMETERS.(ANGLES IN DEGREES)
2. DIMENSIONS "D"DOES NOT INCLUDE BURRS.
   HOWEVER, DIMENSION INCLUDING PROTRUSIONS OR GATE BURRS
   SHALL BE MAX. 0.20mm.
3. DIMENSION "E1"DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
   INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

9.2 Pinout Information

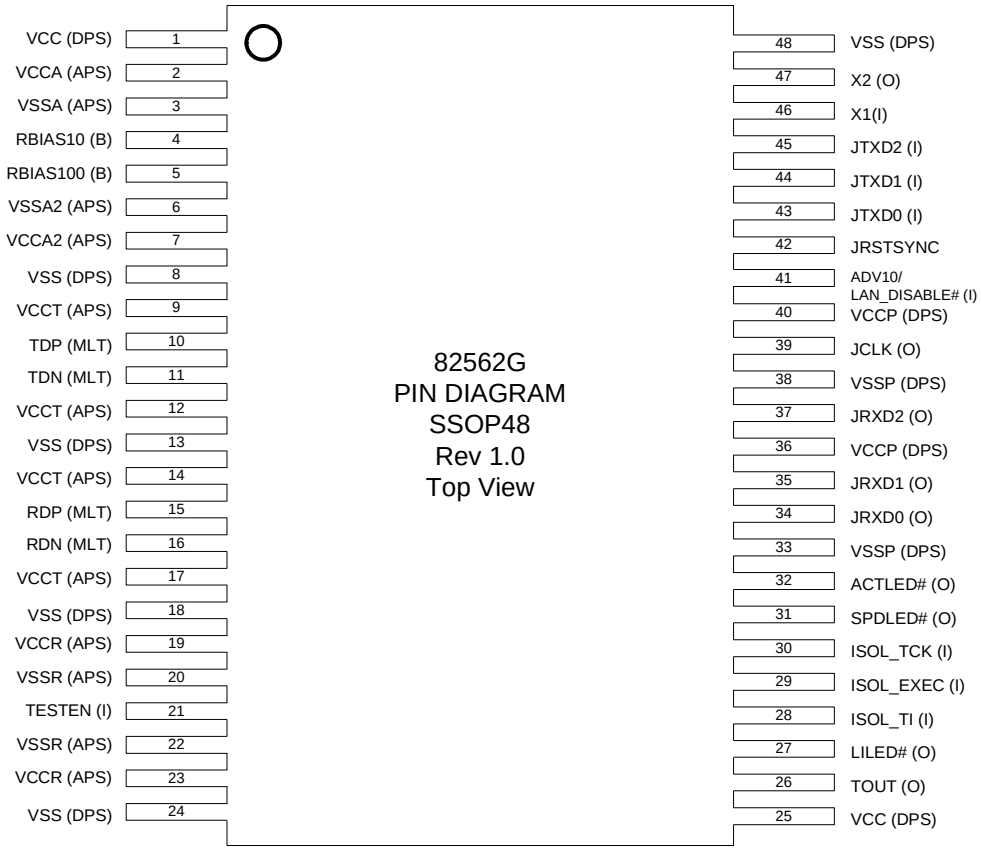
9.2.1 82562G Pin Assignments

Table 20. 82562G Pin Assignments

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	VCC	13	VSS	25	VCC	37	JRXD2
2	VCCA	14	VCCT	26	TOUT	38	VSSP
3	VSSA	15	RDP	27	LILED#	39	JCLK
4	RBIAS10	16	RDN	28	ISOL_TI	40	VCCP
5	RBIAS100	17	VCCT	29	ISOL_EXEC	41	ADV10/LAN_ DISABLE#
6	VSSA2	18	VSS	30	ISOL_TCK	42	JRSTSYNC
7	VCCA2	19	VCCR	31	SPDLED#	43	JTXD0
8	VSS	20	VSSR	32	ACTLED#	44	JTXD1
9	VCCT	21	TESTEN	33	VSSP	45	JTXD2
10	TDP	22	VSSR	34	JRXD0	46	X1
11	TDN	23	VCCR	35	JRXD1	47	X2
12	VCCT	24	VSS	36	VCCP	48	VSS

9.2.2 82562G Shrink Small Outline Package Diagram

Figure 10. 82562G Pin Out Diagram



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