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82527
SERIAL COMMUNICATIONS CONTROLLER CONTROLLER AREA NETWORK PROTOCOL

Automotive

- **Supports CAN Specification 2.0**
  - **— Standard Data and Remote Frames**
  - **— Extended Data and Remote Frames**
- **Programmable Global Mask**
  - **— Standard Message Identifier**
  - **— Extended Message Identifier**
- **15 Message Objects of 8-Byte Data Length**
  - **— 14 Tx/Rx Buffers**
  - **— 1 Rx Buffer with Programmable Mask**
- **Flexible CPU Interface**
  - **— 8-Bit Multiplexed**
  - **— 16-Bit Multiplexed**
  - **— 8-Bit Non-Multiplexed (Synchronous/Asynchronous)**
  - **— Serial Interface**
- **Programmable Bit Rate**
- **Programmable Clock Output**
- **Flexible Interrupt Structure**
- **Flexible Status Interface**
- **Configurable Output Driver**
- **Configurable Input Comparator**
- **Two 8-Bit Bidirectional I/O Ports**
- **44-Lead PLCC Package**
- **44-Lead QFP Package**
- **Pinout Compatibility with the 82526**

The 82527 serial communications controller is a highly integrated device that performs serial communication according to the CAN protocol. It performs all serial communication functions such as transmission and reception of messages, message filtering, transmit search, and interrupt search with minimal interaction from the host microcontroller, or CPU.

The 82527 is Intel's first device to support the standard and extended message frames in CAN Specification 2.0 Part B. It has the capability to transmit, receive, and perform message filtering on extended message frames. Due to the backwardly compatible nature of CAN Specification 2.0, the 82527 also fully supports the standard message frames in CAN Specification 2.0 Part A.

The 82527 features a powerful CPU interface that offers flexibility to directly interface to many different CPUs. It can be configured to interface with CPUs using an 8-bit multiplexed, 16-bit multiplexed, or 8-bit non-multiplexed address/data bus for Intel and non-Intel architectures. A flexible serial interface (SPI) is also available when a parallel CPU interface is not required.

The 82527 provides storage for 15 message objects of 8-byte data length. Each message object can be configured as either transmit or receive except for the last message object. The last message object is a receive-only buffer with a special mask design to allow select groups of different message identifiers to be received.

The 82527 also implements a global masking feature for message filtering. This feature allows the user to globally mask any identifier bits of the incoming message. The programmable global mask can be used for both standard and extended messages.

The 82527 PLCC offers hardware, or pinout, compatibility with the 82526. It is pin-to-pin compatible with the 82526 except for pins 9, 30, and 44. These pins are used as chip selects on the 82526 and are used as CPU interface mode selection pins on the 82527.

The 82527 is fabricated using Intel's reliable CHMOS III 5V technology and is available in either 44-lead PLCC or 44-lead QFP for the automotive temperature range (−40°C to +125°C).

For complete Rochester ordering guide, please refer to page 2
Please contact factory for specific package availability and Military/Aerospace specifications/availability.

Rochester Electronics guarantees performance of its semiconductor products to the original OEM specifications. "Typical" values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing. Rochester Electronics reserves the right to make changes without further notice to any specification herein.

Rochester Ordering Guide

**Most products can also be offered as RoHS compliant, designated by a –G suffix. Please contact factory for more information.*

Rochester Part Number	Intel Part Number	Package	Temperature
AN82527	AN82527	LDCC-44, Plastic	-40° to +125°C
AS82527	AS82527	QFP-44, Plastic	-40° to +125°C

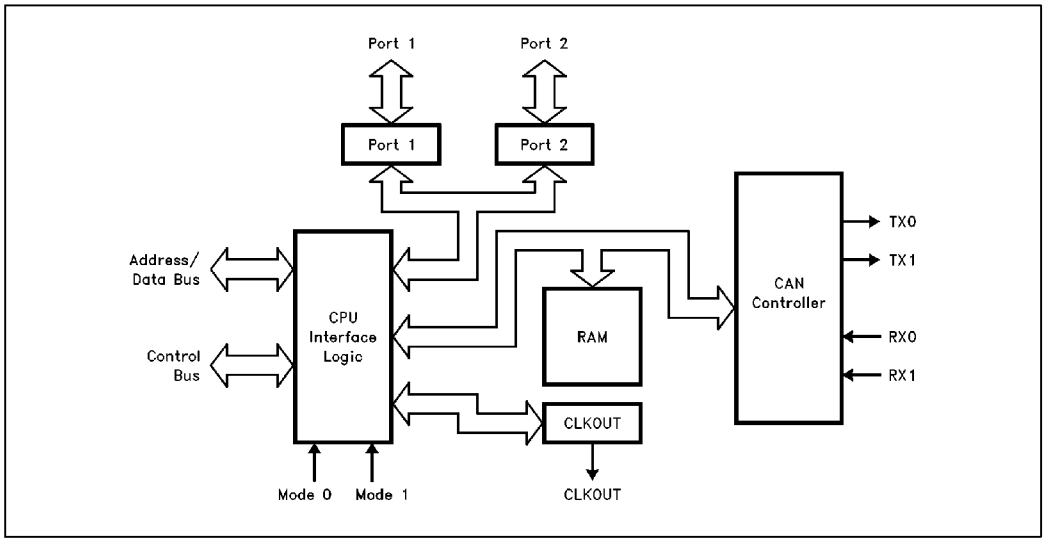


Figure 1. 82527 Block Diagram

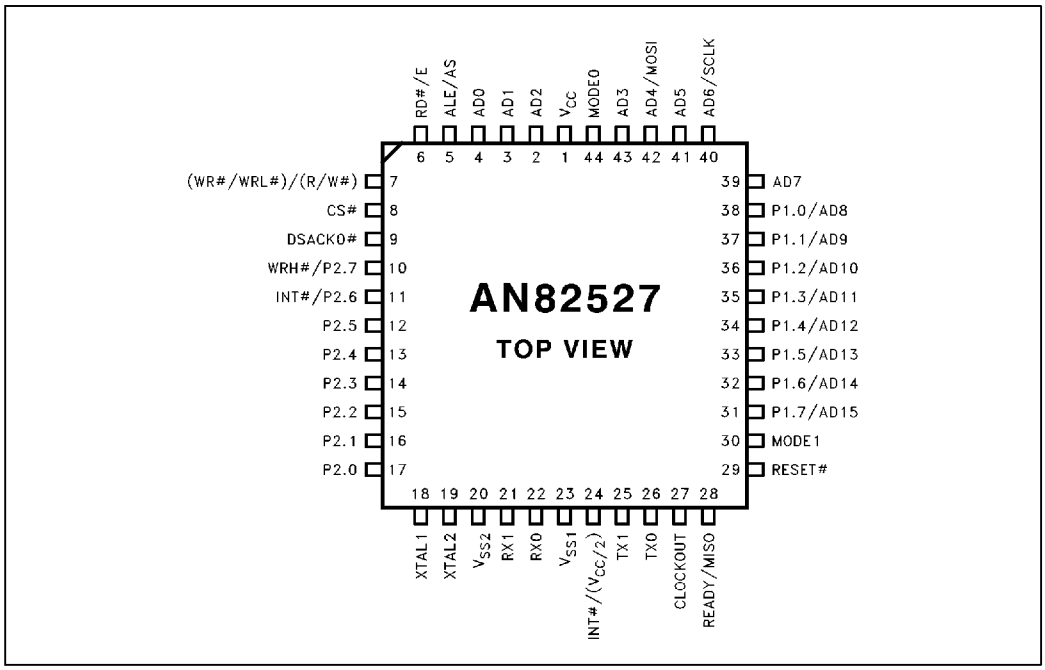


Figure 2. 44-Pin PLCC Package

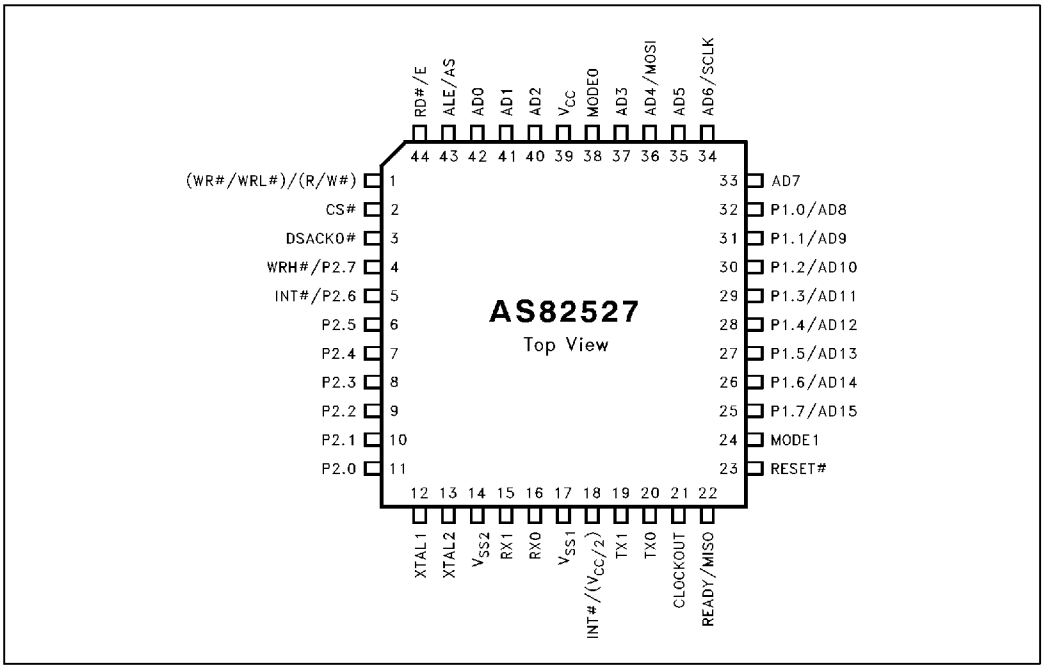


Figure 3. 44-Pin QFP Package

PIN DESCRIPTION

The 82527 pins are described in this section. Table 1 presents the legend for interpreting the pin types.

Table 1. Pin Type Legend

Symbol	Description
I	Input only pin
O	Output only pin
I/O	Pin can be either input or output

PIN DESCRIPTIONS

Pin Name	Pin Type	Pin Description
V_{SS1}	Ground	GROUND connection must be connected externally to a V_{SS} board plane. Provides digital ground.
V_{SS2}	Ground	GROUND connection must be connected externally to a V_{SS} board plane. Provides ground for analog comparator.
V_{CC}	Power	POWER connection must be connected externally to +5V DC. Provides power for entire device.
XTAL1	I	Input for an external clock. XTAL1 (along with XTAL2) are the crystal connections to an internal oscillator.
XTAL2	O	Push-pull output from the internal oscillator. XTAL2 (along with XTAL1) are the crystal connections to an internal oscillator. If an external oscillator is used XTAL2 must be floated, or not be connected. XTAL2 must not be used as a clock output to drive other CPUs.
CLKOUT	O	Programmable clock output. This output may be used to drive the oscillator of the host microcontroller.
RESET#	I	Warm Reset: (V_{CC} remains valid while RESET# is asserted), RESET# must be driven to a valid low level for 1 ms minimum. Cold Reset: (V_{CC} is driven to a valid level while RESET# is asserted), RESET# must be driven low for 1 ms minimum measured from a valid V_{CC} level. No falling edge on the reset pin is required during a cold reset event.
CS#	I	A low level on this pin enables CPU access to the 82527 device.
INT# (V_{CC}/2)	O O	The interrupt pin is an open-drain output to the host microcontroller. V_{CC}/2 is the power supply for the ISO low speed physical layer. The function of this pin is determined by the MUX bit in the CPU Interface Register (Address 02H) as follows: MUX = 1: pin 24 (PLCC) = V_{CC}/2, pin 11 = INT# MUX = 0: pin 24 (PLCC) = INT#
RX0 RX1	I I	Inputs from the CAN bus line(s) to the input comparator. A recessive level is read when RX0 > RX1. A dominant level is read when RX1 > RX0. When the CoBy bit (Bus Configuration register) is programmed as a "1", the input comparator is bypassed and RX0 is the CAN bus line input.
TX0 TX1	O O	Serial data push-pull output to the CAN bus line. During a recessive bit TX0 is high and TX1 is low. During a dominant bit TX0 is low and TX1 is high.

Pin Name	Pin Type	Pin Description
AD0/A0/ICP AD1/A1/CP AD2/A2/CSAS AD3/A3/STE AD4/A4/MOSI AD5/A5 AD6/A6/SCLK AD7/A7	I/O-I-I I/O-I-I I/O-I-I I/O-I I/O-I-I I/O-I I/O-I-I I/O-I	Address/Data bus in 8-bit multiplexed mode. Address bus in 8-bit non-multiplexed mode. Low byte of A/D bus in 16-bit multiplexed mode. In Serial Interface mode, the following pins have the following meaning: AD0: ICP Idle Clock Polarity AD1: CP Clock Phase AD2: CSAS Chip Select Active State AD3: STE Sync Transmit Enable AD6: SCLK Serial Clock Input AD4: MOSI Serial Data Input
AD8/D0/P1.0 AD9/D1/P1.1 AD10/D2/P1.2 AD11/D3/P1.3 AD12/D4/P1.4 AD13/D5/P1.5 AD14/D6/P1.6 AD15/D7/P1.7	I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O	High byte of A/D bus in 16-bit multiplexed mode. Data bus in 8-bit non-multiplexed mode. Low speed I/O port. P1 pins in 8-bit multiplexed mode and serial mode. Port pins have weak pullups until the port is configured by writing to 9FH and AFH.
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6/INT# P2.7/WRH#	I/O I/O I/O I/O I/O I/O I/O-O I/O-I	P2 in all modes. P2.6 is INT# when MUX = 1 and is open-drain. P2.7 is WRH# in 16-bit multiplexed mode.
Mode0 Mode1	I I	These pins select one of the four parallel interfaces. These pins are weakly held low during reset. **Mode1 Mode0** 0 0 8-bit multiplexed — Intel 0 0 Serial Interface mode entered when RD# = 0, WR# = 0 upon reset. 0 1 16-bit multiplexed — Intel 1 0 8-bit multiplexed — non-Intel 1 1 8-bit non-multiplexed
ALE/AS	I-I	ALE used for Intel modes. AS used for non-Intel modes, except Mode 3 this pin must be tied high.
RD# E	I I	RD# used for Intel modes. E used for non-Intel modes, except Mode 3 Asynchronous this pin must be tied high.
WR#/WRL# R/W#	I I	WR# in 8-bit Intel mode and WRL# in 16-bit Intel mode. R/W# used for non-Intel modes.
READY MISO	O O	READY is an output to synchronize accesses from the host microcontroller to the 82527. READY is an open-drain output to the host microcontroller. MISO is the serial data output for the serial interface mode.
DSACK0#	O	DSACK0# is an open-drain output to synchronize accesses from the host microcontroller to the 82527.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −60°C to +150°C

Voltage from Any Pin to V_{SS} ..... −0.5V to +7.0V

Laboratory testing shows the 82527 will withstand up to 10 mA of injected current into both RX0 and RX1 pins for a total of 20 days without sustaining permanent damage. This high current condition may be the result of shorted signal lines. The 82527 will not function properly if the RX0/RX1 input voltage exceeds V_{CC} + 0.5V.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. Characteristics V_{CC} = 5V ±10%; T_A = −40°C to +125°C

Symbol	Parameter	Min	Max	Conditions
V_{IL}	Input Low Voltage (All except RX0, RX1, AD0–AD7 in Mode 3)	−0.5V	0.8V	
V_{IL1}	Input Low Voltage for AD0–AD7 in Mode 3	−0.5V	0.5V	
V_{IL2}	Input Low Voltage (RX0) for Comparator Bypass Mode		0.5V	
V_{IL3}	Input Low Voltage for Port 1 and Port 2 Pins Not Used for Interface to Host CPU		0.3 V_{CC}	
V_{IH}	Input High Voltage (All except RX0, RX1, RESET#)	3.0V	V_{CC} + 0.5V	
V_{IH1}	Input High Voltage (RESET#) Hysteresis on RESET#	3.0V 200 mV	V_{CC} + 0.5V	
V_{IH2}	Input High Voltage (RX0) for Comparator Bypass Mode	4.0V		
V_{IH3}	Input High Voltage for Port 1 and Port 2 Pins Not Used for Interface to Host CPU	0.7 V_{CC}		
V_{OL}	Output Low Voltage (All Outputs except TX0, TX1)		0.45V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage (All Outputs except TX0, TX1, CLOCKOUT)	V_{CC} − 0.8V		I_{OH} = −200 μA
V_{OHR1}	Output High Voltage (CLOCKOUT)	0.8 V_{CC}		I_{OH} = −80 μA
I_{LK}	Input Leakage Current		±10 μA	$V_{SS} < V_{IN} < V_{CC}$
C_{IN}	PIN Capacitance**		10 pF	f_{XTAL} = 1 KHz

D.C. Characteristics V_{CC} = 5V ±10%; T_A = −40°C to +125°C

Symbol	Parameter	Min	Max	Conditions
I_{CC}	Supply Current(1)		50 mA	f_{XTAL} = 16 MHz
I_{SLEEP}	Sleep Current(1) with V_{CC}/2 Output Enabled, No Load with V_{CC}/2 Output Disabled		 700 µA 100 µA	
I_{PD}	Powerdown Current(1)		25 µA	XTAL1 Clocked

NOTES:
**Typical value based on characterization data.
Port pins are weakly held after reset until the port configuration registers are written (9FH, AFH).
1. All pins are driven to V_{SS} or V_{CC} including RX0 and RX1.

PHYSICAL LAYER SPECIFICATIONS Load Condition: 100 pF

D.C. Characteristics V_{CC} = 5V ±10%; T_A = −40°C to +125°C

RX0/RX1 and TX0/TX1	Min	Max	Conditions
Input Voltage	−0.5V	V_{CC} + 0.5V	
Common Mode Range	V_{SS} + 1V	V_{CC} − 1V	
Differential Input Threshold	±100 mV		
Internal Delay 1: Sum of the Comparator Input Delay and the TX0/TX1 Output Driver Delay		60 ns	Load on TX0, TX1 = 100 pF, +100 mV to −100 mV RX0/RX1 differential
Internal Delay 2: Sum of the RX0 Pin Delay (if the Comparator is Bypassed) and the TX0/TX1 Output Driver Delay		50 ns	Load on TX0, TX1 = 100 pF
Source Current on Each TX0, TX1		−10 mA	V_{OUT} = V_{CC} − 1.0V
Sink Current on Each TX0, TX1		10 mA	V_{OUT} = 1.0V
Input Hysteresis for RX0/RX1		0V	
V_{CC}/2			
V_{CC}/2	2.38V	2.62V	I_{OUT} ≤ 75 µA, V_{CC} = 5V

CLOCKOUT SPECIFICATIONS

Load Condition: 50 pF

Parameter	Min	Max
CLOCKOUT Frequency	XTAL/15	XTAL

A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

Symbol	Parameter	Min	Max	Conditions
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz	
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz	
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz	
t_{AVLL}	Address Valid to ALE Low	7.5 ns		
t_{LLAX}	Address Hold after ALE Low	10 ns		
t_{LHLL}	ALE High Time	30 ns		
t_{LLRL}	ALE Low to RD# Low	20 ns		
t_{CLLL}	CS# Low to ALE Low	10 ns		
t_{QVWH}	Data Setup to WR# High	27 ns		
t_{WHQX}	Input Data Hold after WR# High	10 ns		
t_{WLWH}	WR# Pulse Width	30 ns		
t_{WHLH}	WR# High to Next ALE High	8 ns		
t_{WHCH}	WR# High to CS# High	0 ns		
t_{RLRH}	RD# Pulse Width This time is long enough to initiate a double read cycle by loading the High Speed Registers (04H, 05H), but is too short to READ from 04H and 05H (See t_{RLDV})	40 ns		
t_{RLDV}	RD# Low to Data Valid (Only for Registers 02H, 04H, 05H)	0 ns	55 ns	
t_{RLDV1}	RD# Low Data to Data Valid (for Registers except 02H, 04H, 05H) for Read Cycle without a Previous Write(1) for Read Cycle with a Previous Write(1)		 1.5 t_{MCLK} + 100 ns 3.5 t_{MCLK} + 100 ns	
t_{RHDZ}	Data Float after RD# High	0 ns	45 ns	
t_{CLYV}	CS# Low to READY Setup Condition: Load Capacitance on the READY Output: 50 pF		32 ns 40 ns	V_{OL} = 1.0V V_{OL} = 0.45V
t_{WLYZ}	WR# Low to READY Float for a Write Cycle if No Previous Write is Pending(2)		145 ns	
t_{WHYZ}	End of Last Write to READY Float for a Write Cycle if a Previous Write Cycle is Active(2)		2 t_{MCLK} + 100 ns	
t_{RLYZ}	RD# Low to READY Float (for registers except 02H, 04H, 05H) for Read Cycle without a Previous Write(1) for Read Cycle with a Previous Write(1)		 2 t_{MCLK} + 100 ns 4 t_{MCLK} + 100 ns	

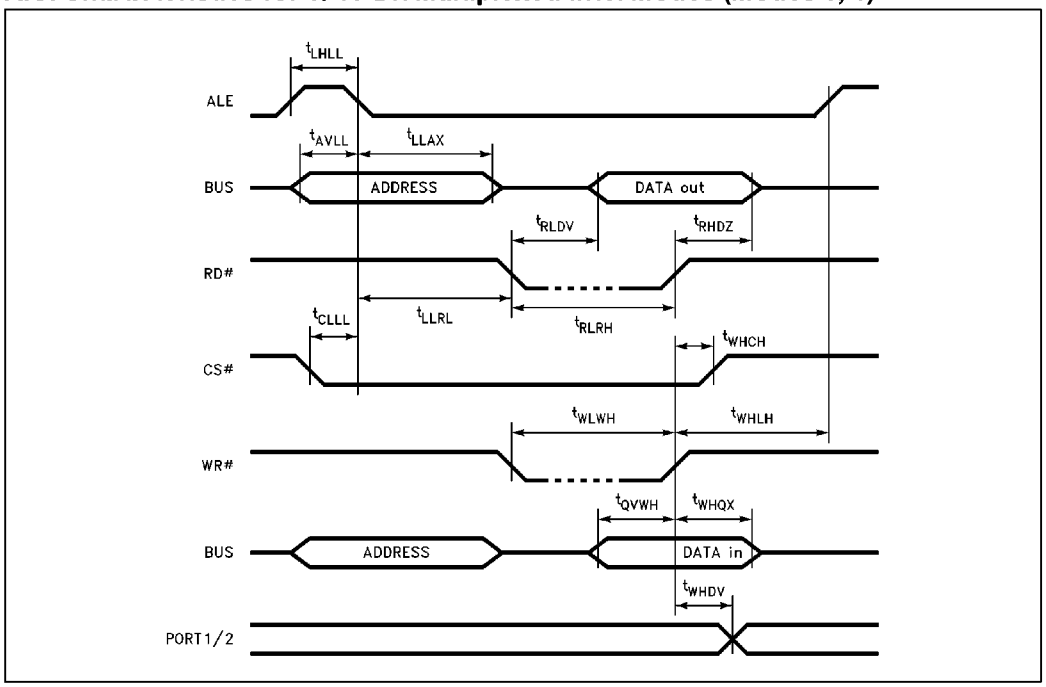
A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF (Continued)

Symbol	Parameter	Min	Max	Conditions
t_{WHDV}	WR# High to Output Data Valid on Port 1/2	t_{MCLK}	2 t_{MCLK} + 500 ns	
t_{COPO}	CLKOUT Period	(CD_V + 1) * t_{OSC}(3)		
t_{CHCL}	CLKOUT High Period	(CD_V + 1) * ½ t_{OSC} − 10	(CD_V + 1) * ½ t_{OSC} + 15	

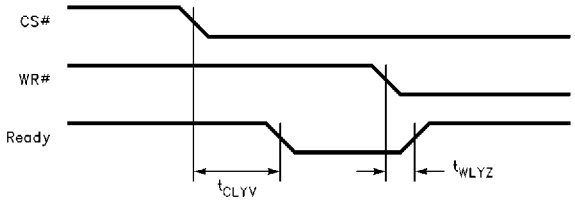
NOTES:
References to WR# also pertain to WRH#.
1. Definition of "read cycle without a previous write": The time between the rising edge of WR#/WRH# (for the previous write cycle) and the falling edge of RD# (for the current read cycle) is greater than 2 t_{MCLK}.
2. Definition of "write cycle with a previous write": The time between the rising edge of WR#/WRH# (for the previous write cycle) and the rising edge of WR#/WRH# (for the current write cycle) is less than 2 t_{MCLK}.
3. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)

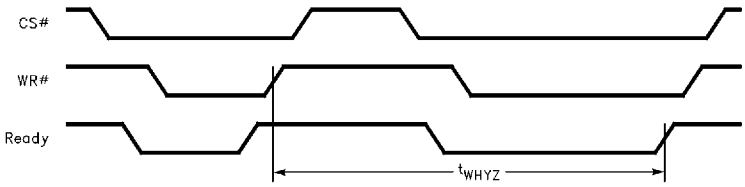


A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)

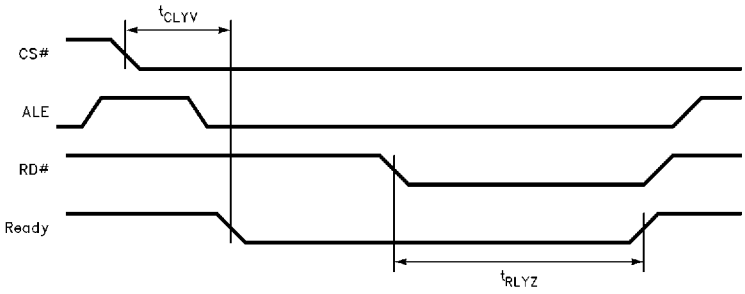
Ready Output Timing for a Write Cycle if No Previous Write is Pending



Ready Output Timing for a Write Cycle if a Previous Write Cycle is Active



Ready Output Timing for a Read Cycle



A.C. Characteristics for 8-Bit Multiplexed Non-Intel Mode (Mode 2)

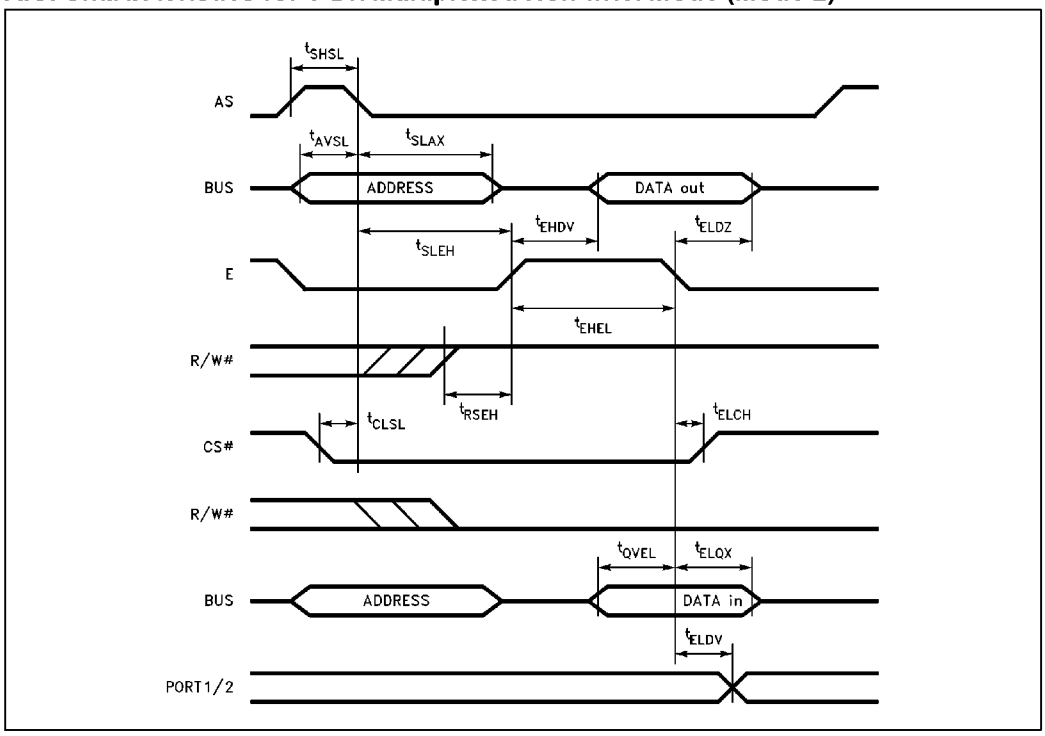
Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

Symbol	Parameter	Min	Max
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVSL}	Address Valid to AS Low	7.5 ns	
t_{SLAX}	Address Hold after AS Low	10 ns	
t_{ELDZ}	Data Float after E Low	0 ns	45 ns
t_{EHDV}	E High to Data Valid for Registers 02H, 04H, 05H	0 ns	45 ns
	for Read Cycle without a Previous Write(1) for Read Cycle with a Previous Write (for Registers except for 02H, 04H, 05H)		1.5 t_{MCLK} + 100 ns 3.5 t_{MCLK} + 100 ns
t_{QVEL}	Data Setup to E Low	30 ns	
t_{ELQX}	Input Data Hold after E Low	20 ns	
t_{ELDV}	E Low to Output Data Valid on Port 1/2	t_{MCLK}	2 t_{MCLK} + 500 ns
t_{EHEL}	E High Time	45 ns	
t_{ELEL}	End of Previous Write (Last E Low) to E Low for a Write Cycle	2 t_{MCLK}	
t_{SHSL}	AS High Time	30 ns	
t_{RSEH}	Setup Time of R/W# to E High	30 ns	
t_{SLEH}	AS Low to E High	20 ns	
t_{CLSL}	CS# Low to AS Low	20 ns	
t_{ELCH}	E Low to CS# High	0 ns	
t_{COPD}	CLKOUT Period	(CD_V + 1) * t_{OSC}(3)	
t_{CHCL}	CLKOUT High Period	(CD_V + 1) * ½ t_{OSC} − 10	(CD_V + 1) * ½t_{OSC} + 15

NOTES:

1. Definition of "Read Cycle without a Previous Write": The time between the falling edge of E (for the previous write cycle) and the rising edge of E (for the current read cycle) is greater than 2 t_{MCLK}.
2. Definition of "Write Cycle with a Previous Write": The time between the falling edge of E (for the previous write cycle) and the falling edge of E (for the current write cycle) is less than 2 t_{MCLK}.
3. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

A.C. Characteristics for 8-Bit Multiplexed Non-Intel Mode (Mode 2)



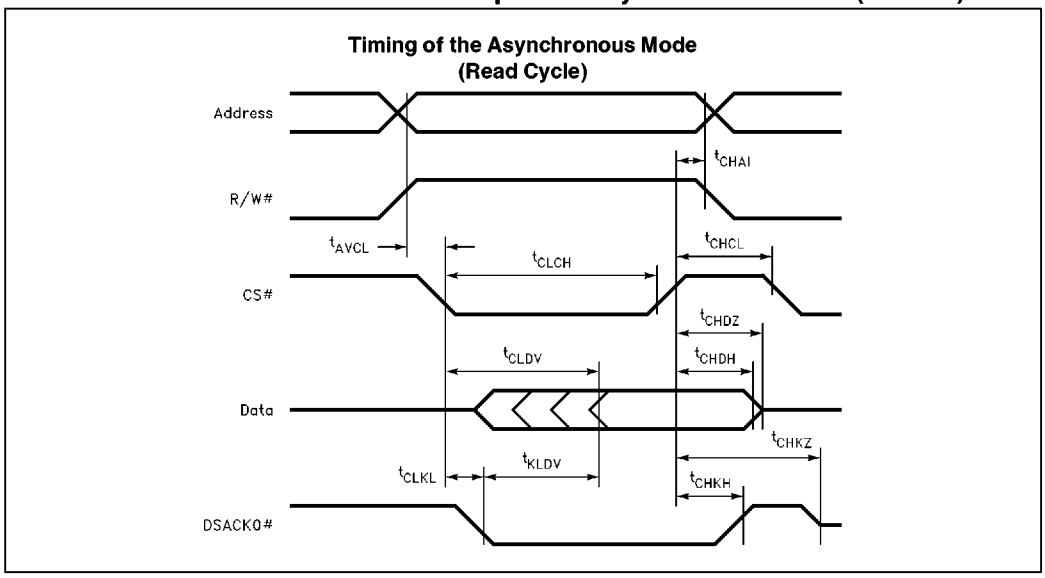
A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous (Mode 3)

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

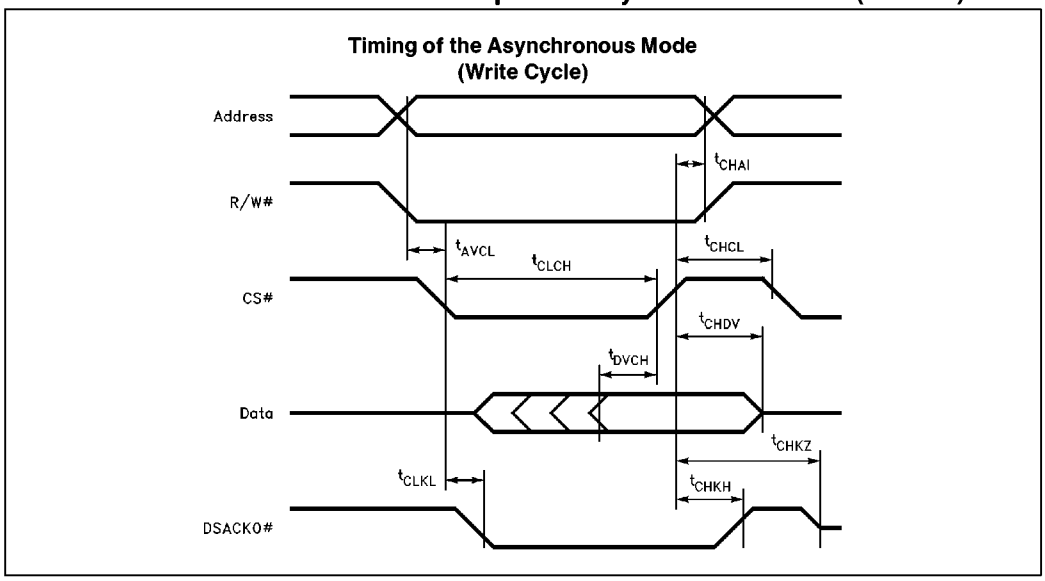
Symbol	Parameter	Min	Max
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVCL}	Address or R/W# Valid to CS# Low Setup	3 ns	
t_{CLDV}	CS# Low to Data Valid for High Speed Registers (02H, 04H, 05H)	0 ns	55 ns
	For Low Speed Registers (Read Cycle without Previous Write)(1)	0 ns	1.5 t_{MCLK} + 100 ns
	For Low Speed Registers (Read Cycle with Previous Write)(1)	0 ns	3.5 t_{MCLK} + 100 ns
t_{KLDV}	DSACK0# Low to Output Data Valid for High Speed Read Register		23 ns
	For Low Speed Read Register	<0 ns	
t_{CHDV}	82527 Input Data Hold after CS# High	15 ns	
t_{CHDH}	82527 Output Data Hold after CS# High	0 ns	
t_{CHDZ}	CS# High to Output Data Float		35 ns
t_{CHKH_1}	CS# High to DSACK0# = 2.4V(3)	0 ns	55 ns
t_{CHKH_2}	CS# High to DSACK0# = 2.8V		150 ns
t_{CHKZ}	CS# High to DSACK0# Float	0 ns	100 ns
t_{CHCL}	CS# Width between Successive Cycles	25 ns	
t_{CHAI}	CS# High to Address Invalid	7 ns	
t_{CHRI}	CS# High to R/W# Invalid	5 ns	
t_{CLCH}	CS# Width Low	65 ns	
t_{DVCH}	CPU Write Data Valid to CS# High	20 ns	
t_{CLKL}	CS# Low to DSACK0# Low for High Speed Registers and Low Speed Registers Write Access without Previous Write(2)	0 ns	67 ns
t_{CHKL}	End of Previous Write (CS# High) to DSACK0# Low for a Write Cycle with a Previous Write(2)	0 ns	2 t_{MCLK} + 145 ns
t_{COPD}	CLKOUT Period	(CD_V + 1) * t_{OSC}(4)	
t_{CHCL}	CLKOUT High Period	(CD_V + 1) * ½ t_{OSC} − 10	(CD_V + 1) * ½ t_{OSC} + 15

NOTES:
E and AS must be tied high in this mode.
1. Definition of "Read Cycle without a Previous Write": The time between the rising edge of CS# (for the previous write cycle) and the falling edge of CS# (for the current read cycle) is greater than 2 t_{MCLK}.
2. Definition of "Write Cycle without a Previous Write": The time between the rising edge of CS# (for the previous write cycle) and the rising edge of CS# (for the current write cycle) is greater than 2 t_{MCLK}.
3. An on-chip pullup will drive DSACK0# to approximately 2.4V. An external pullup is required to drive this signal to a higher voltage.
4. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous Mode (Mode 3)



A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous Mode (Mode 3)



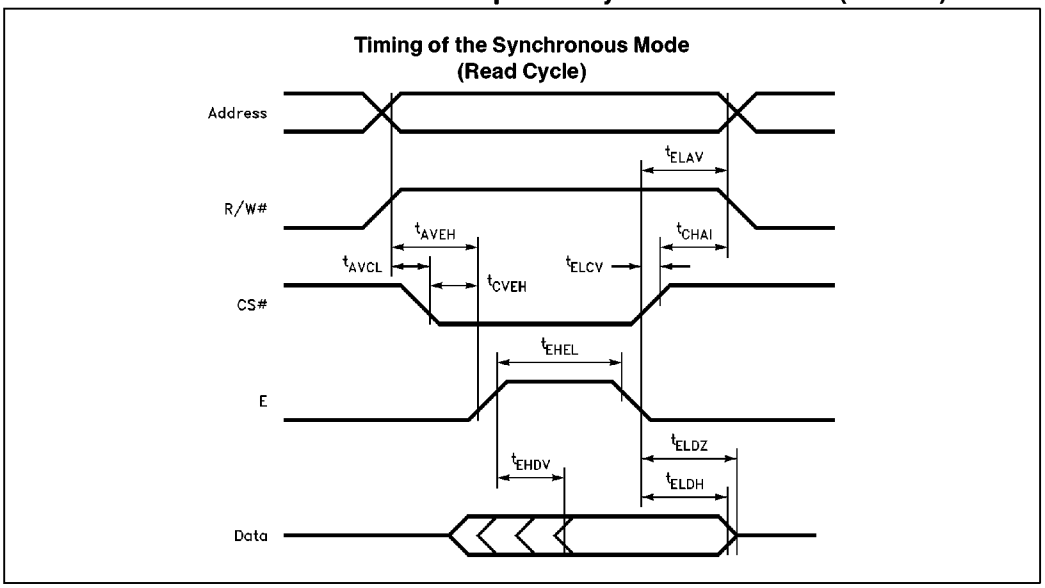
A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

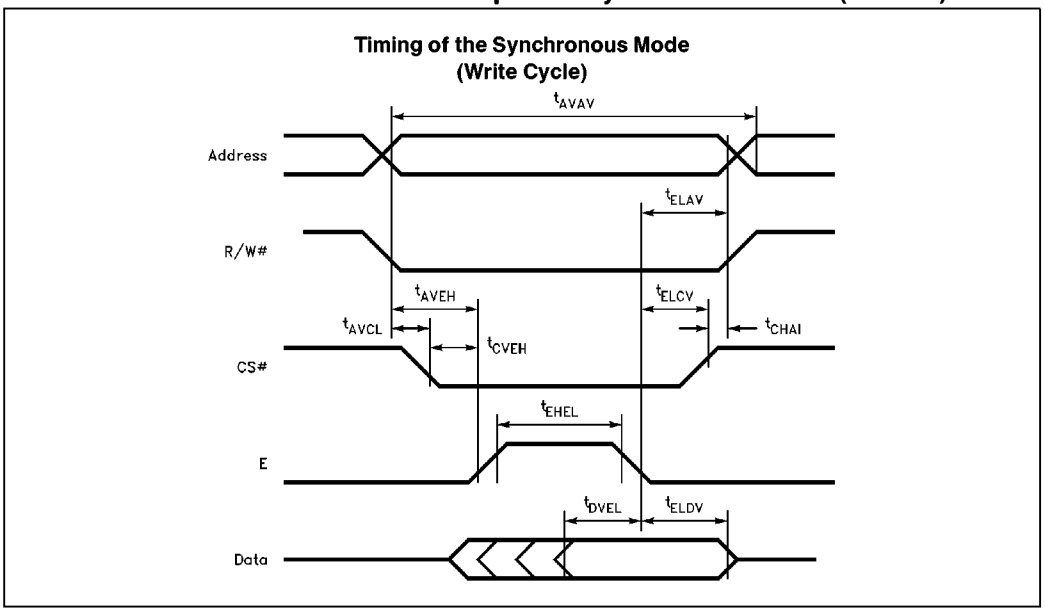
Symbol	Parameter	Min	Max
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{EHDV}	E High to Data Valid out of High Speed Register (02H, 04H, 05H)		55 ns
	Read Cycle without Previous Write for Low Speed Registers(1)		1.5 t_{MCLK} + 100 ns
	Read Cycle with Previous Write for Low Speed Registers(1)		3.5 t_{MCLK} + 100 ns
t_{ELDH}	Data Hold after E Low for a Read Cycle	5 ns	
t_{ELDZ}	Data Float after E Low		35 ns
t_{ELDV}	Data Hold after E Low for a Write Cycle	15 ns	
t_{AVEH}	Address and R/W# to E Setup	25 ns	
t_{ELAV}	Address and R/W# Valid after E Falls	15 ns	
t_{CVEH}	CS# Valid to E High	0 ns	
t_{ELCV}	CS# Valid after E Low	0 ns	
t_{DVEL}	Data Setup to E Low	55 ns	
t_{EHEL}	E Active Width	100 ns	
t_{AVAV}	Start of a Write Cycle after a Previous Write Access	2 t_{MCLK}	
t_{AVCL}	Address or R/W# to CS# Low Setup	3 ns	
t_{CHAI}	CS# High to Address Invalid	7 ns	
t_{COPD}	CLKOUT Period	(CD_V + 1) * t_{OSC}(2)	
t_{CHCL}	CLKOUT High Period	(CD_V + 1) * ½ t_{OSC} − 10	(CD_V + 1) * ½ t_{OSC} + 15

NOTES:
1. Definition of "Read Cycle without a Previous Write": The time between the falling edge of E (for the previous write cycle) and the rising edge of E (for the current read cycle) is greater than 2 t_{MCLK}.
2. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)



A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)



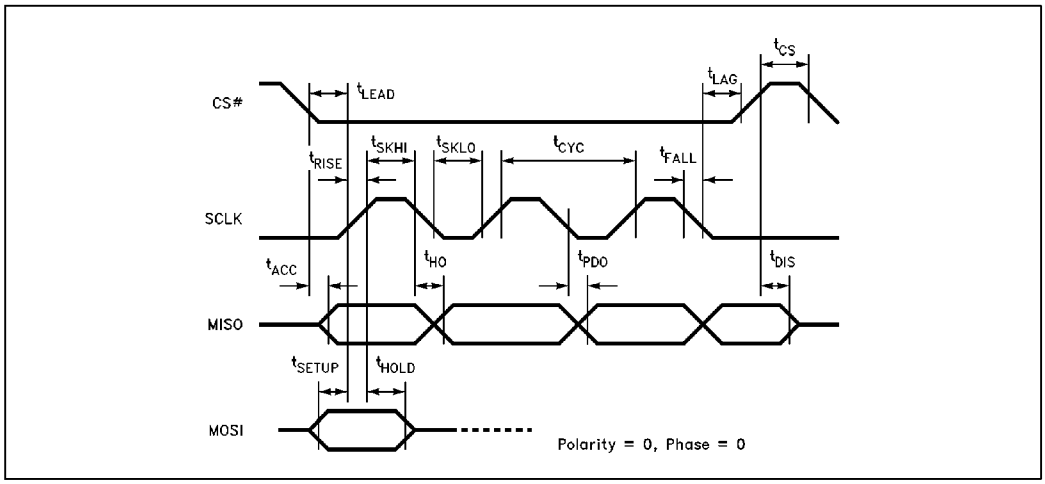
A.C. Characteristics for Serial Interface Mode

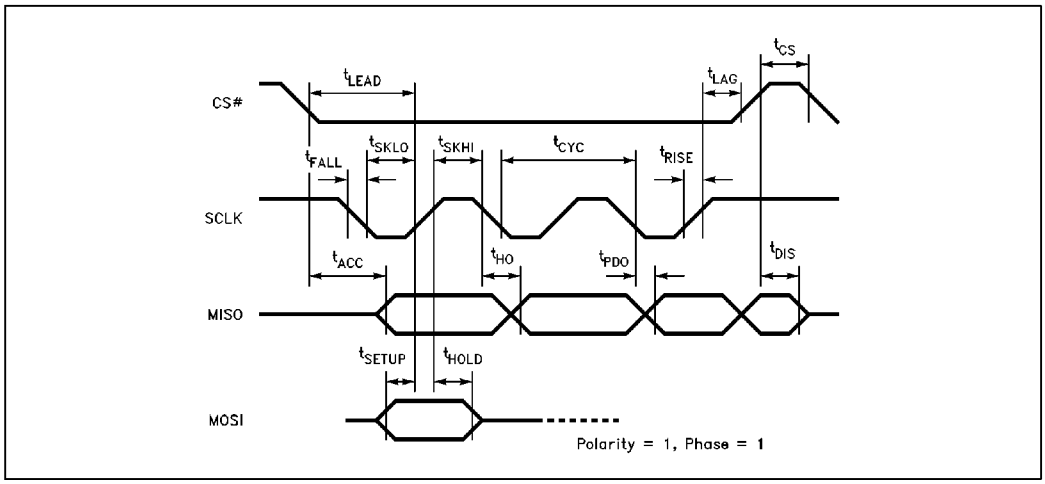
Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

Symbol	Parameter	Min	Max
SCLK	SPI Clock	0.5 MHz	8 MHz
t_{CYC}	1/SCLK	125 ns	2000 ns
t_{SKHI}	Minimum Clock High Time	84 ns	
t_{SKLO}	Minimum Clock Low Time	84 ns	
t_{LEAD}	ENABLE Lead Time	70 ns	
t_{LAG}	Enable Lag Time	109 ns	
t_{ACC}	Access Time		60 ns
t_{PDO}	Maximum Data Out Delay Time		59 ns
t_{HO}	Minimum Data Out Hold Time	0 ns	
t_{DIS}	Maximum Data Out Disable Time		665 ns
t_{SETUP}	Minimum Data Setup Time	35 ns	
t_{HOLD}	Minimum Data Hold Time	84 ns	
t_{RISE}	Maximum Time for Input to go from V_{OL} to V_{OH}		100 ns
t_{FALL}	Maximum Time for Input to go from V_{OH} to V_{OL}		100 ns
t_{CS}	Minimum Time between Consecutive CS# Assertions	670 ns	
t_{COPD}	CLKOUT Period	$(CD_V + 1) * t_{OSC}$(1)	
t_{CHCL}	CLKOUT High Period	$(CD_V + 1) * ½ t_{OSC} - 10$	$(CD_V + 1) * ½ t_{OSC} + 15$

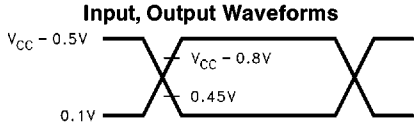
NOTE:
1. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

A.C. Characteristics for Serial Interface Mode





A.C. TESTING INPUT



NOTE:
AC Inputs during testing are driven at V_{CC} – 0.5V for a Logic "1" and 0.1V for a Logic "0". Timing measurements are made at V_{OH} Min for a Logic "1" and V_{OL} Max for a Logic "0".

DATA SHEET REVISION HISTORY

This is the -006 revision of the 82527 data sheet. The following differences exist between the -005 version and the -006 revision. There were no specification changes between the -004 version and the -005 revision.

1. The 82527 44-ld QFP was added to the product description, the pinmap for the QFP package is also included.
2. The pin numbers were removed from the pin description list to accommodate the new 44-ld QFP package.

3. Removed XTAL1 and XTAL2 from the exceptions for V_{IL} spec. XTAL1 V_{IL} is now specified at min = −0.5V, max = 0.8V. XTAL2 is an output.
4. Removed XTAL1 and XTAL2 from the exceptions for V_{IH} spec. XTAL1 V_{IH} is now specified at min = 3.0V, max = V_{CC} + 0.5V. XTAL2 is an output.
5. Source and Sink current for TX0 and TX1 were corrected from minimum values to maximum values.
6. Mode 2; The t_{AVSL} specification was decreased to 7.5 ns from 33 ns.
7. Mode 2; The t_{SLAX} specification was decreased to 10 ns from 20 ns.
8. Mode 3, Asynchronous; The t_{DVCH} specification was decreased to 20 ns from 32 ns.
9. All modes; Two specifications were added for CLKOUT. These specifications are t_{COPD} (CLKOUT Period) = $(CD_V + 1)*t_{OSC}$, and t_{CHCL} (CLKOUT High Period) = min $(CD_V + 1) * ½ t_{OSC} - 10$ ns and max $(CD_V + 1) * ½ t_{OSC} + 15$ ns. **NOTE:** CD_V represented the value loaded in the lower nibble of the CLKOUT Register (1FH).
10. Serial Interface Mode; The maximum SCLK (SPI Clock) rate was increased to 8 MHz from 4.2 MHz. The minimum t_{CYC} (1/SCLK) was set at 125 ns from 238 ns to reflect the increased maximum SPI clock rate.
11. MODE0/1, the t_{WHQX} Specifications was decreased to 10 ns from 12.5 ns.

This is the -004 revision of the 82527 data sheet. The following differences exist between the -003 version and the -004 revision.

1. Remove notice on page 1 concerning Advance Information Data Sheet.
2. Page 4, AS pin description, add "pin tied high in Asycnhronous mode 3".
3. Page 4, E pin description, add "pin tied high in mode 3".
4. Page 5, add V_{IH} = 0.7 V_{CC} and V_{IL} = 0.3 V_{CC} for LSIO port pins (pins not used to interface to host-CPU).
5. Page 6, change Differential Input Threshold from MAX spec to MIN spec.
6. Page 6, add Input Hysteresis spec for RX0/RX1 = 0V maximum.
7. Page 7, t_{LLAX} decreased from 20 ns to 10 ns (to interface to 20 MHz C196).
8. Page 7, t_{QVWH} decreased from 30 ns to 27 ns (to interface to 20 MHz C196).
9. Page 7, t_{WLWH} decreased from 40 ns to 30 ns (to interface to 20 MHz C196).
10. Page 7, t_{RLDV} increased from 45 ns to 55 ns.
11. Page 12, t_{CHKH} specification added for V_{IH} = 2.8V = 150 ns.
12. Page 12, t_{CHAI} decreased from 10 ns to 7 ns.
13. Page 13, timing diagram for t_{AVCL} revised to show common CL low level.
14. Page 14, t_{CHAI} decreased from 10 ns to 7 ns.

15. Page 7, t_{CLLL} decreased from 20 ns to 10 ns.
16. Page 3, RESET# description addition:

    Warm reset: (V_{CC} remains valid while RESET# is asserted), RESET# must be driven to a valid low level for 1 ms minimum.

    Cold reset: (V_{CC} is driven to a valid level while RESET# is asserted, RESET# must be driven low for 1 ms minimum measured from a valid V_{CC} level. No falling edge on the reset pin is required during a cold reset event.
17. Page 2, Figure 2: Pin 7 name changed to (WR#/WRL#)/(R/W#) from WR#/(R/W#).
18. Page 4, pin description name changed to (WR#/WRL#)/(R/W#) from WR#/(R/W#) and WR# in 8-bit Intel mode and WRL# in 16-bit Intel mode replaces the description WR# used for Intel modes.
19. Page 5, ABSOLUTE MAXIMUM RATINGS addition: Laboratory testing shows the 82527 will withstand up to 10 mA for injected current into both RX0 and RX1 pins for a total of 20 days without sustaining permanent damage. This high current condition may be the result of shorted signal lines. The 82527 will not function properly if the RX0/RX1 input voltage exceeds V_{CC} + 0.5V.
20. Page 12, t_{CHDV} decreased from 25 ns to 15 ns.
21. Page 14, t_{ELDV} decreased from 25 ns to 15 ns.
22. Page 7, t_{AVLL} decreased from 20 ns to 7.5 ns.
23. Page 7, t_{WHQX} decreased from 20 ns to 12.5 ns.

This is the -003 revision of the 82527 data sheet. The following differences exist between the -002 version and the -003 revision.

1. The data sheet has been revised to ADVANCE from PRELIMINARY, indicating the specifications have been verified through electrical tests.
2. ABSOLUTE MAXIMUM RATINGS have been added.
3. V_{IL} no longer applies to the AD0–AD7 pins in CPU Interface mode 3.
4. V_{IL1} has been added to specify Input Low Voltage for AD0–AD7 pins in CPU Interface mode 3 as −0.5V minimum and +0.5V maximum.
5. I_{CC} supply current has been reduced to 50 mA from 100 mA.
6. Note 2 was added stating during I_{PD} testing, all pins are driven to V_{SS} or V_{CC}, including RX0 and RX1.
7. t_{AVLL} has been decreased to 20 ns from 33 ns.
8. t_{RLDV1} has been decreased to 1.5 t_{MCLK} + 100 ns from 2 t_{MCLK} + 100 ns for a Read Cycle without a previous Write (Modes 0, 1).

   t_{RLDV1} has been decreased to 3.5 t_{MCLK} + 100 ns from 4 t_{MCLK} + 100 ns for a Read Cycle with a previous Write (Modes 0, 1).
9. t_{CLYV} has added the condition of V_{OL} = 1.0V for a 32 ns delay. t_{CLYV} is 40 ns for V_{OL} = 0.45 (Modes 0, 1).
10. t_{WHYZ} has been decreased to 2 t_{MCLK} + 100 ns from 2 t_{MCLK} + 145 ns (Modes 0, 1).
11. t_{EHDV} has been decreased to 1.5 t_{MCLK} + 100 ns from 2 t_{MCLK} + 100 ns for a Read Cycle without a previous Write (Mode 2).

    t_{EHDV} has been decreased to 3.5 t_{MCLK} + 100 ns from 4 t_{MCLK} + 100 ns for a Read Cycle with a previous Write (Mode 2).
12. t_{ELEL} has been decreased to 2 t_{MCLK} from 2 t_{MCLK} + 145 ns (Mode 2).
13. t_{CLDV} has been decreased to 55 ns from 65 ns (Mode 3).
14. t_{CHKH} is specified for V_{IH} = 2.4V, decreased from V_{IH} = 3.0V. Note 3 has been added which states an on-chip pullup will drive DSACK0# to approximately 2.4V. An external pullup is required to drive this signal to a higher voltage (Mode 3).
15. t_{CHAI} has been increased to 10 ns from 5 ns. t_{CHAI} no longer includes CS# High to R/W# Invalid (Mode 3).
16. t_{CHRI} = 5 ns has been added to specify CS# High to R/W# Invalid (Mode 3).
17. t_{EHDV} has been decreased to 55 ns from 65 ns for Reads of the High Speed Registers (Mode 3).
18. t_{EHDV} has been decreased to 1.5 t_{MCLK} + 100 ns from 2 t_{MCLK} + 100 ns for a Read Cycle without a previous Write (Mode 3).

    t_{EHDV} has been decreased to 3.5 t_{MCLK} + 100 ns from 4 t_{MCLK} + 100 ns for a Read Cycle with a previous Write (Mode 3).
19. The t_{AVAL} specification name has been corrected to t_{AVAV} (Mode 3).
20. t_{CHAI} has been increased to 10 ns from 5 ns (Mode 3).
21. The input voltage in the A.C. Testing Input Diagram have been revised to V_{CC} − 0.5V from 3.0V (high level) and revised to 0.1V from 0.8V (low level).

The following differences exist between the -001 version and the -002 revision.

1. The RAM block in Figure 1. 82527 Block Diagram was previously called DPRAM.
2. The INT#/(V_{CC}/2) pin in Figure 2. 44-Pin PLCC Package and in other descriptions was previously called the INT#/(V_{DD}/2) pin.
3. The Mode0 and Mode1 pin descriptions were modified to include the following note: These pins are weakly held low during reset.
4. The DSACK0# pin description was changed to reflect an open-drain output.
5. V_{IL1} for RX0 in comparator bypass mode was added.
6. V_{IH1} hysteresis on RESET# was added.
7. V_{IH2} for RX0 in comparator bypass mode was added.
8. I_{SLEEP} current with V_{CC}/2 output enabled was corrected from 700 μA minimum to 700 μA maximum.
9. I_{SLEEP} current with V_{CC}/2 output disabled was corrected from 100 μA minimum to 100 μA maximum.
10. I_{PD} current was changed from 10 μA minimum to 25 μA maximum.
11. The following note was added to the electrical characteristics: Port pins are weakly held high after reset until the port configuration registers are written (9FH, AFH).
12. The following D.C. Characteristics Specifications have been removed and replaced by the Internal Delay 1 and Internal Delay 2 specifications. These specifications reflect the production test methodology which requires these two delays to be tested together.
    a. Delay Dominant to Recessive
    b. Delay Recessive to Dominant
    c. Input Delay with Comparator Bypassed
    d. Rise Time
    e. Fall Time
13. The following A.C. Characteristics for 8-Bit/16-Bit Multiplexed Intel Modes (Modes 0,1) have been changed:
    a. $1/t_{MCLK}$ has been increased to 8 MHz from 5 MHz.
    b. t_{LLAX} has been decreased to 20 ns from 22.5 ns.
    c. t_{LLRL} has been increased to 20 ns from 0 ns.
    d. t_{CLLL} has been added.
    e. t_{WHLH} has been increased to 8 ns from 0 ns.
    f. t_{WHCH} has been added.
    g. t_{RLDV1} has been added.
    h. t_{WLYH} has been changed to t_{WLYZ} to reflect the READY pin is an open-drain output.
    i. t_{WHYH} has been changed to t_{WHYZ} to reflect the READY pin is an open-drain output.
    j. t_{RLYH} has been changed to t_{RLYZ} to reflect the READY pin is an open-drain output.
    k. t_{WHDV} has been increased to 2 t_{MCLK} + 250 ns from 2 t_{MCLK} + 100 ns.
    l. The following note was added: References to WR# also pertain to WRH#.
    m. The following definition was added for a "read cycle without a previous write": The time between the rising edge of WR#/WRH# (for the previous write cycle) and the falling edge of RD# (for the current read cycle) is greater than 2 t_{MCLK}.
    n. The following definition was added for a "write cycle with a previous write": The time between the rising edge of WR#/WRH# (for the previous write cycle) and the next rising edge of WR#/WRH# (for the current write cycle) is less than 2 t_{MCLK}.

14. The timing diagrams for 8-Bit/16-Bit Multiplexed Intel Modes (Modes 0,1) have been changed to show ALE rising before CS# falls.
15. The following A.C. Characteristics for 8-Bit Multiplexed Non-Intel Modes (Modes 2) have been changed:
    a. $1/t_{MCLK}$ has been increased to 8 MHz from 5 MHz.
    b. t_{SLAX} has been decreased to 20 ns from 22.5 ns.
    c. t_{EVDV} has been decreased to (2, 4) t_{MCLK} + 100 ns from (2, 4) t_{MCLK} + 145 ns.
    d. t_{ELDV} minimum has been decreased to t_{MCLK} from t_{MCLK} + 100 ns.
    e. t_{ELDV} maximum has been increased to 2 t_{MCLK} + 500 ns from 2 t_{MCLK} + 100 ns.
    f. t_{EHEL} for registers except 02H, 04H, 05H has been renamed to t_{ELEL} and the specification has been decreased to 2 t_{MCLK} + 145 ns from 4 t_{MCLK} + 145 ns.
    g. t_{SLEH} has been increased to 20 ns from 0 ns.
    h. t_{CLSL} has been added.
    i. t_{ELCH} has been added.
    j. The following definition was added for a "read cycle without a previous write": The time between the falling edge of E (for the previous write cycle) and the rising edge of E (for the current read cycle) is greater than 2 t_{MCLK}.
    k. The following definition was added for a "write cycle with a previous write": The time between the falling edge of E (for the previous write cycle) and the next falling edge of E (for the current write cycle) is less than 2 t_{MCLK}.
16. The following A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous Mode (Mode 3) have been changed:
    a. $1/t_{MCLK}$ has been increased to 8 MHz from 5 MHz.
    b. t_{CLDV} has been decreased for low speed registers to (2, 4) t_{MCLK} + 100 ns from (2, 4) t_{MCLK} + 145 ns.
    c. t_{CHKH} comment "with 3.3 KΩ Pullup and 100 pF Load" has been removed since t_{CHKH} is tested with a current source.
    d. t_{CLKL} for a Write Access with a Previous Write has been renamed to t_{CHKL}.
    e. The note "E and AS must be tied high in this mode" has been added.
    f. The following definition was added for a "read cycle without a previous write": The time between the rising edge of CS# (for the previous write cycle) and the falling edge of CS# (for the current read cycle) is greater than 2 t_{MCLK}.
    g. The following definition was added for a "write cycle with a previous write": The time between the rising edge of CS# (for the previous write cycle) and the next rising edge of CS# (for the current write cycle) is less than 2 t_{MCLK}.
17. The following A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3) have been changed:
    a. $1/t_{MCLK}$ has been increased to 8 MHz from 5 MHz.
    b. t_{ELDZ} minimum has been removed.
    c. t_{AVCL} has been added.
    d. t_{CHAI} has been added.
    e. The following definition was added for a "read cycle without a previous write": The time between the falling edge of E (for the previous write cycle) and the rising edge of E (for the current read cycle) is greater than 2 t_{MCLK}.
    f. The following definition was added for a "write cycle with a previous write": The time between the falling edge of E (for the previous write cycle) and the next falling edge of E (for the current write cycle) is less than 2 t_{MCLK}.
18. The following A.C. Characteristics for Serial Interface Mode have been changed:
    a. t_{SKHI} has been decreased to 84 ns from 119 ns.
    b. t_{SKLO} has been decreased to 84 ns from 119 ns.
    c. t_{PDO} has been decreased to 59 ns from 84 ns.
    d. t_{SETUP} has been decreased to 35 ns from 59 ns.
    e. t_{HOLD} has been decreased to 84 ns from 109 ns.
19. The note in the A.C. Testing Input diagram referenced V_{OH} was previously named V_{IH}.

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