

**7N90**

Preliminary

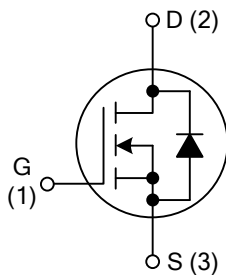
Power MOSFET**900V N-CHANNEL POWER MOSFET****DESCRIPTION**

The UTC **7N90** is an N-channel mode Power FET using UTC's advanced technology to provide costumers with planar stripe and DMOS technology. This technology specializes in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **7N90** is universally applied in active power factor correction, electronic lamp ballast based on half bridge topology and high efficient switched mode power supply.

FEATURES

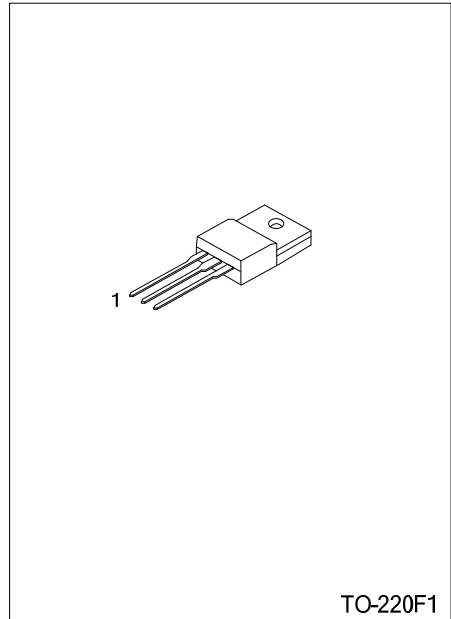
- * High switching speed
- * 7.0A, 900V, $R_{DS(ON)}=1.8\Omega$ @ $V_{GS}=10V$
- * Typically 40nC low gate charge
- * 100% avalanche tested
- * Typically 17pF low C_{RSS}
- * Improved dv/dt capability

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7N90L-TF1-T	7N90G-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

7N90L-TF1-T (1) Packing Type (2) Package Type (3) Lead Plating	(1) T: Tube (2) TF1: TO-220F1 (3) G: Halogen Free, L:Lead Free
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TO-220F1

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}	900	V
Gate to Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current	$T_C=25^{\circ}\text{C}$	I_D	7.0
	$T_C=100^{\circ}\text{C}$		4.4
Pulsed Drain Current (Note 1)	I_{DM}	28	A
Avalanche Current (Note 1)	I_{AR}	6.4	A
Single Pulsed Avalanche Energy (Note 2)	E_{AS}	780	mJ
Repetitive Avalanche Energy (Note 1)	E_{AR}	21	mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.0	V/ns
Power Dissipation	P_D	32	W
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Note : Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Junction-to-Case	θ_{JC}		3.87	$^{\circ}\text{C/W}$
Junction-to-Ambient	θ_{JA}		62.5	$^{\circ}\text{C/W}$

■ ELECTRICAL CHARACTERISTICS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)



PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	900			V
Breakdown Voltage Temperature Coefficient		ΔBV _{DSS} /ΔT _J	I _D =250μA, Referenced to 25°C		0.96		V/°C
Drain-Source Leakage Current		I _{DSS}	V _{DS} =900V, V _{GS} =0V			10	μA
			V _{DS} =720V, T _C =125°C			100	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{DS} =0V ,V _{GS} =30V			100	nA
	Reverse	I _{GSS}	V _{DS} =0V ,V _{GS} =-30V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	3.0		5.0	V
Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =3.5A		1.5	1.8	Ω
Forward Transconductance		g _{FS}	V _{DS} =50V, I _D =3.5A (Note 4)		5.7		S
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =25V,V _{GS} =0V,f=1.0MHz		1440	1880	pF
Output Capacitance		C _{OSS}			140	185	pF
Reverse Transfer Capacitance		C _{RSS}			17	23	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =720V, V _{GS} =10V, I _D =7.0A (Note 4,5)		40	52	nC
Gate-Source Charge		Q _{GS}			8.5		nC
Gate-Drain Charge		Q _{GD}			20		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =450V, I _D =7.0A, R _G =25Ω (Note 4.,5)		35	80	ns
Turn-ON Rise Time		t _R			80	170	ns
Turn-OFF Delay Time		t _{D(OFF)}			95	200	ns
Turn-OFF Fall Time		t _F			55	120	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				6.4	A
Maximum Body-Diode Pulsed Current		I _{SM}				25.6	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =7.0A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{RR}	V _{GS} =0V, I _S =7.0A,		400		ns
Body Diode Reverse Recovery Charge		Q _{RR}	dI _F /dt=100A/μs (Note 4)		4.3		μC

Notes : 1. Repetitive Rating : Pulse width limited by maximum junction temperature

2. $L=30mH, I_{AS}=7.0A, V_{DD}=50V, R_G=25\Omega$, Starting $T_J=25^\circ C$

3. $I_{SD} \leq 7.0A, di/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ C$

4. Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

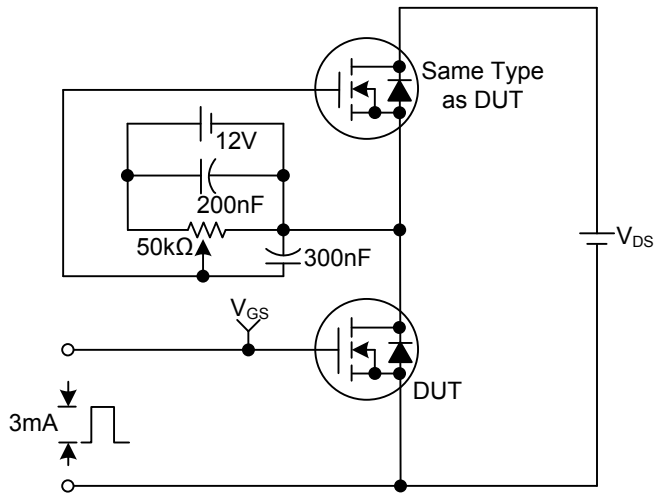
5. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

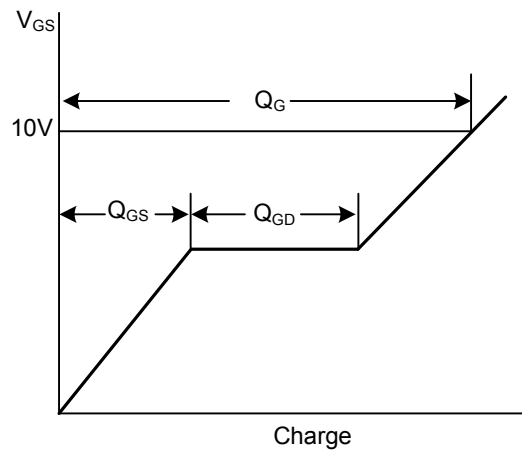
dv/dt controlled by R_G
 I_{SD} controlled by pulse period



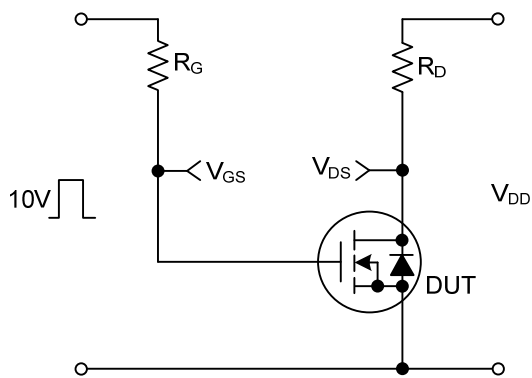
Gate Charge Test Circuit



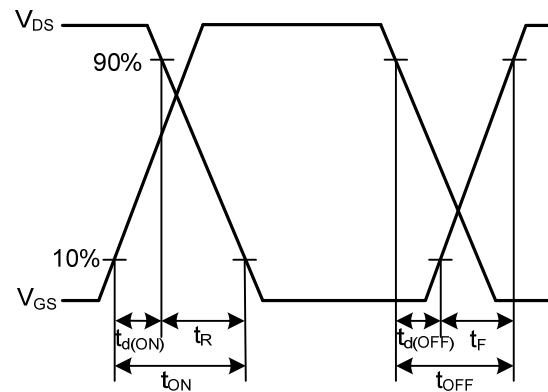
Gate Charge Waveforms



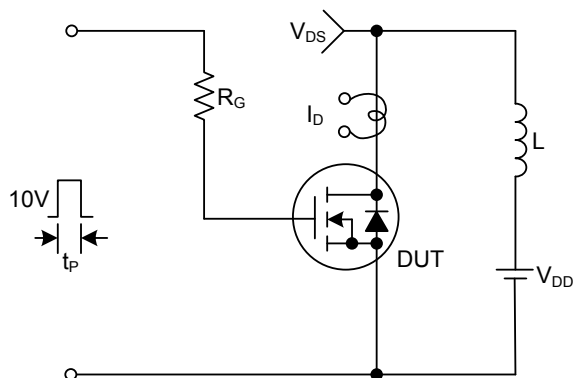
Resistive Switching Test Circuit



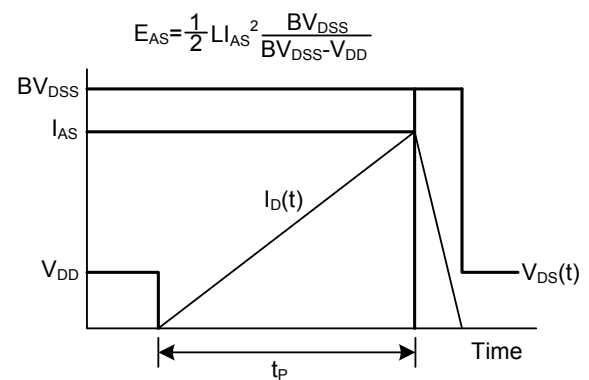
Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



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