78P2352-DB STM1e/E4/OC3 Demo Board

DEMO BOARD MANUAL

AUGUST 2005

INTRODUCTION

This manual will explain the design and operation of the 78P2352-DB demo board (Board rev. D2352T8**C**). The 78P2352 is TERIDIAN's latest dual channel Line Interface Unit (LIU) for 155Mbit/s SONET/SDH (OC-3 or STM-1e) and 140Mbit/s PDH (E4) applications.

DESCRIPTION

The 78P2352-DB demo board is designed to facilitate easy evaluation of the 78P2352 Line Interface Unit (LIU) in the electrical (coaxial) domain. The board can be easily configured into different operating modes with the on board configuration headers and dipswitches. On the line side, all the necessary discrete components are included for transmitting and receiving CMI signal on the 75Ω coaxial line.

If needed, all other discrete components can be populated to support the optical line interface.

FEATURES

- Allows easy evaluation of the 78P2352
- Includes configuration headers and dipswitches for HW control options
- Link status LEDs for both channels
- Options for using on-board crystal oscillator or external reference clock
- 17.408MHz and 19.44MHz on-board crystal oscillators allow easy evaluations of PDH and SDN/SONET applications.
- 48-pin box connector for parallel (nibble) interface
- SMA connectors for serial (LVPECL) interface
- 3.3V power supply

ORDERING INFO

PART DESCRIPTION	ORDER NUMBER
78P2352-IGT Demo Board	78P2352-DB

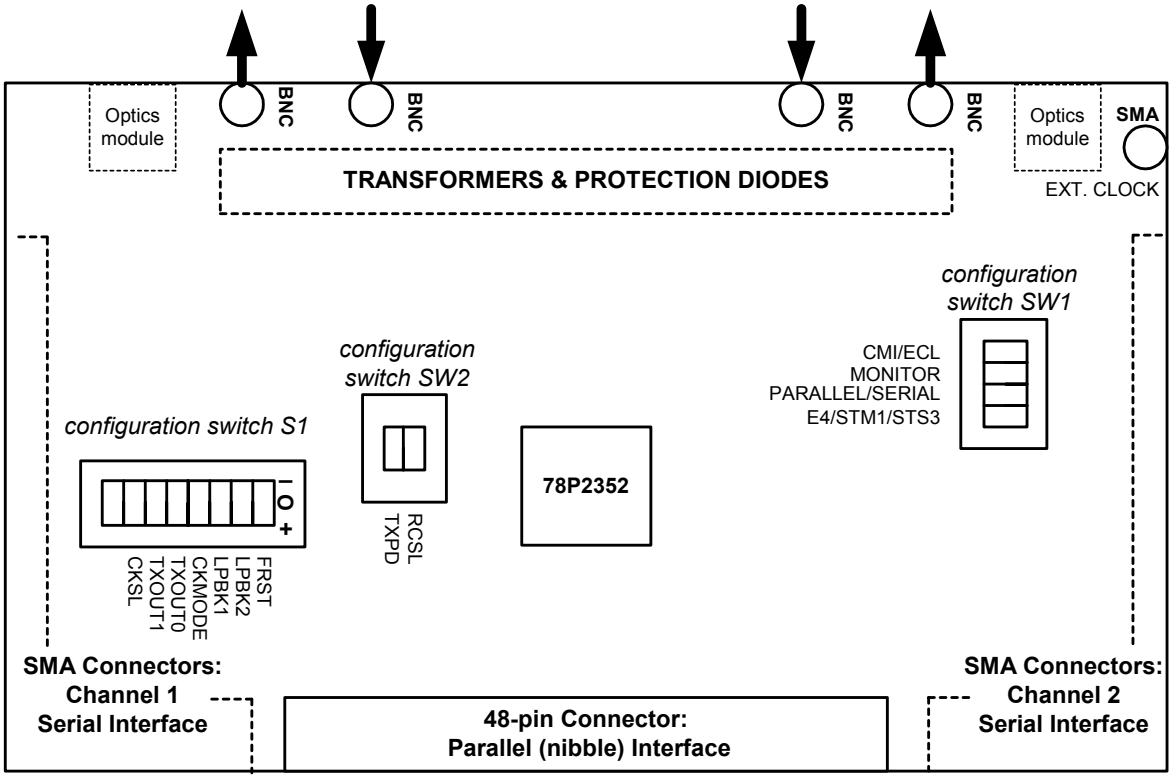


FIGURE 1: D2352T8**C** board block diagram

REQUIRED EQUIPMENT

- TERIDIAN D2352T8**C** demo board
- Power Supply, 3.3V, 1.5Amp
- Banana Plug Connection Cable for Power Supply
- 75Ω coax cable set.
- Test Equipment (Signal Source generator, Jitter Measurement, etc.)

GETTING STARTED

1. Configurations for the headers:
   a) **JP1**: Shunt connects to P/S to use SW1
   b) **JP2**: Shunt connects to E/S to use SW1
   c) **JP3**: Shunt connects to GND to use hardware control mode
   d) **JP4**: Shunt connects to MON to use SW1
   e) **JP5**: Shunt connects to C/E to use SW1
   f) **JP6**: Connect shunt to E4 to use 19.44M XO for STM-1/STS-3 mode or connect to STM1 to use 17.408M XO for E4 mode
   g) **JP7**: Connect shunt to LOC to use on-board crystal oscillators for reference clock or connect to EXT to use external clock source provided at (CKREF) SMA connector
2. Configurations for the dipswitches:

   Typical settings in **Bold**

   SW1

   Pin 1: Line Interface Select
   - **CMI** or ECL
   - *See SEN_CMI pin description in datasheet*

   Pin 2: Receiver Monitor Mode
   - Enabled or **Disabled**
   - *See SCK_MON pin description in datasheet*

   Pin 3: System Interface Select
   - Parallel or **Serial**
   - *See SDI_PAR pin description in datasheet*

   Pin 4: Rate Select
   - E4 or **SMT1/STS3**
   - *See SDO_E4 pin description in datasheet*

   SW2

   Pin 1: Transmitter Power Down
   - Enabled or **Disabled**
   - *See TXPD pin description in datasheet*

   Pin 2: Redundant Channel
   - Enabled or **Disabled**
   - *Not used in 78P2352*

   S1

   Pin 1: FIFO phase initialization
   - **Float** (normal operation)
   - *See FRST pin description in datasheet*

   Pin 2: Channel 2 Loopback
   - **Float** (remote loopback)
   - *See LPBK2 pin description in datasheet*

   Pin 3: Channel 1 Loopback
   - **Float** (remote loopback)
   - *See LPBK1 pin description in datasheet*

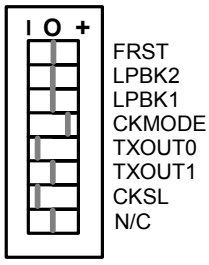
   Pin 4: Clock (timing) Mode Select
   - **High** (plesiochronous mode)
   - *See CKMODE pin description in datasheet*

   Pin 5: CMI Tx Amplitude Boost
   - **Low** (normal)
   - *See TXOUT0 pin description in datasheet*

   Pin 6: CMI Tx Peaking Control
   - **Float** (no peaking)
   - *See TXOUT1 pin description in datasheet*

   Pin 7: Reference clock frequency
   - **Low** (17.408MHz or 19.44MHz)
   - *See CKSL pin description in datasheet*

   Pin 8: unused



Typical S1 settings

3. Apply 3.3V power to the demo board

DEMO BOARD DESCRIPTION

CONFIGURING BIT RATE

The D2352T8**C** can be configured for either E4 or STS3/STM1 rates by **SW1** (pin 4).

A corresponding reference clock input is required for operation. The compatible reference clocks for each rate are as follows:

Rate	Reference Clock
E4	17.408MHz, 139.264 MHz
STS3 /STM1	19.44MHz, 77.76MHz, 155.52 MHz

S1 (pin 7) is used to configure the reference clock frequency based on the selected bit rate.

CKSL	Reference Clock
High	139.264 MHz, 155.52 MHz
Float	77.76MHz
Low	17.408MHz, 19.44MHz

The 78P2352-DB provides on-board 17.408MHz and 19.44MHz crystal oscillators as well as an SMA connector for use of external reference clock sources. Headers **JP6** and **JP7** allow easy selection of the reference clock source.

> **NOTE**: If using any system/timing interface other than the recommended Serial Plesiochronous mode, an external reference clock source must be provided at the SMA input labeled CKREF and must be synchronous to the transmit data (and timing) source.

LINE INTERFACE

The 78P2352-DB is pre-configured and shipped to allow easy evaluation of the CMI encoded, coaxial line interface.

Footprints for optics modules, however, are provided for evaluating the optical line interface of the 78P2352. For more information on configuring the D2352T8**C** board in optical (NRZ) mode, please contact TERIDIAN's applications support group.

TRANSMIT SIGNAL PATH

The transmitter's coaxial connectors are connected to the LIU transmitter pins (CMxP, CMxN) through a 1:1CT (center-tapped) transformer. The transformer center tap is tied to Vcc to bias the transmitter drivers. The signal path is differentially terminated with a 75Ω resistor on the LIU side of the transformer. The termination resistor, in combination with the characteristic impedance of the transformer and the line impedance create the required pulse shaping impedance for the LIU's driver.

The user may configure serial or parallel interface by changing **SW1** (pin 3), although Serial Plesiochronous mode is recommended to eliminate the need for a synchronous timing relationship between the transmit clock/data and the reference clock.

> When the parallel (system) interface is chosen, the 48-pin box connector U2 can be used to connect other digital control boards. By default the LIU expects transmit data to clock in on the rising clock edge so the transmitter source (i.e framer) should clock out transmit data on the clock's falling edge. If using this interface, the user must ensure the reference clock is synchronous with the transmit clock/data source.
>
> SMA connectors support the option for a serial (system) interface. Each channel provides four SMA connectors, two for the differential clock (SIxCKP/N) and two for the respective differential data signal (SIxDP/N). These inputs accept LVPECL differential signals, which are AC-coupled and differentially terminated with 100Ω at the LIU. If using any serial timing mode other than Plesiochronous mode, the user must ensure the reference clock is synchronous with the transmit clock/data source.

RECEIVE SIGNAL PATH

The line side (coax) receiver interface has the same architecture as the transmit interface, except the transformer winding's center tap is left open. The received signal is internally equalized for dispersive cable attenuation and decoded in the CMI to NRZ decoder.

The user may configure serial or parallel interface by changing **SW1** (pin 3), although Serial Plesiochronous mode is recommended.

If selecting the parallel interface, data to the system (i.e. framer) passes through the 48-pin box connector. The receive data is clocked out at the falling edge of the receive clock. This is the default state of the LIU.

SMA connectors support the option for a serial (system) interface. Each channel's serial interface provides four SMA connectors, two for the differential clock (SOxCKP/N) and two for the respective differential data signal (SOxDP/N). These outputs provide LVPECL differential signals, which are AC-coupled to the system at the SMA connectors.

SUPPLEMENTAL SURGE PROTECTION

Optional surge protection circuitry is included on the coax line side to ensure proper operation of the device during the presence of differential voltage surges, as called for by ITU-T, Bellcore, and IEC specifications. Protection diode U3 provides additional protection against ESD and power supply transients at the power supply banana jacks.

Consult the application note for more information on supplemental surge protection for electrical interfaces.

LOOPBACK OPERATION

S1 (pins 2 and 3) also provides controls for configuring the internal loopback modes.

When the pin is pulled low, the chip is in the normal mode.

When the pin is pulled high, the receiver uses the transmitter output signal as its input, known as local (analog) loopback.

When the pin is floating, the received signal is looped back to the transmitter, known as remote (digital) loopback.

DIFFERENTIAL TEST POINTS

The following test points are provided to facilitate test and measurement.

Test Point	Signal	Description
PDT1 PDT2	PWR	Power plane test points
PDT3	SI2CKP/N	Channel 2 transmit serial clock / data input
PDT4	SI2DP/N	
PDT5	SO2CKP/N	Channel 2 receive serial clock / data output
PDT6	SO2DP/N	
PDT7	SI1CKP/N	Channel 1 transmit serial clock / data input
PDT8	SI1DP/N	
PDT9	SO1CKP/N	Channel 1 receive serial clock / data output
PDT10	SO1DP/N	
PDT13 PDT16	RXxP/N	Receive serial CMI or LVPECL input
PDT14 PDT17	CMIxP/N	Transmit serial CMI data output
PDT15 PDT17	ECLxP/N	Transmit serial (NRZ) LVPECL data output

STATUS PINS

The 78P2352 provides both open drain and CMOS versions for the status pins. On the demo board, resistor population options are available to evaluate different version of chips. The demo boards are populated by open drain chips.

Open drain:

LOS1: R7 -- 0Ω, R96 -- 300Ω

LOS2: R39 -- 0Ω, R97 -- 300Ω

LOL1: R8 -- 0Ω, R98 -- 300Ω

LOL2: R38 -- 0Ω, R99 -- 300Ω

INTTX1B: R92 – 10KΩ, R42 -- 300Ω

INTTX2B: R94 – 10KΩ, R46 -- 300Ω

INTRX1B: R93 – 10KΩ, R43 -- 300Ω

INTRX2B: R95 – 10KΩ, R47 -- 300Ω

CMOS:

LOS1: R7 -- 300Ω, R96 – DNP

LOS2: R39 -- 300Ω, R97 – DNP

LOL1: R8 -- 300Ω, R98 – DNP

LOL2: R38 -- 300Ω, R99 – DNP

INTTX1B: R92 – DNP, R42 -- 300Ω

INTTX2B: R94 – DNP, R46 -- 300Ω

INTRX1B: R93 – DNP, R43 -- 300Ω

INTRX2B: R95 – DNP, R47 -- 300Ω

PCB DESIGN DESCRIPTION

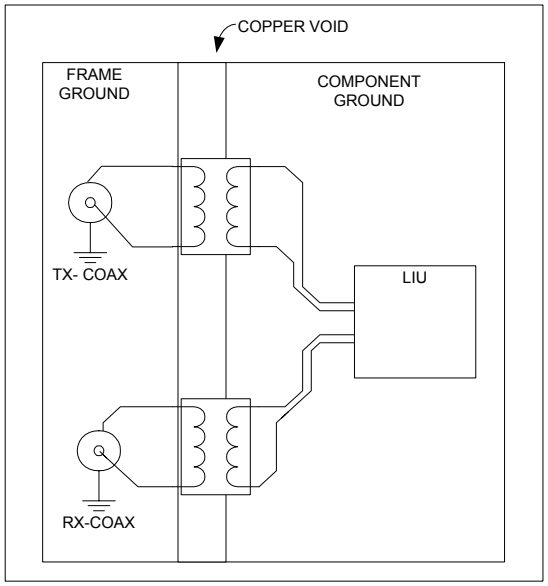
The 78P2352-DB (D2352T8**C**) demo board is constructed as a four-layer PC board. The top layer has the major components and signal routes. The bottom layer has bypass capacitors and mostly miscellaneous discrete components, as well as additional signal routes. The internal two layers have ground and power supply planes only. The power supply and ground pins of the 78P2352 LIU are connected directly to these planes.

The ground layer is directly under the component side of the board, followed by the power plane layer, then the bottom layer.

GROUND

The ground layer uses a split plane to divide system ground and frame (or chassis) ground. The frame ground plane is on the line side (the primary side of the transformer and the BNCs) and system digital ground is the LIU side (the secondary side of the transformer).

The chassis plane typically will be connected to the equipment chassis, which connects to the facilities Earth ground structure. The coax shield also typically connects to the chassis at equipment or patch panel bulkhead, providing a solid common bonding tie-point to the facility's grounding structure, as specified in the ITU-T recommendation K.27.



VCC PLANE

As with the digital ground plane, the power plane layer should only extends to the LIU side of the transformer. The outer edge of the power plane is kept 10 mils short of the ground plane's outer edge to avoid plane-to-plane current fringing at the plane edges.

DECOUPLING

Two decades of caps are used on the D2352T8**C** demo board, e.g. a mix of 0.1uF and 0.001uF. Consult the application note for general guidelines.

ANALOG TRACES

All CMI transmitter and receiver differential pair signal routes have a differential impedance of 75Ω to the secondary side of the transformer.

The line-side transmit pair (primary side of transformer), as well as the line side receive pair, is a 75Ω single-ended trace. The coax shield is connected directly to the line-side chassis ground.

TRANSFORMERS

The 78P2352-DB (D2352T8**C**) uses 1:1CT wide band transformers on transmit and receive. The following table lists the recommended transformers from different vendors that can be fitted on the 78P2352-DB demo board:

Dual core transformers

Manufacturer	***Part Number***
Halo	***TG04-TDK1N1***
TAMURA	***TTC-300***

See application note for transformer specifications and other recommended vendors and part numbers.

SAMPLE TEST RESULTS

Refer to Appendix A for sample test results.

SCHEMATICS

Refer to Appendix B for schematics and bill of material.

TEST SETUP

Refer to Appendix C for recommended test setups.

Appendix A: Sample Test Results

MASK MEASURMENTS

The following is a typical mask measurement for an STM-1e (CMI 0) pulse.

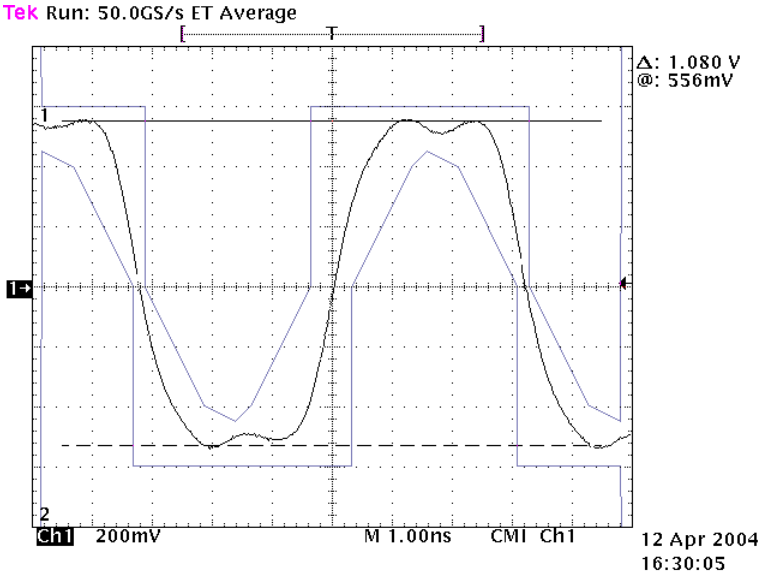


Figure A1: STM-1e pulse mask (CMI 0)

The following is a typical mask measurement for an STM-1e (CMI 1) pulse.

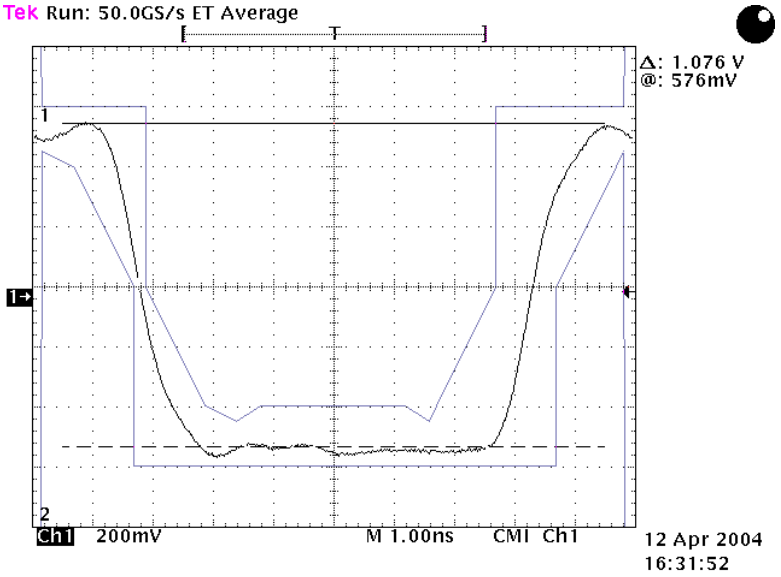


Figure A2: STM-1e pulse mask (CMI 1)

JITTER TOLERANCE: The following are typical STM-1 jitter tolerance measurements when tested in remote loopback (see Appendix C2).

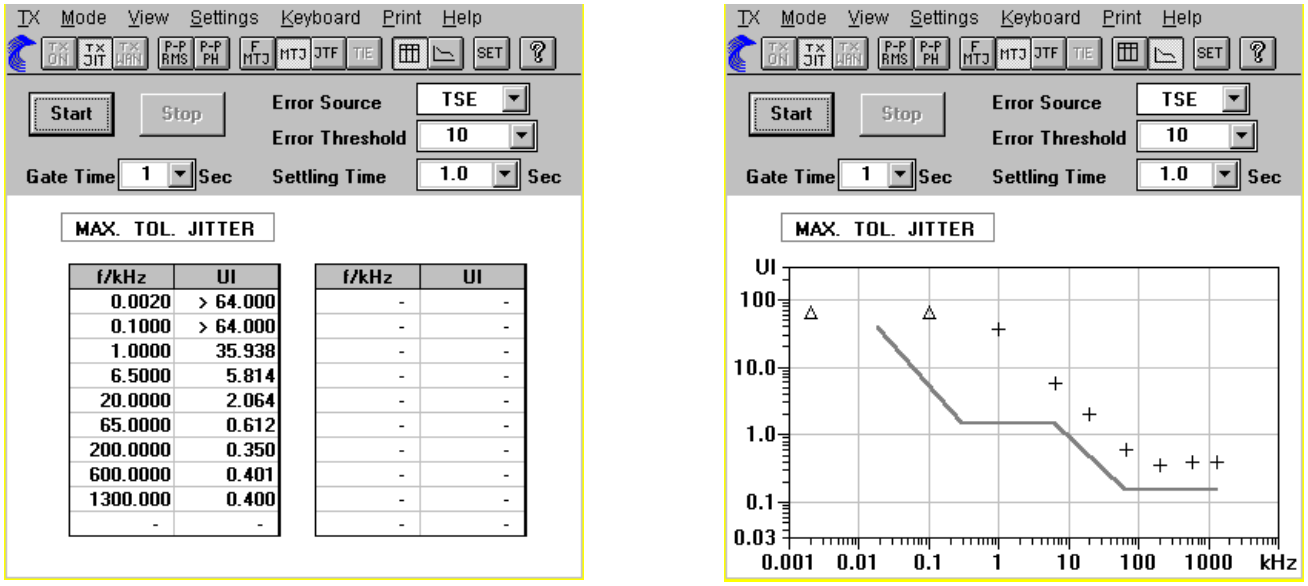


Figure A3: STM-1e jitter tolerance test result

JITTER TRANSFER FUNCTION: The following scope pics show the jitter transfer performance of the 78P2352. when tested in remote loopback (see Appendix C2).

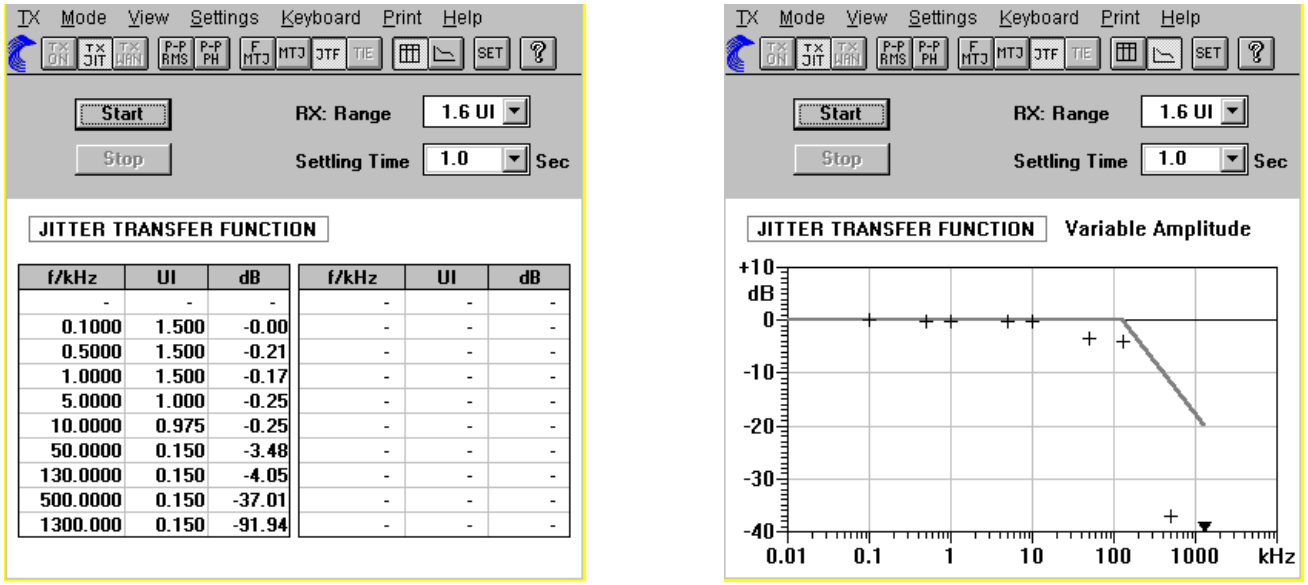
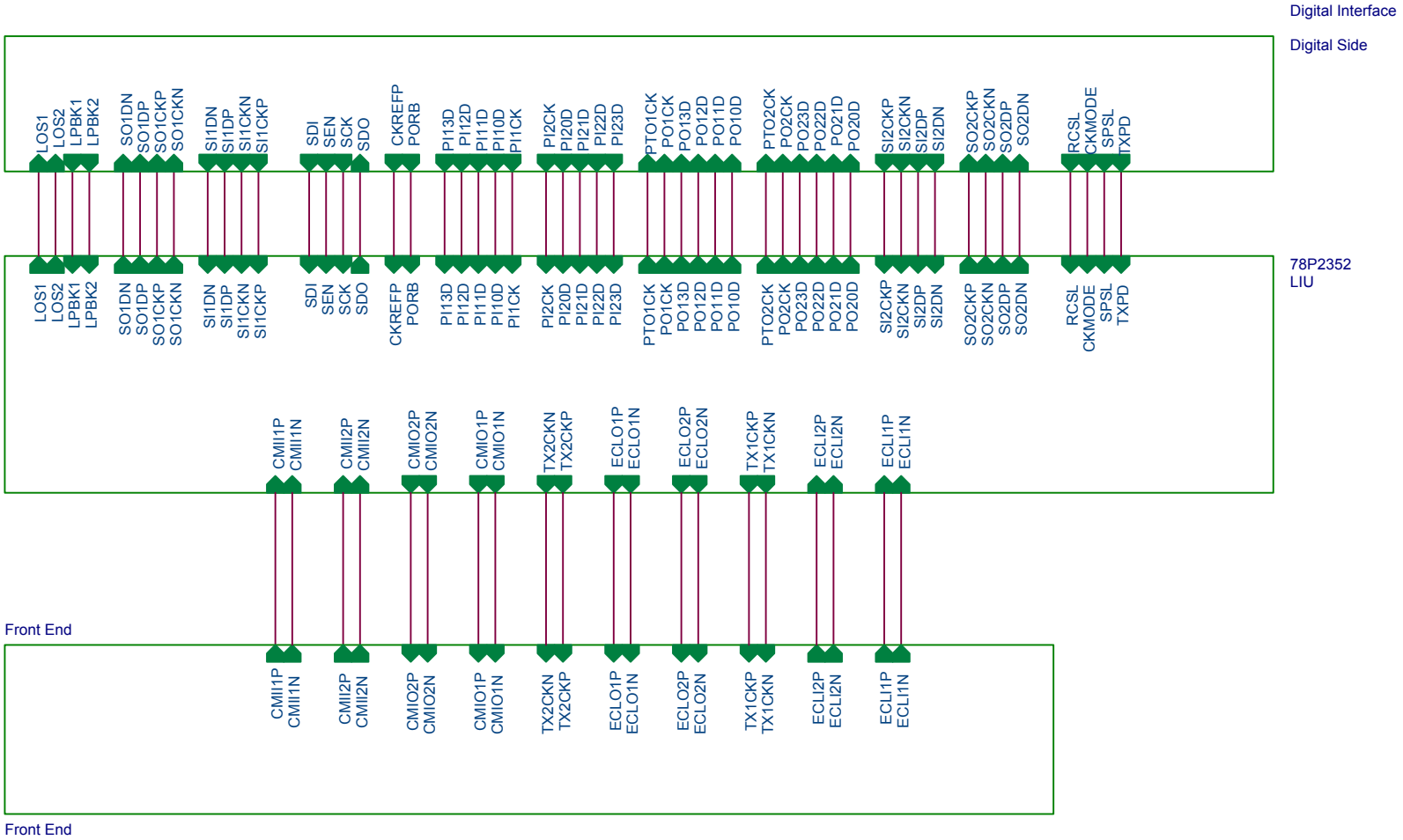
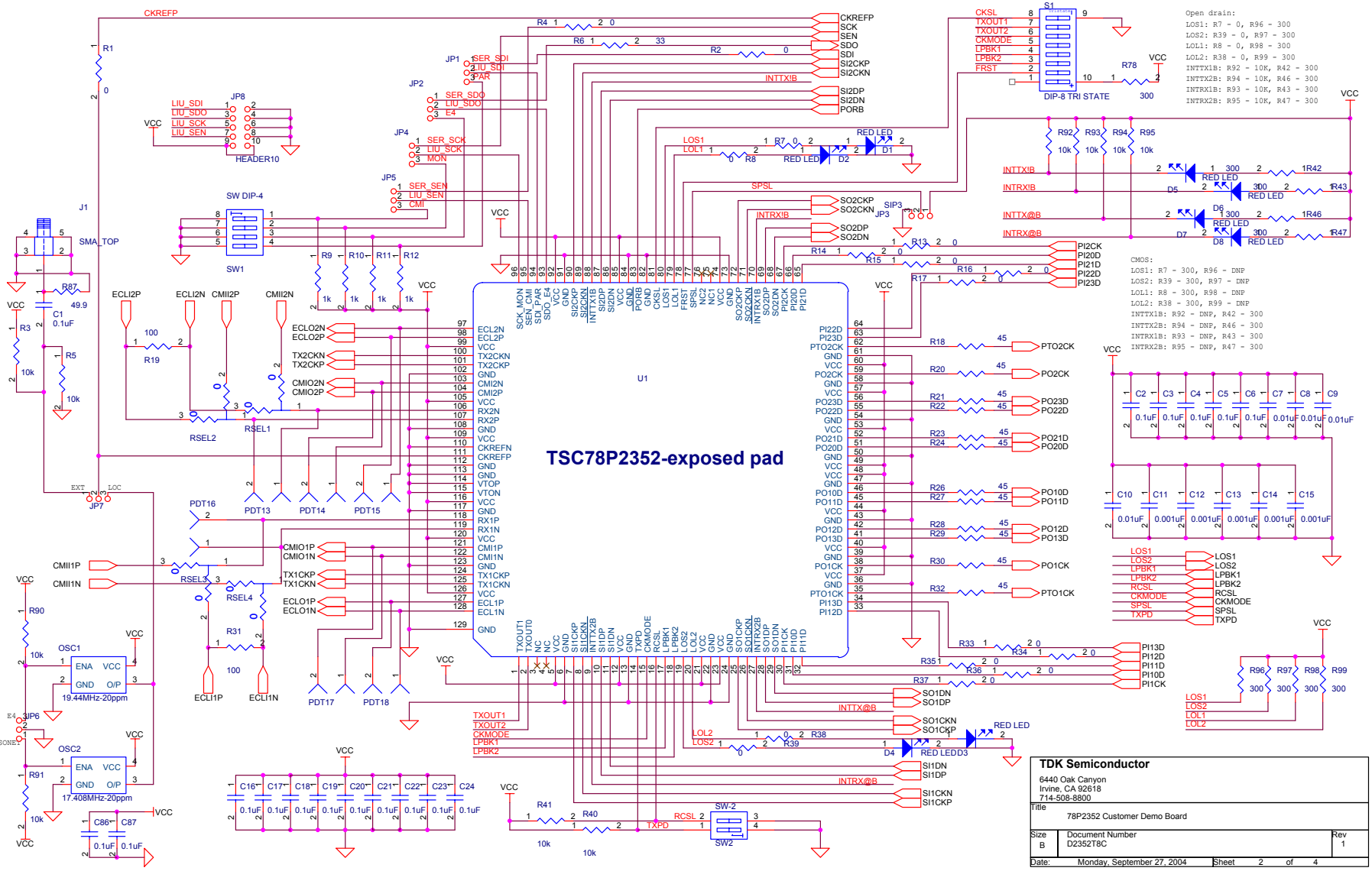


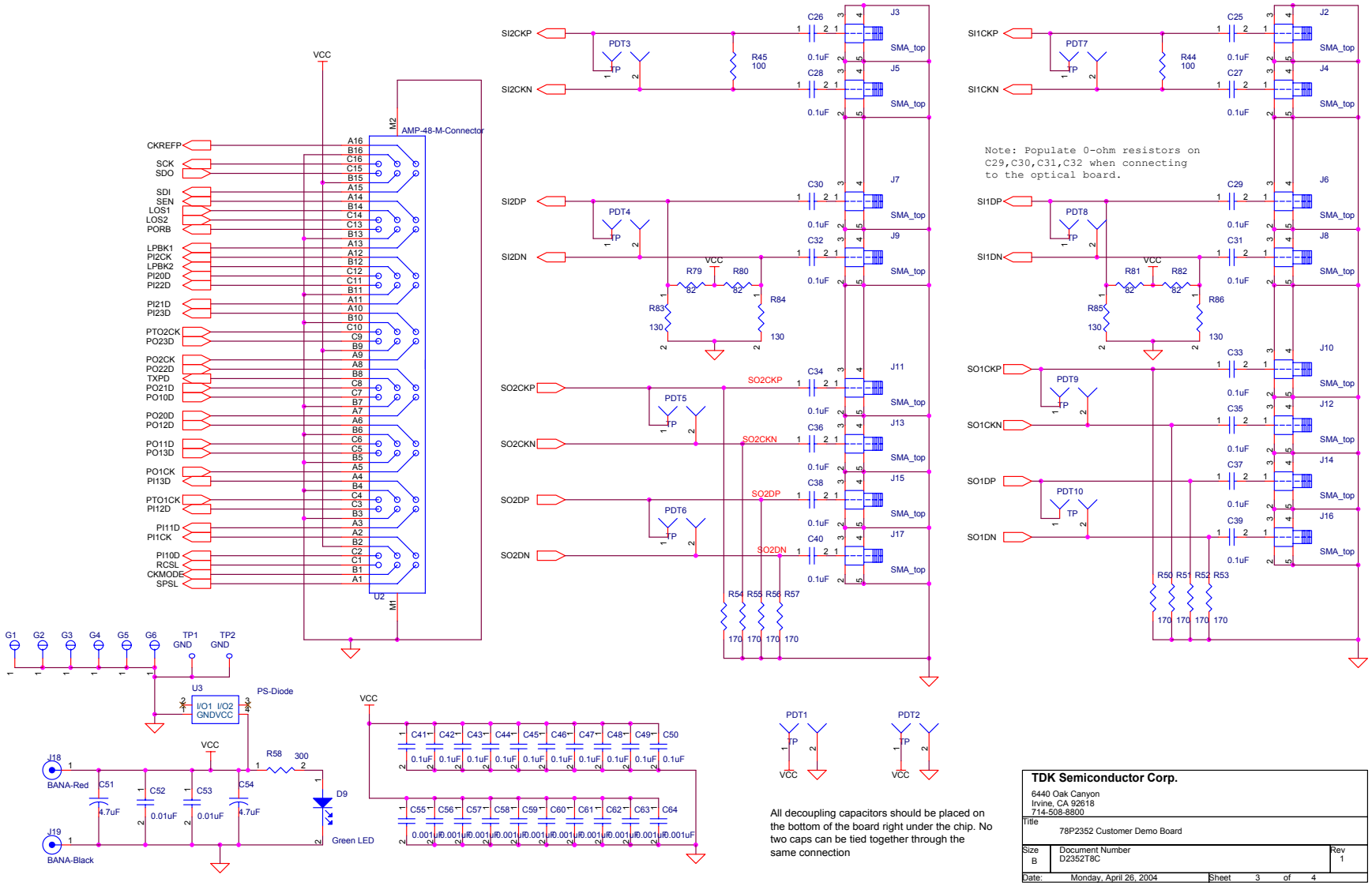
Figure A4: STM-1e jitter transfer test result

Appendix B: Schematics & Bill of Material



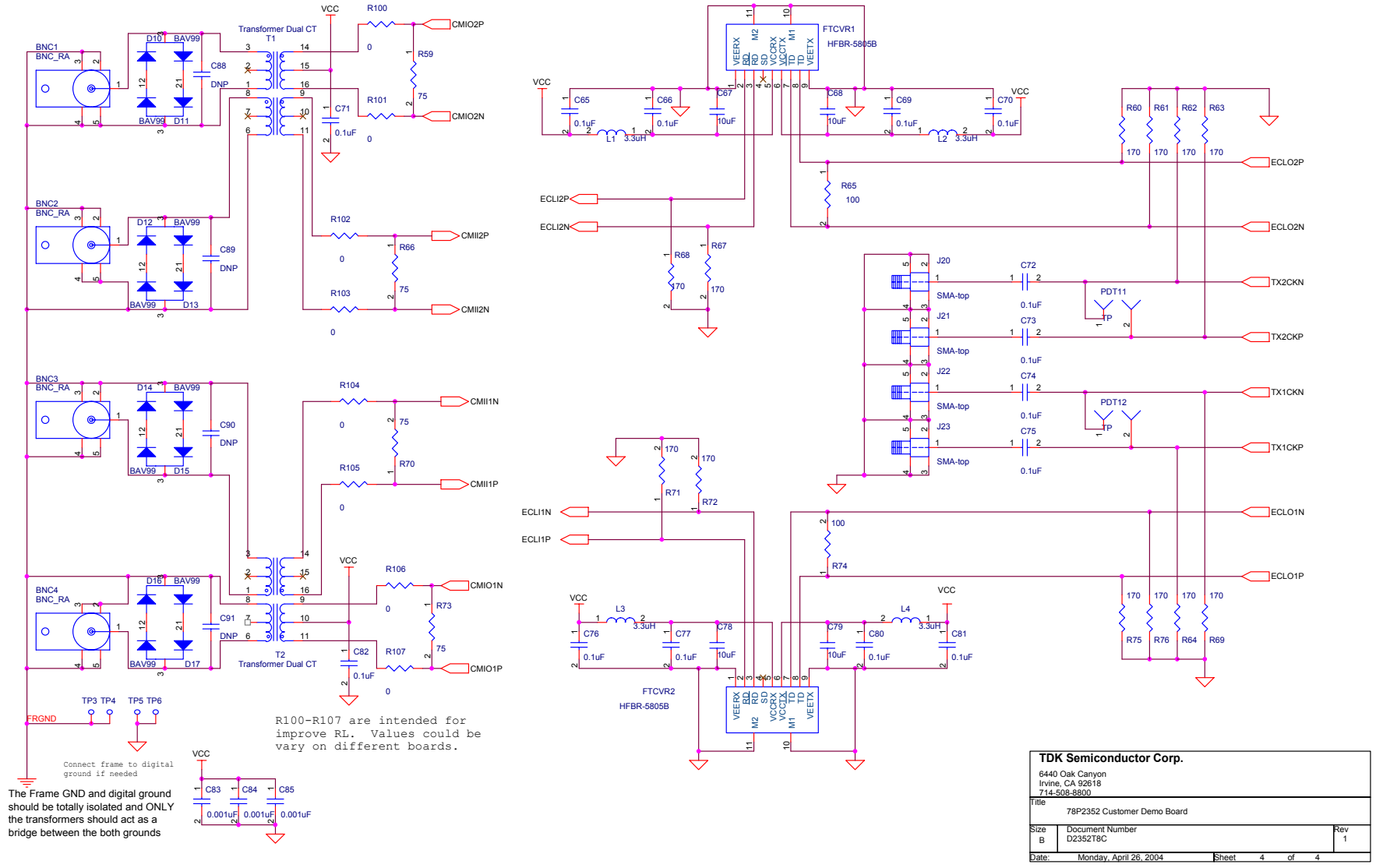
TDK Semiconductor Corp.		
6440 Oak Canyon Irvine, CA 92618 714-508-8800		
Title: 78P2352 Customer Demo Board		
Size: A	Document Number: D2352T8C	Rev: 1
Date: Monday, April 26, 2004	Sheet 1 of 4	


TSC78P2352-exposed pad
U1
J1
SMA_TOP
SW DIP-4
SW1
JP1
JP2
JP4
JP5
JP7
JP8
HEADER10
DIP-8 TRI STATE
S1
SW-2
OSC1
OSC2
19.44MHz-20ppm
17.408MHz-20ppm
CKREFP
CKREFN
SER_SDI
LIU_SDI
SER_SDO
LIU_SDO
SER_SCK
LIU_SCK
SER_SEN
LIU_SEN
MON
CMI
INTTXIB
INTRXIB
SPSL
LOS1
LOL1
RED LED
D1
D2
D3
D4
D5
D6
D7
D8
SIP3
JP3
RSEL1
RSEL2
RSEL3
RSEL4
PDT13
PDT14
PDT15
PDT16
PDT17
PDT18
ECLI1P
ECLI1N
ECLI2P
ECLI2N
CMII1P
CMII1N
CMII2P
CMII2N
ECLO1P
ECLO1N
ECLO2N
ECLO2P
CMIO1P
CMIO1N
CMIO2N
CMIO2P
TX1CKP
TX1CKN
TX2CKN
TX2CKP
PTO1CK
PTO2CK
PO1CK
PO2CK
PO10D
PO11D
PO12D
PO13D
PO20D
PO21D
PO22D
PO23D
PI1CK
PI2CK
PI10D
PI11D
PI12D
PI13D
PI20D
PI21D
PI22D
PI23D
SO1CKP
SO1CKN
SO1DP
SO1DN
SO2CKP
SO2CKN
SO2DP
SO2DN
SI1CKP
SI1CKN
SI1DP
SI1DN
SI2CKP
SI2CKN
SI2DP
SI2DN
CKSL
TXOUT1
TXOUT2
CKMODE
LPBK1
LPBK2
FRST
RCSL
TXPD
LOS2
CMOS:
LOS1: R7 - 300, R96 - DNP
LOS2: R39 - 300, R97 - DNP
LOL1: R8 - 300, R98 - DNP
LOL2: R38 - 300, R99 - DNP
INTTX1B: R92 - DNP, R42 - 300
INTTX2B: R94 - DNP, R46 - 300
INTRX1B: R93 - DNP, R43 - 300
INTRX2B: R95 - DNP, R47 - 300
Open drain:
LOS1: R7 - 0, R96 - 300
LOS2: R39 - 0, R97 - 300
LOL1: R8 - 0, R98 - 300
LOL2: R38 - 0, R99 - 300
INTTX1B: R92 - 10K, R42 - 300
INTTX2B: R94 - 10K, R46 - 300
INTRX1B: R93 - 10K, R43 - 300
INTRX2B: R95 - 10K, R47 - 300
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78P2352 Customer Demo Board
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Rev 1
Date: Monday, September 27, 2004
Sheet 2 of 4



All decoupling capacitors should be placed on the bottom of the board right under the chip. No two caps can be tied together through the same connection

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Date: Monday, April 26, 2004	Sheet 3 of 4	


Transformer Dual CT
T1
T2
Transformer Dual CT
FTCVR1
HFBR-5805B
FTCVR2
HFBR-5805B
R100-R107 are intended for improve RL. Values could be vary on different boards.
Connect frame to digital ground if needed
The Frame GND and digital ground should be totally isolated and ONLY the transformers should act as a bridge between the both grounds
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Document Number D2352T8C
Rev 1
Monday, April 26, 2004
Sheet 4 of 4

BILL OF MATERIAL

Item	Quantity	Reference	Part	PCB Footprint	Part Number	Vendor
1	4	BNC1, BNC2, BNC3, BNC4	BNC_RA	BNC_RT	A24611-ND/413558-1	DIGIKEY AMP
2	53	C1-C6, C16-C50, C65, C66, C69, C70, C71, C76, C77, C80, C81, C82, C86, C87	CAP., 0.1uF, 16V	C_0603	PCC2277CT-ND ECJ-1VB1E104K C1608X7R1E104k	DIGIKEY Panasonic TDK
3	6	C7, C8, C9, C10, C52, C53	CAP, 0.01uF, 50V	C_0603	399-1091-1-ND C0603C103K5RACTU C0603X5R0J103k	DIGIKEY Kemet TDK
4	18	C11, C12, C13, C14, C15, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C83, C84, C85	CAP, 0.001uF, 10V	C_0603	PCC1772CT-ND ECJ-1VB1H102K C1608X7R1H102k	DIGIKEY Panasonic TDK
5	2	C51, C54	CAP, 4.7uF, 10V	sacap	399-1587-1-ND T491A475K016AS	DIGIKEY Kemet
6	4	C67, C68, C78, C79	10uF	C_0805	Not installed	N/A
7	8	D1, D2, D3, D4, D5, D6, D7, D8	RED LED	ledsmd 0805	L62411CT-ND CMD17-21SRC	DIGIKEY Chicago Miniature Lamp
8	1	D9	Green LED	ledsmd 0805	L62505CT-ND CMD17-21VG	DIGIKEY Chicago Miniature Lamp
9	8	D10-D17	BAV99	SOT-23	BAV99INCT-ND BAV99E6327	DIGIKEY Infineon Technologies
10	6	G1, G2, G3, G4, G5, G6	MTHOLE	MTHOLE	1809k-ND H704-ND	DIGIKEY
11	7	JP1, JP2, JP3, JP4, JP5, JP6, JP7	SIP3	SIP\3P	S1011-03-ND PZC03SAAN	DIGIKEY Sullins Electronics Corp
12	1	J1	SMA_Top	SMA_Top	LTI-SASF54GT	Lighthorse Technologies
13	16	J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12,J13,J14, J15,J16,J17,J20,J21,J22,J23	SMA_Edge	SMA_Edge	J502-ND 142-0701-801	DIGIKEY Jonson Components
14	1	J18	BANA-Red	BAN	16BJ381 16BJ381	Mouser DGS Pro-Audio
15	1	J19	BANA-Black	BAN	16BJ382 16BJ382	Mouser DGS Pro-Audio
16	16	PDT1,PDT2,PDT3,PDT4,PDT5,PDT6,PDT7,PDT8, PDT9,PDT10,PDT11,PDT12, PDT13,PDT14,PDT15,PDT16, PDT17,PDT18	TP	sip\2p	S1011-02-ND PZC02SAAN	DIGIKEY Sullins Electronics Corp

Item	Quantity	Reference	Part	PCB Footprint	Part Number	Vendor
17	4	RSEL1,RSEL2, RSEL3,RSEL4	RES, 0, 5%	RSEL	P0.0GCT-ND ERJ-3GEY0R00V	DIGIKEY Panasonic
18	17	R1,R2,R4,R7,R8,R13,R14,R15,R16,R17,R33, R34,R35,R36,R37,R38,R39	RES, 0, 5%	R_0603	P0.0GCT-ND ERJ-3GEY0R00V	DIGIKEY Panasonic
19	8	R3,R5,R90-95	RES, 10k, 5%	R_0603	P10KGCT-ND ERJ-3GEYJ103V	DIGIKEY Panasonic
20	1	R6	RES, 33, 5%	R_0603	P33GCT-ND ERJ-3GEYJ330V	DIGIKEY Panasonic
21	10	R42,R43,R46,R47,R58,R78, R96-R99	RES, 300, 5%	R_0603	P300GCT-ND ERJ-3GEYJ301V	DIGIKEY Panasonic
22	4	R9,R10,R11,R12	RES, 1k, 1%	R_0603	P1.00KHCT-ND ERJ-EEKF1001V	DIGIKEY Panasonic
23	12	R18,R20,R21,R22,R23,R24,R26,R27,R28,R29,R30,R32	RES, 43, 5%	R_0603	P43GCT-ND ERJ-3GEYJ430V	DIGIKEY Panasonic
24	6	R19,R31,R44,R45, R65,R74	RES, 100, 1%	R_0603	P100HCT-ND ERJ-3EKF1000V	DIGIKEY Panasonic
25	2	R41,R40	RES, 10k, 5%	R_0805	P10KACT-ND ERJ-6GEYJ103V	DIGIKEY Panasonic
26	16	R50,R51,R52,R53,R54,R55,R56,R57,R60,R61,R62,R63, R64,R67,R68,R69,R71,R72,R75,R76	RES, 169, 1%	R_0603	P169HCT-ND ERJ-3EKF1690V	DIGIKEY Panasonic
27	4	R59,R66,R70,R73	RES, 75, 1%	R_0603	P75.0HCT-ND ERJ-3EKF75R0V	DIGIKEY Panasonic
28	4	R83,R84,R85,R86	RES, 130, 1%	R_0603	P130HCT-ND ERJ-3EKF1300V	DIGIKEY Panasonic
29	4	R79,R80,R81,R82	RES, 82, 1%	R_0603	311-82.0HCT-ND 9C06031A82R0FKHFT	DIGIKEY YAGEO
30	1	R87	RES, 49.9, 1%	R_0603	P49.9HCT-ND ERJ-3EKF49R9V	DIGIKEY Panasonic
31	1	SW1	SW DIP-4	DIP8	GH1004-ND 76SB04S	DIGIKEY Grayhill, Inc.
32	1	SW2	SW-2	DIP4	GH1002-ND 76SB02S	DIGIKEY Grayhill, Inc
33	1	S1	DIP-8 TRI STATE	DIP8_TRIS	138991 ETA-108E	Jameco ECE
34	2	T1,T2	TG04-TDK1N1	Dual CT	TG04-TDK1N1	HALO

Item	Quantity	Reference	Part	PCB Footprint	Part Number	Vendor
35	1	U1	78P2352	TQFP128	78P2352-IGT	TERIDIAN Semiconductor
36	1	OSC1	19.44MHz	SO4	ASV-19.44MHz-J	Abracon Corporation
37	1	OSC2	17.408MHz	SO4	ASV-17.408MHz-J	Abracon Corporation
38	1	TP1/TP2	Ground strip	TP-025SQ	C2118B-100-ND/ C2118	Digikey General cable
39	1	U3	DIODE	SOT-143	SR3.3	Semtech
40	1	U2	AMP-48 Female Connector	AMP-48R	650893-5-ND 650893-5	DIGIKEY AMP

Appendix C
Test Measurement Setups

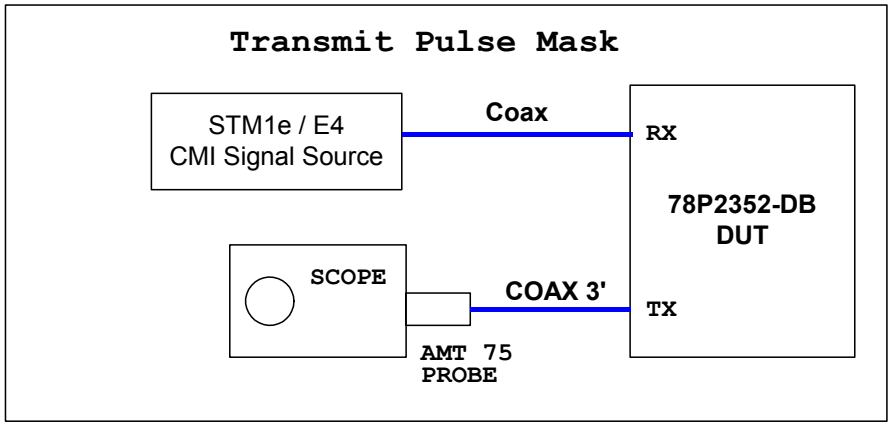


Figure C1. Notes:

- Signal source (i.e. Test Equipment) transmits CMI coded data to the demo board.
- The demo board is configured in remote loopback mode.
- A 50Ω to 75Ω adaptor (i.e. Tektronix AMT 75) is needed for 50Ω Scopes.

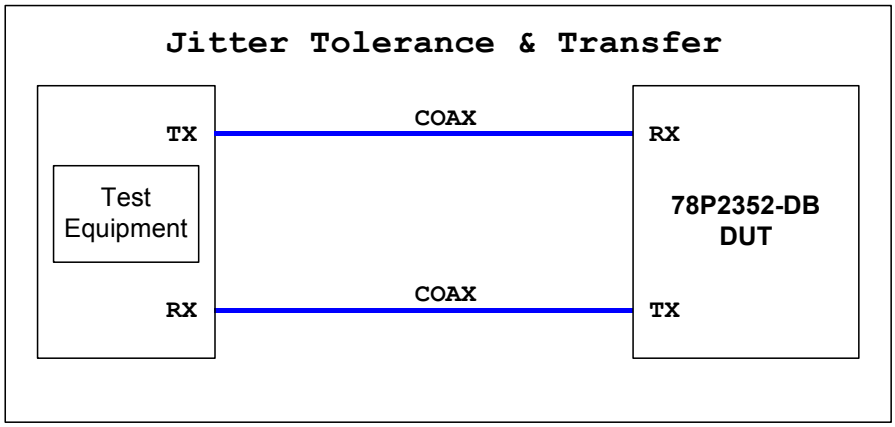


Figure C2. Notes:

- Test equipment transmits CMI coded data to the demo board.
- The demo board is configured in remote loopback mode.
- Run the Receive Jitter Tolerance and/or Jitter Transfer Function (JTF) tests on the Test Equipment.

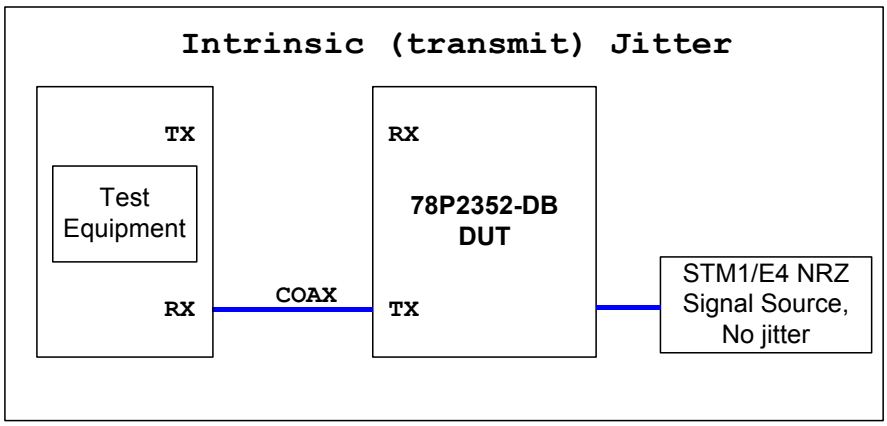


Figure C3. Notes:

- NRZ signal generator transmits data to the demo board via SMA LVPECL inputs.
- The demo board is in thru-mode (no loopbacks).
- Input signal should be free of jitter.

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