100 and 50 MHz, Programmable-Voltage Digital Waveform Generator/Analyzers

NI 655x

- 100 MHz maximum clock rate
- -2.0 to 5.5 V programmable voltage levels in 10 mV steps
- 20 channels with per-channel, per-cycle bidirectional control
- 1, 8, or 64 Mb/channel onboard memory
- Real-time hardware comparison of acquired data
- Complex triggering and pattern sequencing
- Interactive waveform and script editor software
- Synchronization and Memory Core (SMC) for tight synchronization with other SMC-based devices

Operating Systems

- Windows 2000/NT/XP
- LabVIEW Real-Time

Recommended Software

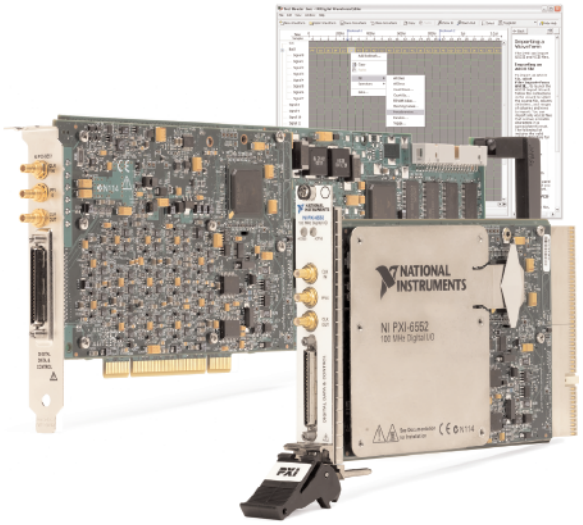
- LabVIEW
- LabWindows/CVI
- SignalExpress

Driver and Editing Software (included)

- NI-HSDIO driver
- Script Editor
- Digital Waveform Editor (included with 8 and 64 Mb/channel models)

Calibration

- NIST traceable
- 2-year external calibration cycle



Product	Platform	Channels	Maximum Clock Rate (MHz)	Voltage Levels	Memory (Mb/channel)	Scripting (Linking/Looping)	Programmable Data Delay	Per-Cycle Tristate	Hardware Comparison
NI 6552	PCI, PXI	20	100	Programmable, 10 mV steps	1, 8, or 64	✓	✓	✓	✓
NI 6551	PCI, PXI	20	50	Programmable, 10 mV steps	1, 8, or 64	✓	✓	✓	✓

Table 1. NI 655x Selection Guide

Overview

Applications
Semiconductor
Mixed-signal design validation and test
Interfacing to digital electronics
Aerospace/Defense
Subsystem emulation
Bit error rate tester (BERT)
Communications
Multimedia chipset emulation
Consumer Electronics
CMOS and CCD imaging sensors
Digital display tests

The National Instruments 6552 and 6551 are 100 and 50 MHz digital waveform generator/analyzers, respectively, for characterizing, validating, and testing digital electronics. These modules feature 20 channels with per-channel, per-cycle direction control and deep onboard memory with triggering and pattern sequencing. You can program the voltage levels on NI 655x devices with 10 mV resolution. You can use them with the NI Digital Waveform Editor, an interactive software tool for creating, editing, and importing digital waveforms. With the SMC, you can create mixed-signal test systems with digitizers, arbitrary waveform generators, and other digital waveform generator/analyzers, or you can synchronize multiple digital waveform devices to build high-channel-count test systems.

Design High-Performance Tests

For building high-performance stimulus-response systems, the NI 655x devices include:

- A sophisticated timing engine to adjust for the timing parameters of the device under test
- Programmable voltage levels for testing multiple devices or characterizing a single device under changing conditions
- Per-cycle tristate for bidirectional communication
- A versatile memory architecture for maximum flexibility of waveform and scripting memory

The hardware architecture is designed to preserve high signal quality, and an eye diagram of the PXI-6552 generation is shown in Figure 1. You can use the internal clock or an external clock, such as from the NI PXI-5404, through the front panel. You can also shift the data generated, data acquired, and exported sample clock relative to the onboard clock for clock frequencies above 25 MHz, which is critical to adjust for propagation delays and setup-and-hold times in the device under test.

Programmable voltage levels are needed when testing different devices or when characterizing how a given device performs under changing conditions. With NI 655x devices, the high and low levels for

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acquisition and generation can be set independently. You can program the voltage levels between -2.0 and 5.5 V with 10 mV resolution for TTL, LVTTL, LVCMOS, ECL, PECL, and other signal level compatibility.

The SMC memory architecture is designed for maximum flexibility between waveform memory and scripting memory, the instructions for pattern linking and looping. Using a single memory bank, you can allocate as much memory as needed for script and waveform data, giving you maximum flexibility from test to test.

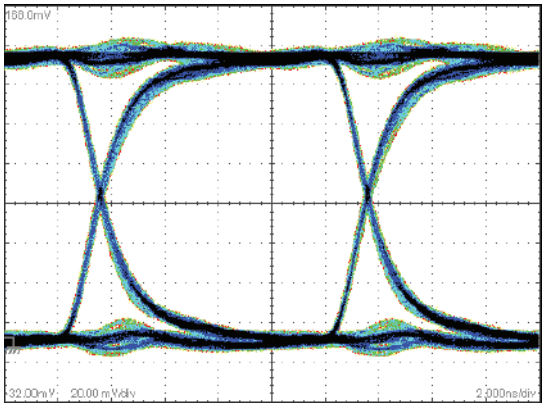


Figure 1. Eye Diagram of NI PXI-6552 Generation

Create Digital Waveforms Interactively with the Digital Waveform Editor

With the NI Digital Waveform Editor, an interactive software tool for creating and editing digital waveforms, you can import existing test patterns from popular spreadsheet and VHDL simulation packages in ASCII or value change dump (VCD) formats. Once imported, you can view the waveforms graphically and edit them interactively for new devices or new test conditions. You can also build new waveforms with built-in fill patterns such as pseudorandom bit sequences (PRBS) and count up/down patterns. When ready to test your device, the waveforms import seamlessly into NI LabVIEW, SignalExpress, and C. The Digital Waveform Editor is included with the 8 and 64 Mb/channel memory models, and is a separate add-on for use with the 1 Mb/channel model.

Build Tightly Synchronized Mixed-Signal Test Systems

NI 655x devices use the same SMC architecture as the NI 5122 high-resolution digitizers and NI 5441 arbitrary waveform generators, so you can combine these devices to build tightly synchronized mixed-signal prototyping and test systems. For tight timing requirements, these PXI modules phase-lock to the 10 MHz reference clock on the PXI backplane. If you have an external precision reference, you can import it through the front panel SMB connector.

Driver Software

NI 655x devices include the NI-HSDIO driver with an intuitive, powerful API based on IVI guidelines. The Windows-compatible NI-HSDIO driver provides an API for LabVIEW, SignalExpress, LabWindows/CVI, and other text-based development environments.

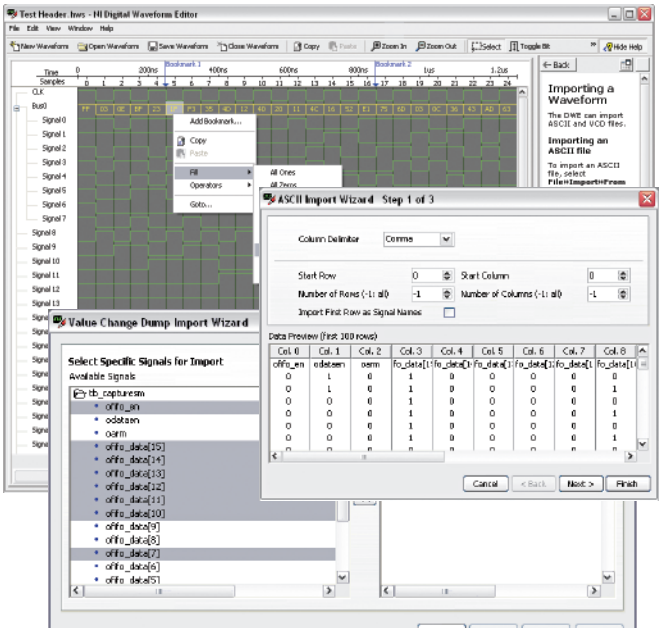


Figure 2. Digital Waveform Editor with ASCII and VCD Import Wizards

Ordering Information

NI PCI-6551 .....778950-0M[1]
NI PCI-6552 .....778951-0M[1]
NI PXI-6551 .....778538-0M[1]
NI PXI-6552 .....778539-0M[1]

[1]Where M is: 1 (1 Mb/channel), 2 (8 Mb/channel), or 3 (64 Mb/channel)

Includes NI 655x device and NI-HSDIO driver. The 8 and 64 Mb/channel models also include the Digital Waveform Editor.

Software

NI Digital Waveform Editor 778724-03

Cable

SHC68-C68-D2 188142-01
SHC68-HIX38 .....192681-1R5

Accessories

CB-2162 778592-01
SMB-2163.....778749-01

BUY NOW!

For complete product specifications, pricing, and accessory information, call (800) 813 3693 (U.S. only) or go to **ni.com**.

Specifications

These specifications are valid for the following temperature ranges: PXI: 0 to 55 °C, PCI: 0 to 45 °C.

Channel Characteristics

Number of data channels 20
Direction control of data channels ..... Per-channel, per-cycle

Generation Signal Characteristics (data, DDC ClkOut, and PFI <0..3> channels)

All voltage ranges specified into 1 MΩ
Generation voltage range ..... -2.0 to 5.5 V
Generation signal type ..... Single-ended
Number of programmable voltage levels ..... 1 voltage low level and 1 voltage high level applies to all data, Clk Out (sample clock only), and PFI channels
Generation voltage range restrictions ..... -0.5 to 5.5 V (up to 50 MHz clock rate)
-2 to 3.7 V (up to 50 MHz clock rate)
-0.5 to 3.7 V (50 to 100 MHz clock rate; NI 6552 only)
Generation voltage swing ..... 400 mV to 6 V (up to 50 MHz clock rate)
400 mV to 4.2 V (50 to 100 MHz clock rate; NI 6552 only)
Generation voltage-level resolution ..... 10 mV
DC generation voltage-level accuracy ..... ±20 mV (excluding system crosstalk)
Output impedance ..... 50 Ω nominal at 25 °C
Maximum DC drive strength ..... ±50 mA maximum per channel
±600 mA maximum for all data, clock, and PFI channels
Channel power-up state ..... Drivers disabled, 10 kΩ input impedance

Acquisition Signal Characteristics (data, strobe, and PFI <0..3> channels)

Acquisition voltage range ..... -2.0 V to 5.5 V
Number of programmable acquisition thresholds ..... 1 voltage low threshold and a strobe voltage high threshold applies to all data and PFI channels
Minimum detectable voltage swing ..... 50 mV
Acquisition voltage threshold resolution ..... 10 mV
DC acquisition voltage threshold accuracy ..... ±30 mV (excluding system crosstalk)
Input impedance ..... 50 Ω or 10 kΩ (default), software-selectable per channel; applies when powered on and within valid voltage range

Timing Characteristics

Sample Clock

Sample clock sources ..... 1. Onboard clock (internal VCXO with divider)
2. CLK IN (SMB jack connector)
3. PXI_STAR (PXI backplane; PXI only)
4. STROBE (DDC Connector) – Acquisition only
Onboard clock frequency range ..... NI 6551: 48 Hz to 50 MHz. (settable to 200 MHz/N; $4 \leq N \leq 4{,}194{,}304$)
NI 6552: 48 Hz to 100 MHz (settable to 200 MHz/N; $2 \leq N \leq 4{,}194{,}304$)
Exported sample clock delay range ..... 0 to 1 sample clock periods for clock frequencies ≥25 MHz
Exported sample clock delay resolution ..... 1/256 of sample clock period for clock frequencies ≥25 MHz

Exported Sample Clock Jitter (typical using onboard clock)

Period jitter	Cycle-to-cycle jitter
20 ps (rms)	35 ps (rms)

Generation Signal Characteristics (data, DDC Clk Out, and PFI <0..3> channels)

Data channel-to-channel skew	±300 ps (typical across all data channels) ±900 ps (maximum across all data channels)
Maximum data channel toggle rate	NI 6551: 25 MHz; NI 6552: 50 MHz
Data formats	NRZ
Data position modes	Rising edge, falling edge, delayed relative to sample clock
Generation data delay range	0 to 1 sample clock period for clock frequencies ≥25 MHz
Generation data delay resolution	1/256 of sample clock period for clock frequencies ≥25 MHz

Acquisition Signal Characteristics (data, strobe, and PFI <0..3> channels)

Channel-to-channel skew	±400 ps (typical across all data channels) ±900 ps (maximum across all data channels)
Minimum detectable pulse width	4 ns (required at both acquisition voltage thresholds)
Acquisition timing delay range	0 to 1 sample clock periods for clock frequencies ≥25 MHz
Acquisition timing delay resolution	1/256 of sample clock period for clock frequencies ≥25 MHz

Waveform Characteristics

Memory and Scripting

Onboard memory size (assumes no scripting instructions)	1 Mb/channel (for generation sessions)	8 Mb/channel (for generation sessions)	64 Mb/channel (for generation sessions)
	1 Mb/channel (for acquisition sessions)	8 Mb/channel (for acquisition sessions)	64 Mb/channel (for acquisition sessions)

Generation Modes

Waveform: Generate a single waveform once, N times, or continuously.
Scripted: Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to script triggers.

Triggers (inputs to the NI 655x)

Trigger types	Start Trigger, Pause Trigger, Script Trigger <0..3> (generation sessions only) Reference Trigger (acquisition sessions only) Multirecord Advance Trigger (acquisition sessions only)
Sources	1. PFI <0> (SMB jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane, PXI only), RTSI <0..7> (PCI only) 4. PXI_STAR (PXI backplane, PXI only) 5. Pattern match (acquisition sessions only) 6. Software (user function call) 7. Disabled (do not wait for a trigger)
Trigger detection	1. Start Trigger (edge detection: rising or falling) 2. Pause Trigger (level detection: high or low) 3. Script Trigger <0..3> (edge detection: rising or falling, Level detection: high or low) 4. Reference Triggers (edge detection: rising or falling) 5. Advance Trigger (edge detection)
Minimum required trigger pulse width	30 ns
Destinations	1. PFI 0 (SMB jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG <0..7> (PXI backplane, PXI only), RTSI <0..7> (PCI only) Each of the triggers can be routed to any of the 13 destinations except the pause trigger cannot be exported.

Events (outputs from the NI 655x)

Event types ..... Marker <0..3>, Data Active event, Ready for Start event

Destinations ..... 1. PFI 0 (SMB jack connectors)
2. PFI <1..3> (DDC connector)
3. PXI_TRIG <0..7> (PXI backplane)
Each of the events can be routed to any of the destinations with the exception of the Data Active event. The Data Active event can only be routed to the PFI channels.

Miscellaneous

Interval for external calibration ..... 2 years

Onboard Clock Characteristics (only valid when PLL reference source is set to "None")

Frequency accuracy ..... ±100 ppm (typical)

Temperature stability ..... ±30 ppm (typical)

Aging ..... ±5 ppm first year (typical)

Power Requirements

Typical ..... 21.6 W

Maximum ..... PXI: 26.5 W; PCI: 27 W

Physical

Dimensions ..... PXI: Single 3U CompactPCI Slot. PXI Compatible
PCI: 12.6 by 35.5 cm (4.95 by 13.9 in.)

Environment

I/O Panel Connectors Label	External Function(s)	Connector Type
CLK IN	Sample Clock, External PLL Reference Input	SMB jack
PFI 0	Events, Triggers	SMB jack
CLK OUT	Exported Sample Clock, Exported Reference Clock	SMB jack
Digital Data and Control (DDC)	Digital Data Channels, Exported Sample Clock, STROBE, Events, Triggers	68-pin VHDCI

Operating temperature ..... PXI: 0 to 55 °C in all NI PXI chassis except the following. 0 to 45 °C when installed in an NI PXI-1000/B and PXI-101x chassis (meets IEC-60068-2-1 and IEC-60068-2-2).
PCI: 0 to 45 °C

Storage temperature ..... -20 to 70 °C

Relative humidity ..... 10 to 90% relative humidity, noncondensing (meets IEC-60068-2-56)

Storage relative humidity ..... 5 to 95% relative humidity, noncondensing (meets IEC-60068-2-56)

Certifications and Compliance

Safety

NI 655x devices meet the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use: IEC 61010-1, EN 61010-1, UL 61010B-1, CAN/CSA C22.2 No. 61010-1

EMC ..... Emissions: EN 55011 Class A at 10 m. FCC Part 15A above 1 GHz Immunity: EN 61326:1997 + A2:2001, Table 1, CE, C-Tick, and FCC Part 15 (Class A) Compliant

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