# 74LVC1G07-Q100

## Buffer with open-drain output

Rev. 1 — 23 May 2013 Product data sheet

## 1. General description

The 74LVC1G07-Q100 provides the non-inverting buffer.

The output of this device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- −24 mA output drive ($V_{CC}$ = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC1G07GW-Q100 | –40 °C to +125 °C | TSSOP5 | plastic thin shrink small outline package; 5 leads; body width 1.25 mm | SOT353-1 |
| 74LVC1G07GV-Q100 | –40 °C to +125 °C | SC-74A | plastic surface-mounted package; 5 leads | SOT753 |

## 4. Marking

**Table 2. Marking**

| Type number | Marking code[1] |
|---|---|
| 74LVC1G07GW-Q100 | VS |
| 74LVC1G07GV-Q100 | V07 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram

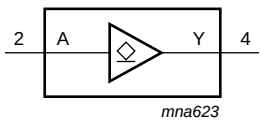



**Fig 1. Logic symbol**




**Fig 2. IEC logic symbol**

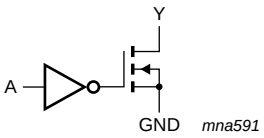



**Fig 3. Logic diagram**

## 6. Pinning information

### 6.1 Pinning

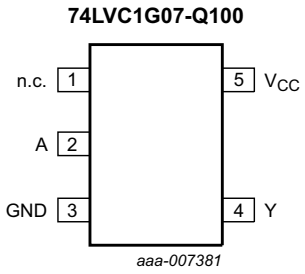



**Fig 4. Pin configuration SOT353-1 and SOT753**


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### 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| n.c. | 1 | not connected |
| A | 2 | data input |
| GND | 3 | ground (0 V) |
| Y | 4 | data output |
| $V_{CC}$ | 5 | supply voltage |

## 7. Functional description

**Table 4. Function table[1]**

| Input A | Output Y |
|---|---|
| L | L |
| H | Z |

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | –50 | - | mA |
| $V_I$ | input voltage | | [1] | –0.5 | +6.5 | V |
| $I_{OK}$ | output clamping current | $V_O < 0$ V | | –50 | - | mA |
| $V_O$ | output voltage | Active mode | [1] | –0.5 | +6.5 | V |
| | | Power-down mode | [1][2] | –0.5 | +6.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to 6.5 V | | - | 50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |
| $I_{GND}$ | ground current | | | –100 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –40 °C to +125 °C | [3] | - | 250 | mW |

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC}$ = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP5 and SC-74A packages: above 87.5 °C the value of $P_{tot}$ derates linearly with 4.0 mW/K.


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## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | - | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | Active mode | 0 | - | 5.5 | V |
| | | Power-down mode; $V_{CC}$ = 0 V | 0 | - | 5.5 | V |
| $T_{amb}$ | ambient temperature | | −40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 1.65 V to 2.7 V | - | - | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 5.5 V | - | - | 10 | ns/V |

## 10. Static characteristics

**Table 7. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65$V_{CC}$ | - | - | 0.65$V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.7$V_{CC}$ | - | - | 0.7$V_{CC}$ | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | - | - | 0.35$V_{CC}$ | - | 0.35$V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.3$V_{CC}$ | - | 0.3$V_{CC}$ | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = 100 μA; $V_{CC}$ = 1.65 V to 5.5 V | - | - | 0.10 | - | 0.10 | V |
| | | $I_O$ = 4 mA; $V_{CC}$ = 1.65 V | - | - | 0.45 | - | 0.70 | V |
| | | $I_O$ = 8 mA; $V_{CC}$ = 2.3 V | - | - | 0.30 | - | 0.45 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | - | 0.40 | - | 0.60 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | - | 0.55 | - | 0.80 | V |
| | | $I_O$ = 32 mA; $V_{CC}$ = 4.5 V | - | - | 0.55 | - | 0.80 | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V [2] | - | ±0.1 | ±5 | - | ±100 | μA |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = $V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | ±0.1 | ±10 | - | ±100 | μA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 5.5 V; $V_{CC}$ = 0 V | - | ±0.1 | ±10 | - | ±200 | μA |


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**Table 7. Static characteristics** *...continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $I_{CC}$ | supply current | $V_I$ = 5.5 V or GND; $I_O$ = 0 A; $V_{CC}$ = 1.65 V to 5.5 V | - | 0.1 | 10 | - | 200 | μA |
| $\Delta I_{CC}$ | additional supply current | per pin; $V_I = V_{CC} - 0.6$ V; $I_O$ = 0 A; $V_{CC}$ = 2.3 V to 5.5 V [2] | - | 5 | 500 | - | 5000 | μA |
| $C_I$ | input capacitance | $V_{CC}$ = 3.3 V; $V_I$ = GND to $V_{CC}$ | - | 5.0 | - | - | - | pF |

[1] All typical values are measured at $T_{amb}$ = 25 °C.

[2] These typical values are measured at $V_{CC}$ = 3.3 V.

# 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for load circuit see Figure 6.*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | A to Y; see Figure 5 [2] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.0 | 2.6 | 6.7 | 1.0 | 8.4 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0.5 | 1.7 | 5.5 | 0.5 | 7.0 | ns |
| | | $V_{CC}$ = 2.7 V | 0.5 | 2.3 | 4.7 | 0.5 | 6.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0.5 | 2.2 | 4.2 | 0.5 | 5.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.5 | 1.6 | 3.5 | 0.5 | 4.5 | ns |
| $C_{PD}$ | power dissipation capacitance | $V_I$ = GND to $V_{CC}$; $V_{CC}$ = 3.3 V [3] | - | 7.0 | - | - | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

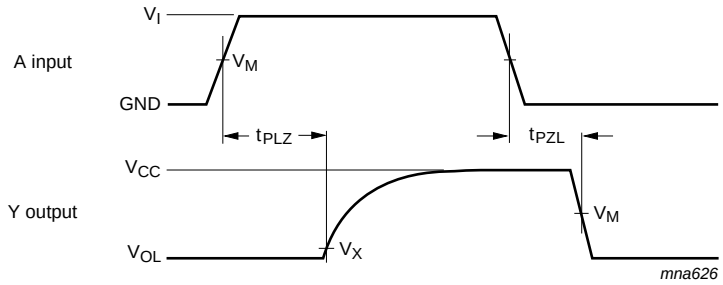
[2] $t_{pd}$ is the same as $t_{PLZ}$ and $t_{PZL}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.


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## 12. Waveforms




Measurement points are given in Table 9.

$V_{OL}$ is the typical output voltage level that occurs with the output load.

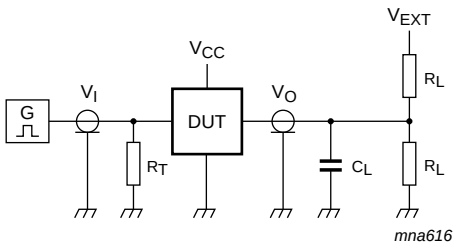
**Fig 5. The input (A) to output (Y) propagation delays**

**Table 9. Measurement points**

| Supply voltage | Input | Output | |
|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ | $V_X$ |
| 1.65 V to 1.95 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.15 V |
| 2.3 V to 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.15 V |
| 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V |
| 4.5 V to 5.5 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.3 V |


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Test data is given in Table 10.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

**Fig 6. Test circuit for measuring switching times**

**Table 10. Test data**

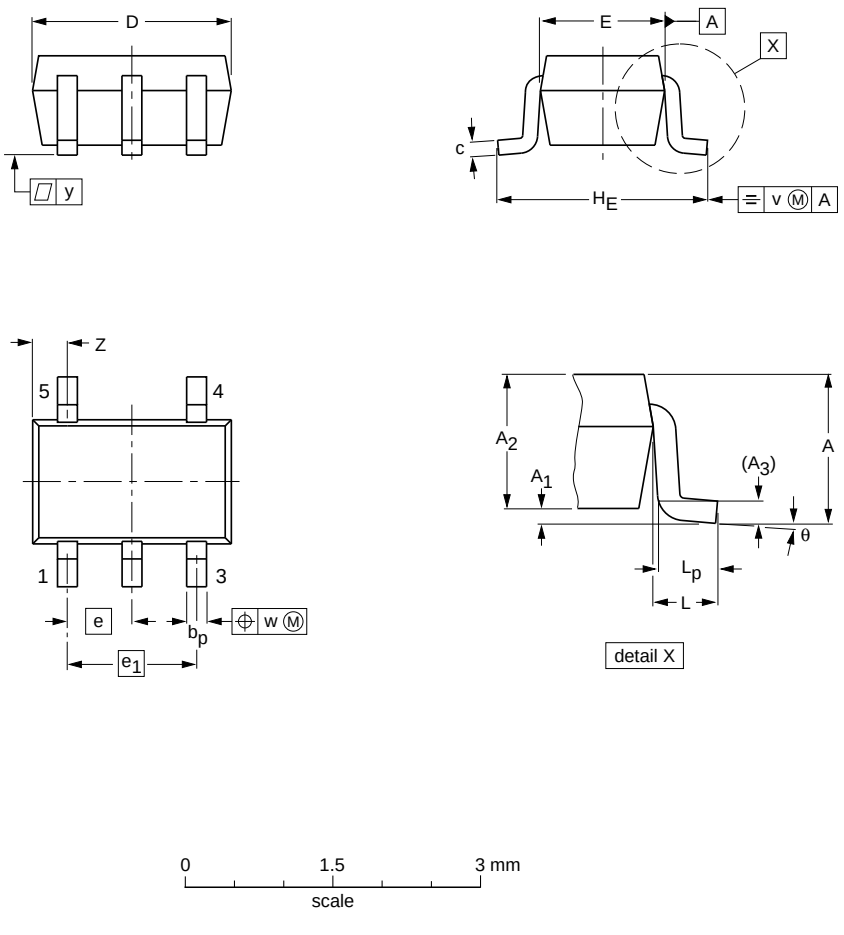
| Supply voltage | Input | | Load | | $V_{EXT}$ |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PZL}$, $t_{PLZ}$ |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 1 kΩ | $2V_{CC}$ |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 500 Ω | $2V_{CC}$ |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | 6 V |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | 6 V |
| 4.5 V to 5.5 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω | $2V_{CC}$ |


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## 13. Package outline

**TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm** **SOT353-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $e_1$ | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.1<br>0 | 1.0<br>0.8 | 0.15 | 0.30<br>0.15 | 0.25<br>0.08 | 2.25<br>1.85 | 1.35<br>1.15 | 0.65 | 1.3 | 2.25<br>2.0 | 0.425 | 0.46<br>0.21 | 0.3 | 0.1 | 0.1 | 0.60<br>0.15 | 7°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

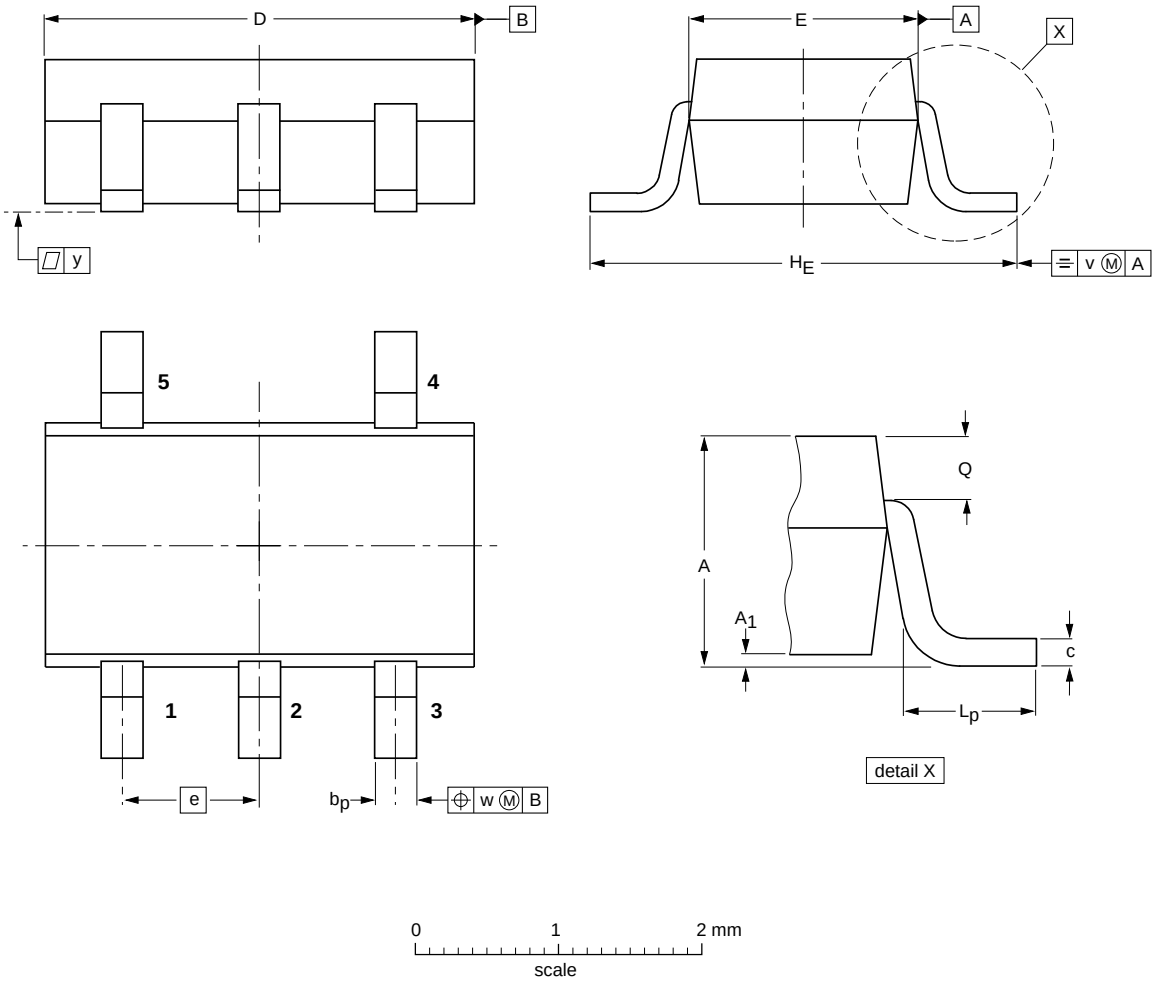
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT353-1 | | MO-203 | SC-88A | | | ~~00-09-01~~<br>03-02-19 |

**Fig 7. Package outline SOT353-1 (TSSOP5)**


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**Plastic surface-mounted package; 5 leads** **SOT753**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | c | D | E | e | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.100<br>0.013 | 0.40<br>0.25 | 0.26<br>0.10 | 3.1<br>2.7 | 1.7<br>1.3 | 0.95 | 3.0<br>2.5 | 0.6<br>0.2 | 0.33<br>0.23 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT753 | | | SC-74A | | | ~~02-04-16~~<br>06-03-16 |

**Fig 8. Package outline SOT753 (SC-74A)**


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## 14. Abbreviations

**Table 11. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MIL | Military |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 15. Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC1G07_Q100 v.1 | 20130523 | Product data sheet | - | - |


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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 18. Contents


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