DATA SHEET

74LV132
Quad 2-input NAND Schmitt-trigger

Product specification
Supersedes data of 1997 Feb 04
IC24 Data Handbook

1998 Apr 28

Philips
Semiconductors



PHILIPS

Quad 2-input NAND Schmitt-trigger 74LV132

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) $< 0.8V$ @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) $> 2V$ @ V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

DESCRIPTION

The 74LV132 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT132.

The 74LV132 contains four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 15pF V_{CC} = 3.3V	10	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	24	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV132 N	74LV132 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV132 D	74LV132 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV132 DB	74LV132 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV132 PW	74LV132PW DH	SOT402-1

PIN DESCRIPTION

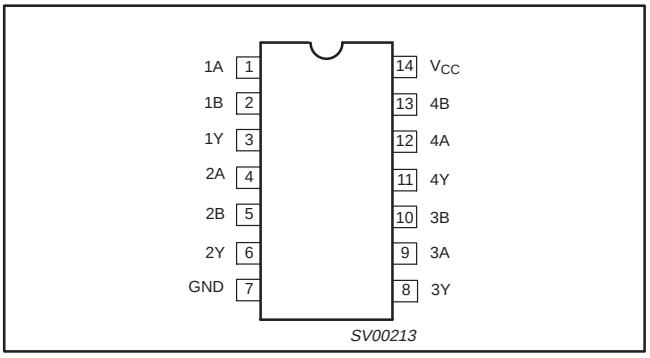
PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

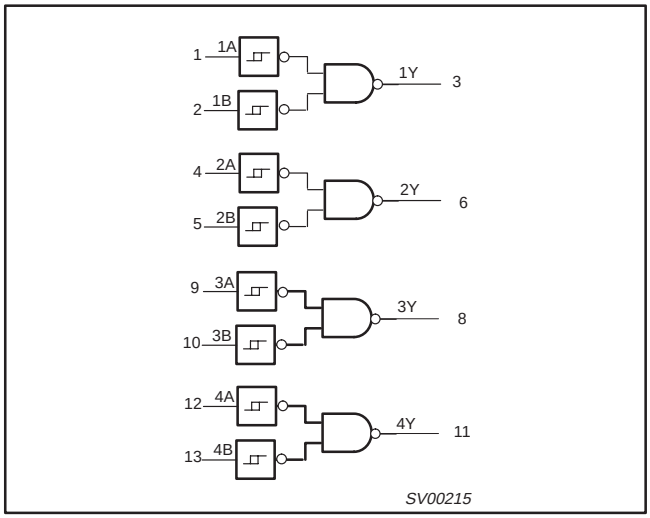
INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level

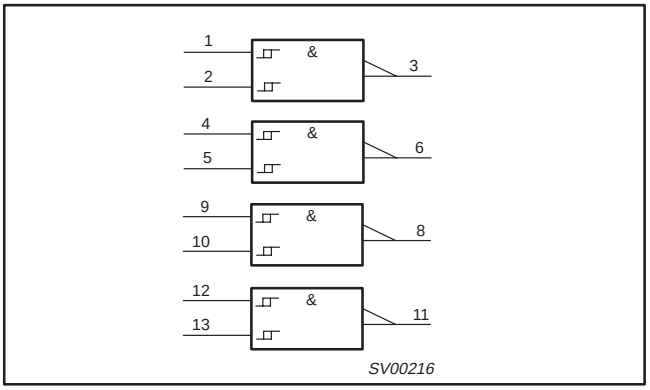
PIN CONFIGURATION



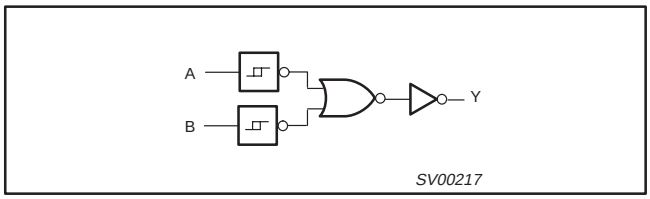
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < –0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < –0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$–0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	$0.7*V_{CC}$			$0.7*V_{CC}$		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			$0.3*V_{CC}$		$0.3*V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	

DC CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ – 0.6V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

TRANSFER CHARACTERISTICS

Voltages are referenced to GND = 0V.

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85°C			–40 to +125°C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
V_{T+}	Positive going threshold	Figures 1 and 2	1.2	–	0.70	–	–		V
			2.0	0.8	1.10	1.4	0.8	1.4	
			2.7	1.0	1.45	2.0	1.0	2.0	
			3.0	1.2	1.60	2.2	1.2	2.2	
			3.6	1.5	1.95	2.4	1.5	2.4	
			4.5	1.7	2.50	3.2	1.7	3.2	
			5.5	2.1	3.00	3.9	2.1	3.9	
V_{T-}	Negative going threshold	Figures 1 and 2	1.2	–	0.34	–	–	–	V
			2.0	0.3	0.65	0.9	0.3	0.9	
			2.7	0.4	0.90	1.4	0.4	1.4	
			3.0	0.6	1.05	1.5	0.6	1.5	
			3.6	0.8	1.30	1.8	0.8	1.8	
			4.5	0.9	1.60	2.0	0.9	2.0	
			5.5	1.2	2.00	2.6	1.2	2.6	
V_H	Hysteresis ($V_{T+} – V_{T-}$)	Figures 1 and 2	1.2	–	0.30	–	–	–	V
			2.0	0.2	0.55	0.8	0.2	0.8	
			2.7	0.3	0.60	1.1	0.3	1.1	
			3.0	0.4	0.65	1.2	0.4	1.2	
			3.6	0.4	0.70	1.2	0.4	1.2	
			4.5	0.4	0.80	1.4	0.4	1.4	
			5.5	0.6	1.00	1.5	0.6	1.5	

NOTE:
1. Unless otherwise stated, all typical values are at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85°C			–40 to +125°C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA, nB, to nY	Figure 6	1.2	–	65	–	–	–	ns
			2.0	–	18	34	–	43	
			2.7	–	15	24	–	30	
			3.0 to 3.6	–	12[2]	20	–	25	
			4.5 to 5.5	–	9.0[2]	14	–	17	

NOTES:
1. Unless otherwise stated, all typical values are at T_{amb} = 25°C.
2. Typical value measured at V_{CC} = 3.3V.
3. Typical value measured at V_{CC} = 5.0V.

TRANSFER CHARACTERISTIC WAVEFORMS

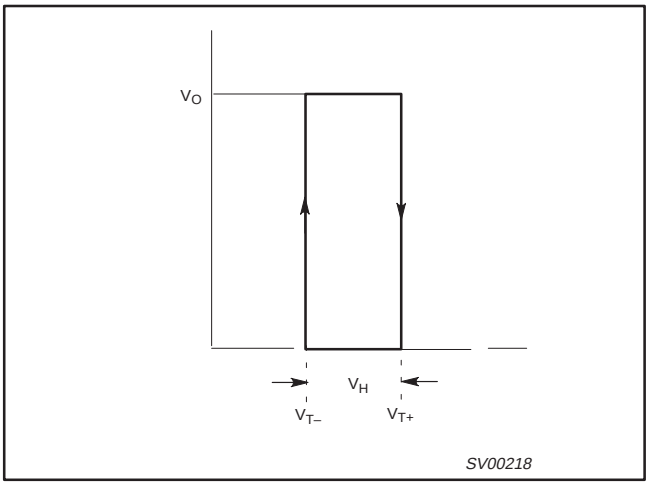


Figure 1. Transfer characteristic.

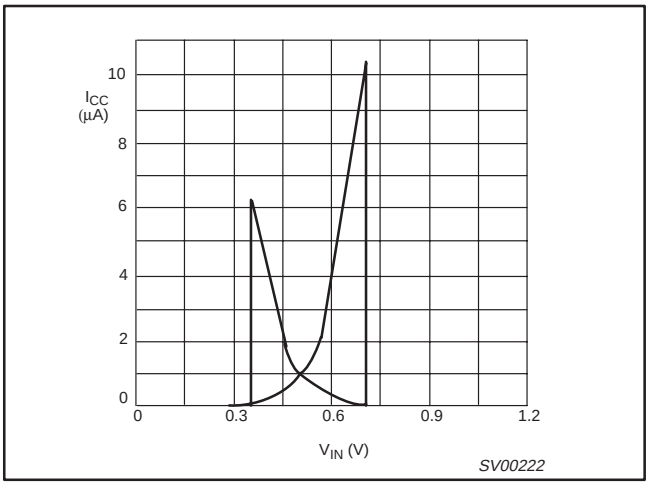


Figure 3. Typical LV132 transfer characteristics; V_{CC} = 1.2V.

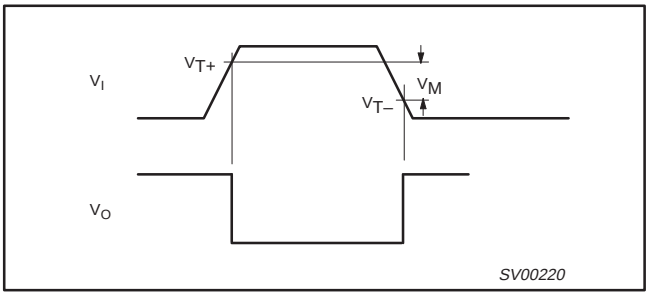


Figure 2. Definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%.

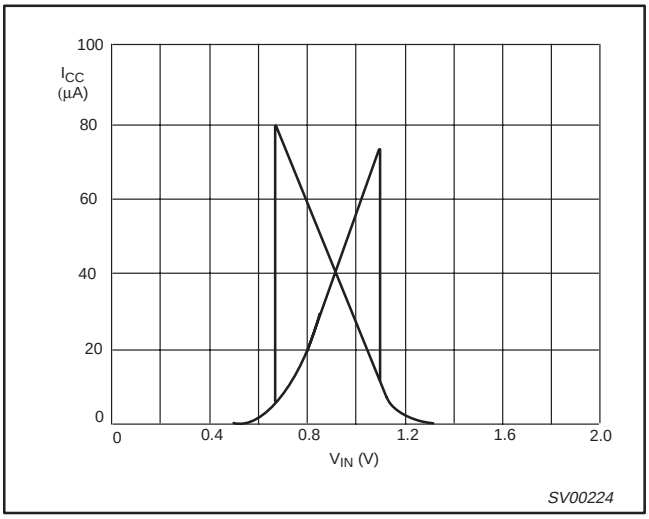


Figure 4. Typical LV132 transfer characteristics; V_{CC} = 2.0V.

TRANSFER CHARACTERISTIC WAVEFORMS (Continued)

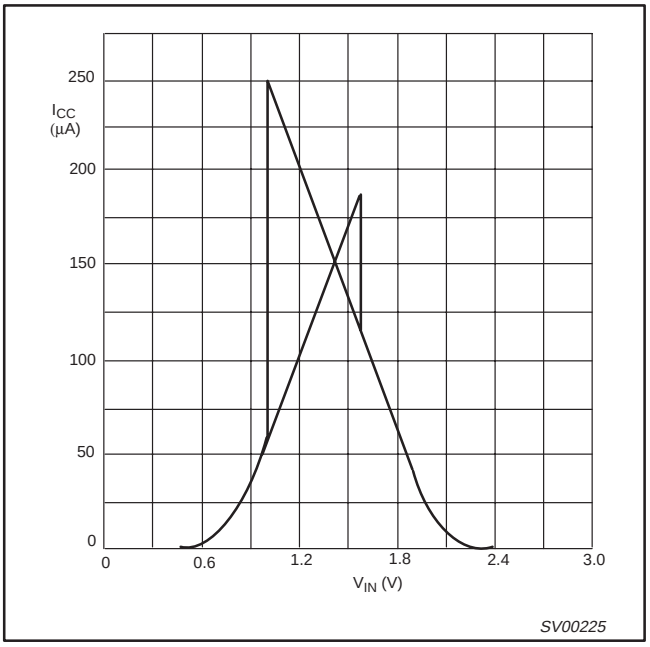


Figure 5. Typical LV132 transfer characteristics; V_{CC} = 3.0V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq 2.7V \leq 3.6V$
V_M = 0.5V * V_{CC} at $V_{CC} < 2.7V$ and $\geq 4.5V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

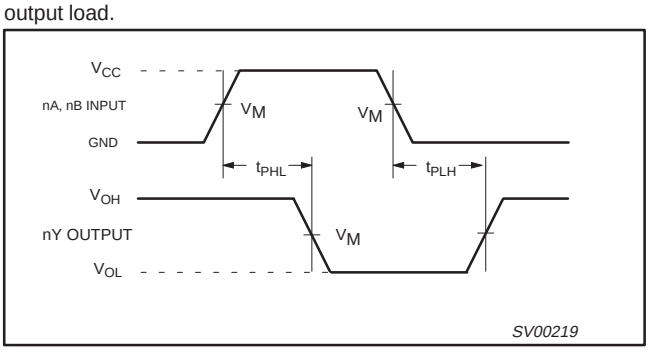
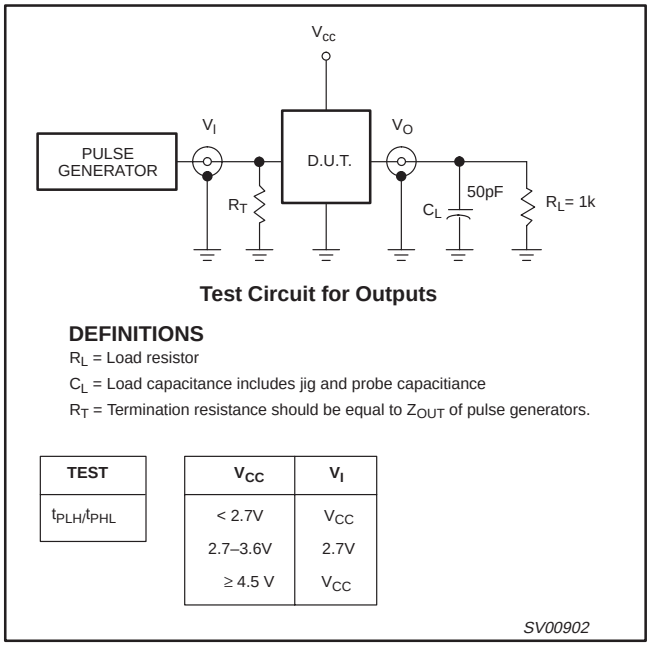


Figure 6. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

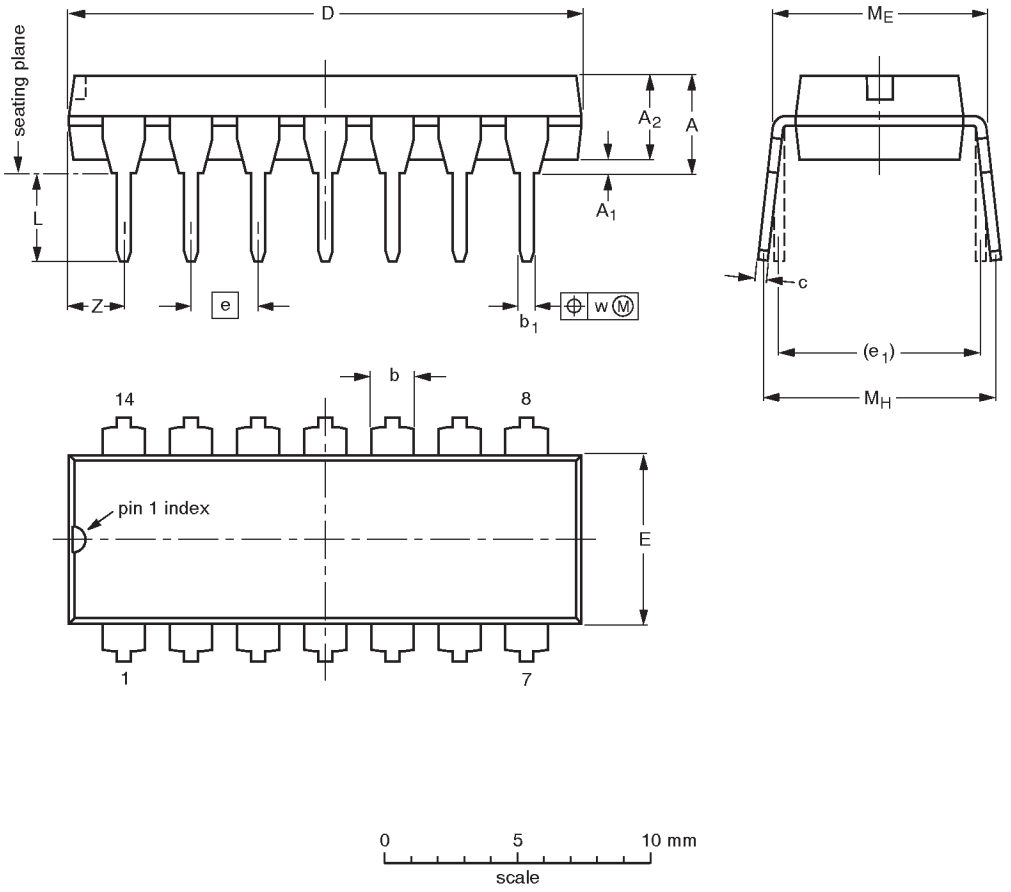
C_L = Load capacitance includes jig and probe capacitiance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V
	≥ 4.5 V	V_{CC}

Figure 7.Load circuitry for switching times.

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

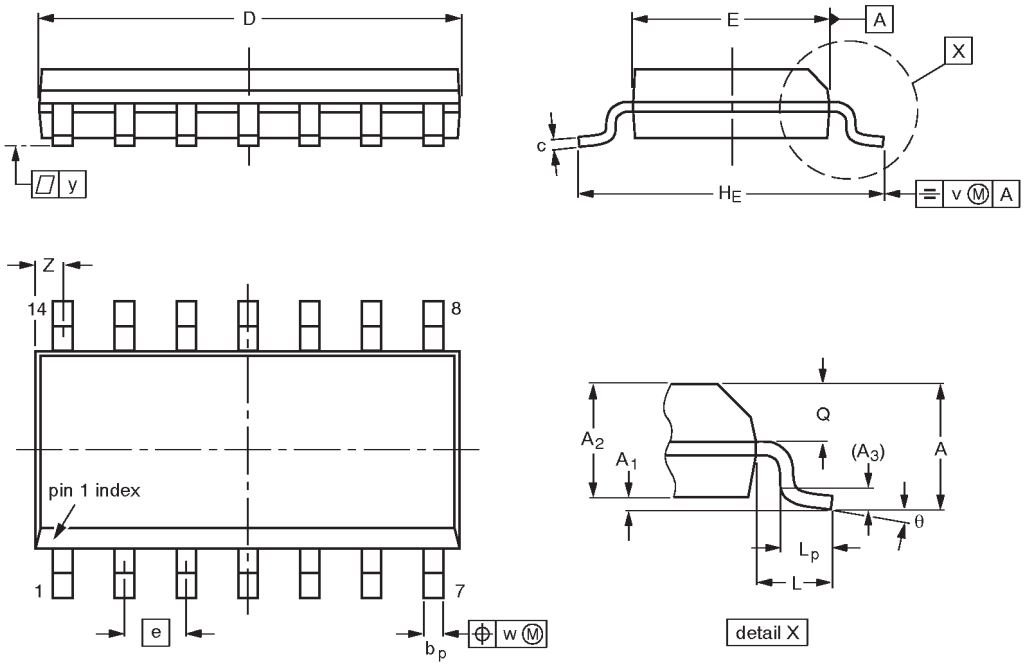
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

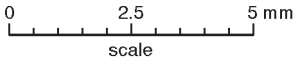
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

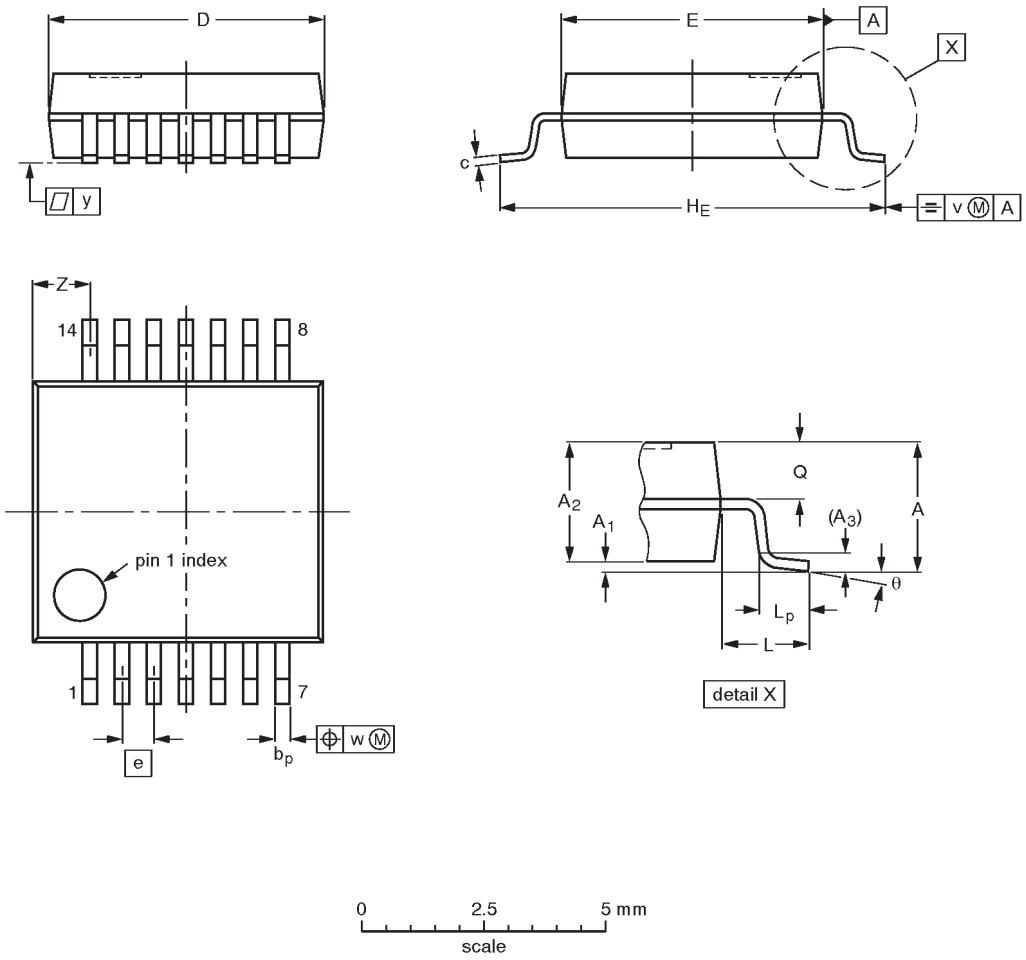
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

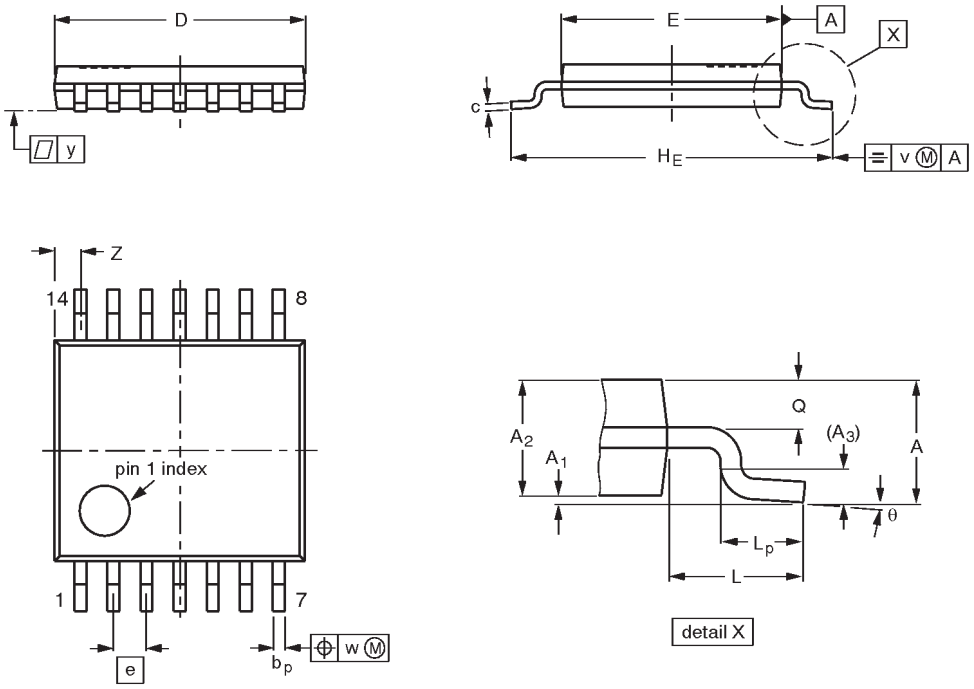
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

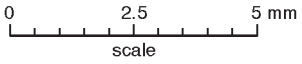
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~95-02-04~~ 96-01-18

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~94-07-12~~ 95-04-04

Data sheet status

Data sheet status	Product status	Definition [1]
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