# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

# 74HC/HCT4020

## 14-stage binary ripple counter

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

# 14-stage binary ripple counter 74HC/HCT4020

## FEATURES

- Output capability: standard
- $I_{CC}$ category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT4020 are high-speed Si-gate CMOS devices and are pin compatible with the “4020” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4020 are 14-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs ($Q_0$, $Q_3$ to $Q_{13}$).

The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f$ = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| $t_{PHL}/ t_{PLH}$ | propagation delay | $C_L$ = 15 pF; $V_{CC}$ = 5 V | | | |
| | $\overline{CP}$ to $Q_0$ | | 11 | 15 | ns |
| | $Q_n$ to $Q_{n+1}$ | | 6 | 6 | ns |
| | MR to $Q_n$ | | 17 | 19 | ns |
| $f_{max}$ | maximum clock frequency | | 101 | 52 | MHz |
| $C_I$ | input capacitance | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation capacitance per package | notes 1 and 2 | 19 | 20 | pF |

### Notes

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz

   $f_o$ = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   $C_L$ = output load capacitance in pF

   $V_{CC}$ = supply voltage in V

2. For HC the condition is $V_I$ = GND to $V_{CC}$
   For HCT the condition is $V_I$ = GND to $V_{CC}$ – 1.5 V

## ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

**PIN DESCRIPTION**

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3 | $Q_0$, $Q_3$ to $Q_{13}$ | parallel outputs |
| 8 | GND | ground (0 V) |
| 10 | $\overline{CP}$ | clock input (HIGH-to-LOW, edge-triggered) |
| 11 | MR | master reset input (active HIGH) |
| 16 | $V_{CC}$ | positive supply voltage |

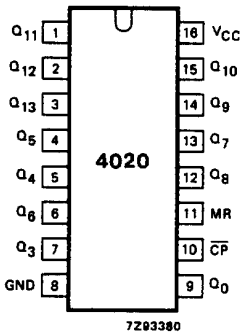



Fig.1 Pin configuration.

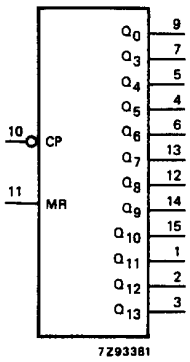



Fig.2 Logic symbol.

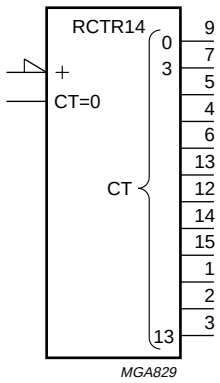



Fig.3 IEC logic symbol.

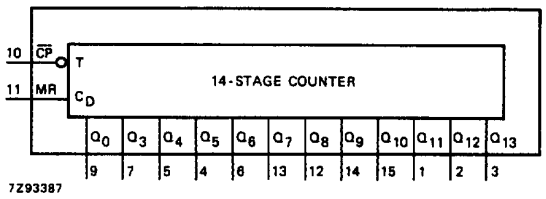



Fig.4 Functional diagram.

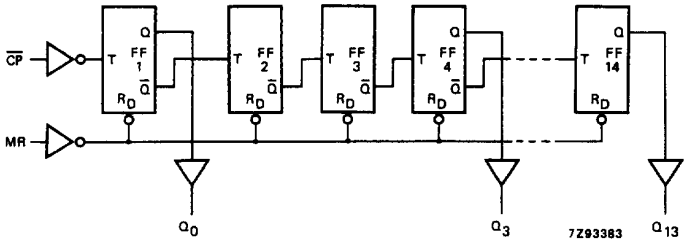



Fig.5 Logic diagram.

**FUNCTION TABLE**

| INPUTS | | OUTPUTS |
|---|---|---|
| $\overline{CP}$ | MR | $Q_0$, $Q_3$ to $Q_{13}$ |
| ↑ | L | no change |
| ↓ | L | count |
| X | H | L |

**Notes**

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH clock transition
   ↓ = HIGH-to-LOW clock transition

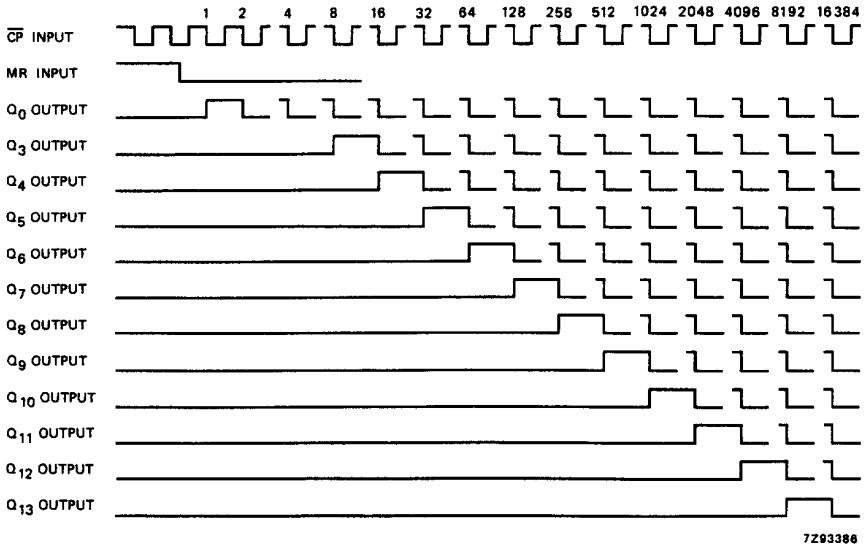



Fig.6 Timing diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{CP}$ to $Q_0$ | | 39<br>14<br>11 | 140<br>28<br>24 | | 175<br>35<br>30 | | 210<br>42<br>36 | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $Q_n$ to $Q_{n+1}$ | | 22<br>8<br>6 | 75<br>15<br>13 | | 95<br>19<br>16 | | 110<br>22<br>19 | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{PHL}$ | propagation delay MR to $Q_n$ | | 55<br>20<br>16 | 170<br>34<br>29 | | 215<br>43<br>37 | | 225<br>51<br>43 | ns | 2.0<br>4.5<br>6.0 | Fig.8 |
| $t_{THL}/ t_{TLH}$ | output transition time | | 19<br>7<br>6 | 75<br>15<br>13 | | 95<br>19<br>16 | | 110<br>22<br>19 | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_W$ | clock pulse width HIGH or LOW | 80<br>16<br>14 | 11<br>4<br>3 | | 100<br>20<br>17 | | 120<br>24<br>20 | | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_W$ | master reset pulse width HIGH | 80<br>16<br>14 | 17<br>6<br>5 | | 100<br>20<br>17 | | 120<br>24<br>20 | | ns | 2.0<br>4.5<br>6.0 | Fig.8 |
| $t_{rem}$ | removal time MR to $\overline{CP}$ | 50<br>10<br>9 | 6<br>2<br>2 | | 65<br>13<br>11 | | 75<br>15<br>13 | | ns | 2.0<br>4.5<br>6.0 | Fig.8 |
| $f_{max}$ | maximum clock pulse frequency | 6.0<br>30<br>35 | 30<br>92<br>109 | | 4.8<br>24<br>28 | | 4.0<br>20<br>24 | | MHz | 2.0<br>4.5<br>6.0 | Fig.7 |

### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

### Note to HCT types

The value of additional quiescent supply current ($\Delta I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

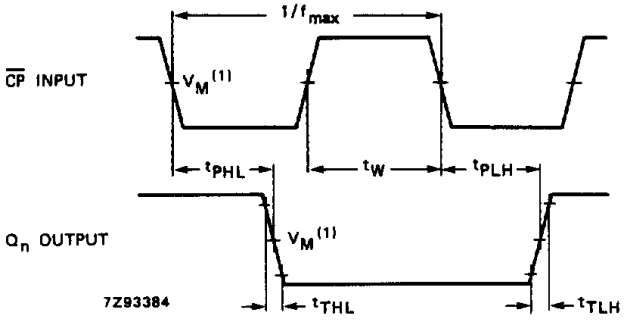
| INPUT | UNIT LOAD COEFFICIENT |
|---|---|
| $\overline{CP}$ | 0.85 |
| MR | 1.10 |

### AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

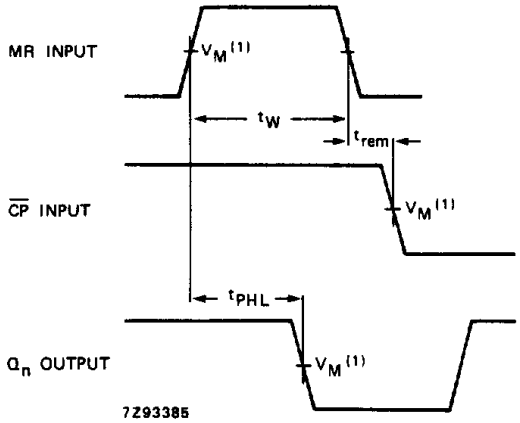
| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | –40 to +85 | | –40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{CP}$ to $Q_0$ | | 18 | 36 | | 45 | | 54 | ns | 4.5 | Fig.7 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $Q_n$ to $Q_{n+1}$ | | 8 | 15 | | 19 | | 22 | ns | 4.5 | Fig.7 |
| $t_{PHL}$ | propagation delay MR to $Q_n$ | | 22 | 45 | | 56 | | 68 | ns | 4.5 | Fig.8 |
| $t_{THL}/ t_{TLH}$ | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.7 |
| $t_W$ | clock pulse width HIGH or LOW | 20 | 7 | | 25 | | 30 | | ns | 4.5 | Fig.7 |
| $t_W$ | master reset pulse width HIGH | 20 | 8 | | 25 | | 30 | | ns | 4.5 | Fig.8 |
| $t_{rem}$ | removal time MR to $\overline{CP}$ | 10 | 2 | | 13 | | 15 | | ns | 4.5 | Fig.8 |
| $f_{max}$ | maximum clock pulse frequency | 25 | 47 | | 20 | | 17 | | MHz | 4.5 | Fig.7 |

## AC WAVEFORMS




(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.7 Waveforms showing the clock ($\overline{CP}$) to output ($Q_n$) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.




(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.8 Waveforms showing the master reset (MR) pulse width, the master reset to output ($Q_n$) propagation delays and the master reset to clock ($\overline{CP}$) removal time.

## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.