FAIRCHILD SEMICONDUCTOR™

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MM74HC4046
CMOS Phase Lock Loop

General Description

The MM74HC4046 is a low power phase lock loop utilizing advanced silicon-gate CMOS technology to obtain high frequency operation both in the phase comparator and VCO sections. This device contains a low power linear voltage controlled oscillator (VCO), a source follower, and three phase comparators. The three phase comparators have a common signal input and a common comparator input. The signal input has a self biasing amplifier allowing signals to be either capacitively coupled to the phase comparators with a small signal or directly coupled with standard input logic levels. This device is similar to the CD4046 except that the Zener diode of the metal gate CMOS device has been replaced with a third phase comparator.

Phase Comparator I is an exclusive OR (XOR) gate. It provides a digital error signal that maintains a 90 phase shift between the VCO's center frequency and the input signal (50% duty cycle input waveforms). This phase detector is more susceptible to locking onto harmonics of the input frequency than phase comparator I, but provides better noise rejection.

Phase comparator III is an SR flip-flop gate. It can be used to provide the phase comparator functions and is similar to the first comparator in performance.

Phase comparator II is an edge sensitive digital sequential network. Two signal outputs are provided, a comparator output and a phase pulse output. The comparator output is a 3-STATE output that provides a signal that locks the VCO output signal to the input signal with 0 phase shift between them. This comparator is more susceptible to noise throwing the loop out of lock, but is less likely to lock onto harmonics than the other two comparators.

In a typical application any one of the three comparators feed an external filter network which in turn feeds the VCO input. This input is a very high impedance CMOS input which also drives the source follower. The VCO's operating frequency is set by three external components connected to the C1A, C1B, R1 and R2 pins. An inhibit pin is provided to disable the VCO and the source follower, providing a method of putting the IC in a low power state.

The source follower is a MOS transistor whose gate is connected to the VCO input and whose drain connects the Demodulator output. This output normally is used by tying a resistor from pin 10 to ground, and provides a means of looking at the VCO input without loading down modifying the characteristics of the PLL filter.

Features

- Low dynamic power consumption: (V_{CC} = 4.5V)
- Maximum VCO operating frequency: 12 MHz (V_{CC} = 4.5V)
- Fast comparator response time (V_{CC} = 4.5V)
  - Comparator I: 25 ns
  - Comparator II: 30 ns
  - Comparator III: 25 ns
- VCO has high linearity and high temperature stability

Ordering Code:

Order Number	Package Number	Package Description
MM74HC4046M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4046SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4046MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4046N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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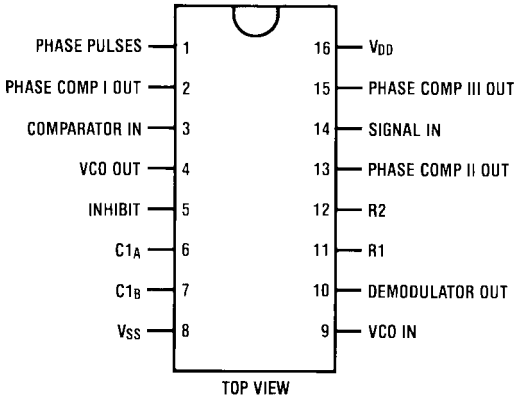
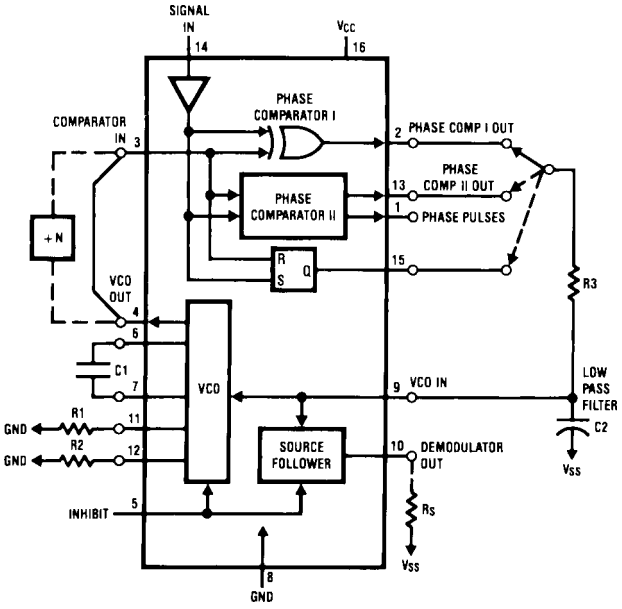
Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Block Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to + 7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH}or V_{IL}						
		$\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 3,5,9)	V_{IN} = V_{CC}or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{IN}	Maximum Input Current (Pin 14)	V_{IN} = V_{CC} or GND	6.0V	20	50	80	100	μA
I_{OZ}	Maximum 3-STATE Output Leakage Current (Pin 13)	V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	6.0V	30	80	130	160	μA
		I_{OUT} = 0 μA						
		V_{IN} = V_{CC} or GND	6.0V	600	1500	2400	3000	μA
		Pin 14 Open						

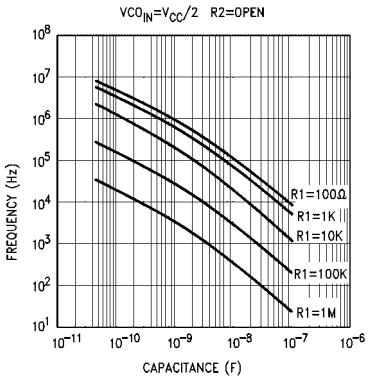
Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics V_{CC} = 2.0 to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified.)

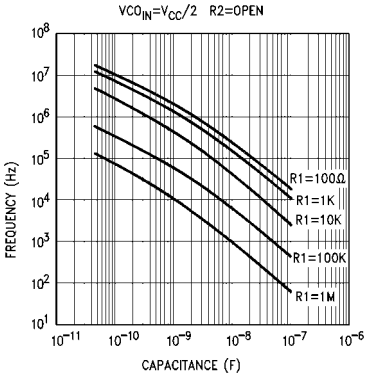
Symbol	Parameters	Conditions	V_{CC}	T_A=25C		T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
	AC Coupled	C (series) = 100 pF	2.0V	25	100	150	200	mV
	Input Sensitivity,	f_{IN} = 500 kHz	4.5V	50	150	200	250	mV
	Signal In		6.0V	135	250	300	350	mV
t_r, t_f	Maximum Output		2.0V	30	75	95	110	ns
	Rise and Fall Time		4.5V	9	15	19	22	ns
			6.0V	8	12	15	19	ns
C_{IN}	Maximum Input Capacitance		7					pF
Phase Comparator I								
t_{PHL}, t_{PLH}	Maximum		2.0V	65	200	250	300	ns
	Propagation Delay		4.5V	25	40	50	60	ns
			6.0V	20	34	43	51	ns
Phase Comparator II								
t_{PZL}	Maximum 3-STATE		2.0V	75	225	280	340	ns
	Enable Time		4.5V	25	45	56	68	ns
			6.0V	22	38	48	57	ns
t_{PZH}, t_{PHZ}	Maximum 3-STATE		2.0V	88	240	300	360	ns
	Enable Time		4.5V	30	48	60	72	ns
			6.0V	25	41	51	61	ns
t_{PLZ}	Maximum 3-STATE		2.0V	90	240	300	360	ns
	Disable Time		4.5V	32	48	60	72	ns
			6.0V	28	41	51	61	ns
t_{PHL}, t_{PLH}	Maximum		2.0V	100	250	310	380	ns
	Propagation Delay		4.5V	34	50	63	75	ns
	HIGH-to-LOW to Phase Pulses		6.0V	27	43	53	64	ns
Phase Comparator III								
t_{PHL}, t_{PLH}	Maximum		2.0V	75	200	250	300	ns
	Propagation Delay		4.5V	25	40	50	60	ns
			6.0V	22	34	43	51	ns
C_{PD}	Maximum Power	All Comparators		130				pF
	Dissipation Capacitance	$V_{IN} = V_{CC}$ and GND						
Voltage Controlled Oscillator (Specified to operate from V_{CC}= 3.0V to 6.0V)								
f_{MAX}	Maximum	C1 = 50 pF						
	Operating	R1 = 100Ω	4.5V	7	4.5			MHz
	Frequency	R2 = ∞	6.0V	11	7			MHz
		$VCO_{in} = V_{CC}$						
		C1 = 0 pF	4.5V	12				MHz
		R1 = 100Ω	6.0	14				MHz
		$VCO_{in} = V_{CC}$						
	Duty Cycle			50				%
Demodulator Output								
	Offset Voltage	R_S = 20 kΩ	4.5V	0.75	1.3	1.5	1.6	V
	VCO_{in}–V_{dem}							
	Offset	R_S = 20 kΩ	4.5V					
	Variation	VCO_{in} = 1.75V		0.65				V
		2.25V		0.1				
		2.75V		0.75				

Typical Performance Characteristics

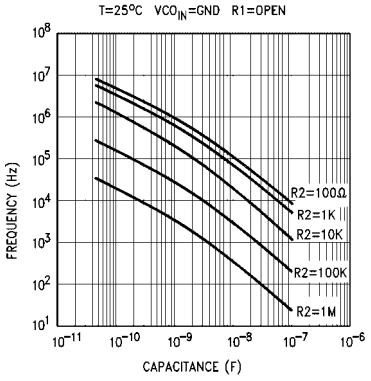
Typical Center Frequency vs R1, C1 V_{CC} = 4.5V



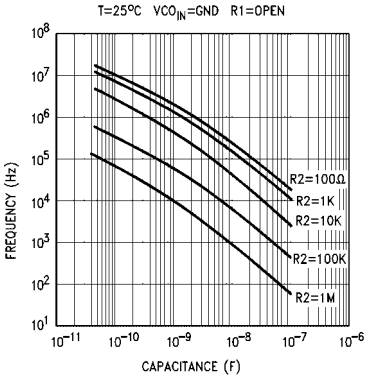
Typical Center Frequency vs R1, C1 V_{CC} = 6V



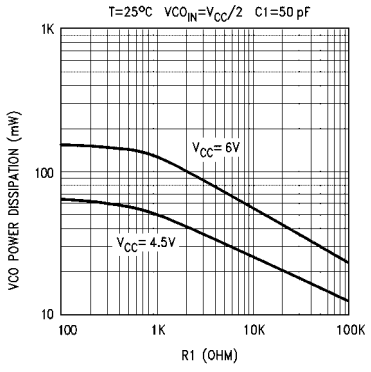
Typical Offset Frequency vs R2, C1 V_{CC} = 4.5V



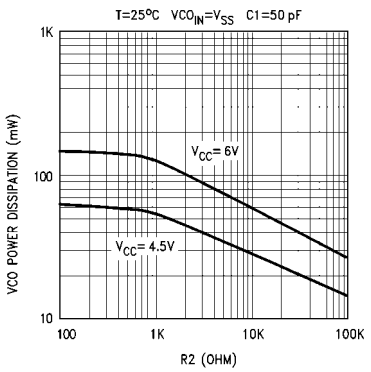
Typical Offset Frequency vs R2, C1 V_{CC} = 6V



Typical VCO Power Dissipation @ Center Frequency vs R1

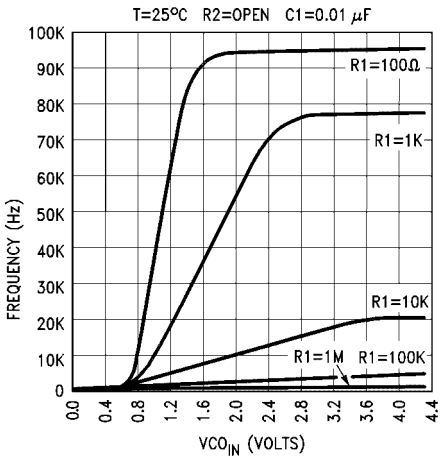


Typical VCO Power Dissipation @ f_{MIN} vs R2

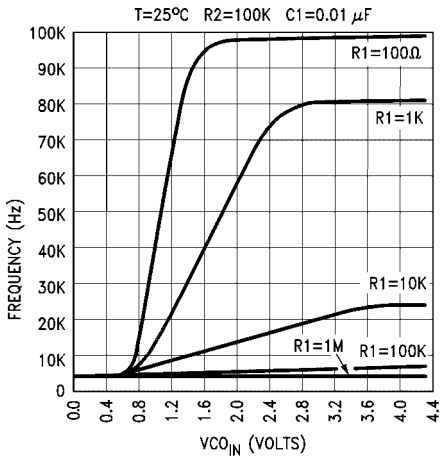


Typical Performance Characteristics (Continued)

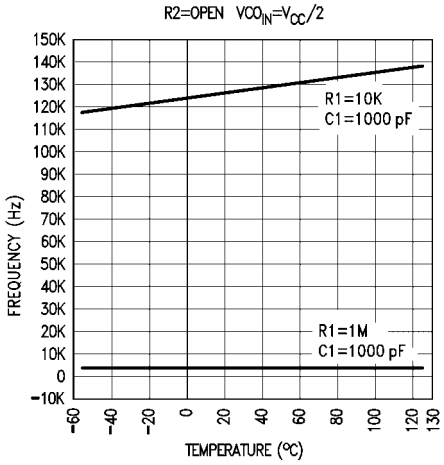
VCO_{in} vs f_{out} V_{CC} = 4.5V



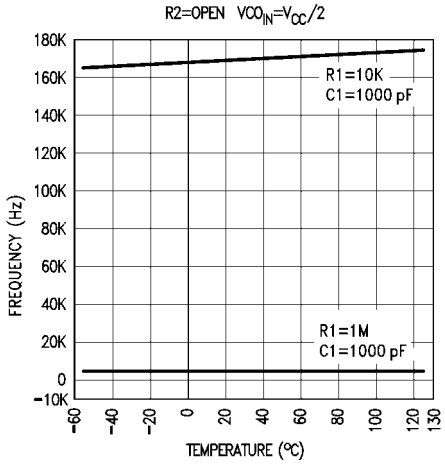
VCO_{in} vs f_{out} V_{CC} = 4.5V



VCO_{out} vs Temperature V_{CC} = 4.5V

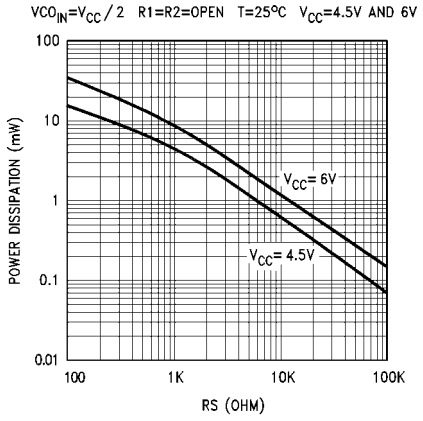


VCO_{out} vs Temperature V_{CC} = 6V

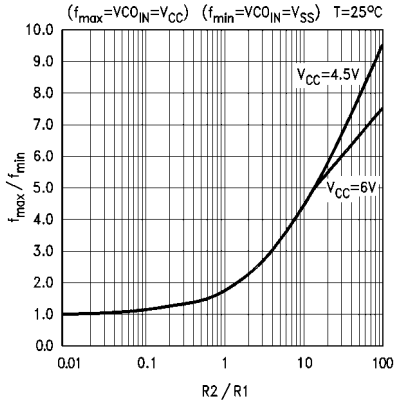


Typical Performance Characteristics (Continued)

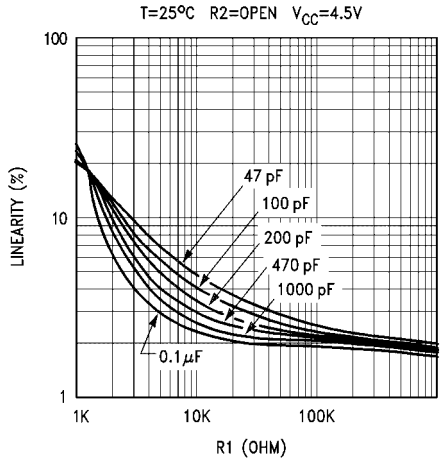
HC4046 Typical Source Follower Power Dissipation vs RS



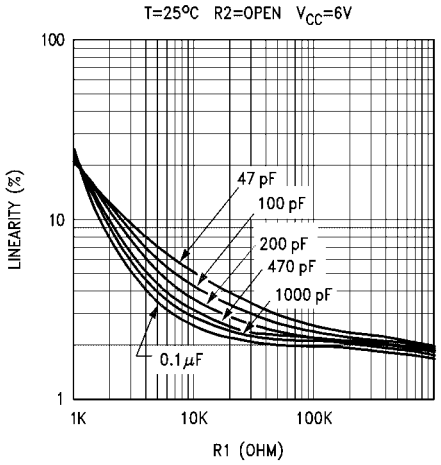
Typical f_{MAX}/f_{MIN} vs R2/R1
V_{CC} = 4.5V & 6V f_{MAX}/f_{MIN}



Typical VCO Linaearity vs R1 & C1



Typical VCO Linearity vs R1 & C1



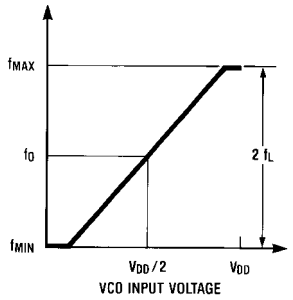
Detailed Circuit Description

VOLTAGE CONTROLLED OSCILLATOR/SOURCE FOLLOWER

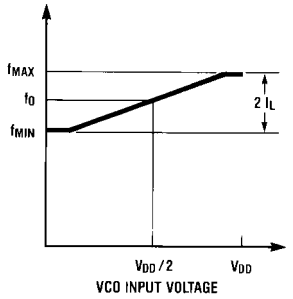
The VCO requires two or three external components to operate. These are R1, R2, C1. Resistor R1 and capacitor C1 are selected to determine the center frequency of the VCO. R1 controls the lock range. As R1's resistance decreases the range of f_{MIN} to f_{MAX} increases. Thus the VCO's gain increases. As C1 is changed the offset (if used) of R2, and the center frequency is changed. (See typical performance curves) R2 can be used to set the offset frequency with 0V at VCO input. If R2 is omitted the VCO range is from 0Hz. As R2 is decreased the offset frequency is increased. The effect of R2 is shown in the design information table and typical performance curves. By increasing the value of R2 the lock range of the PLL is offset above 0Hz and the gain (Hz/Volt) does not change. In general, when offset is desired, R2 and C1 should be chosen first, and then R1 should be chosen to obtain the proper center frequency.

Internally the resistors set a current in a current mirror as shown in Figure 1. The mirrored current drives one side of the capacitor once the capacitor charges up to the threshold of the schmitt trigger the oscillator logic flips the capacitor over and causes the mirror to charge the opposite side of the capacitor. The output from the internal logic is then taken to pin 4.

VCO WITHOUT OFFSET
R2 = ∞



VCO WITH OFFSET



Comparator I		Comparator II & III	
$R_2 = \infty$	$R_2 \neq \infty$	$R_2 = \infty$	$R_2 \neq \infty$
•Given: f_0 •Use f_0 with curve titled center frequency vs R1, C to determine R1 and C1	•Given: f_0 and f_L •Calculate f_{MIN} from the equation $f_{MIN} = f_o - f_L$ •Use f_{MIN} with curve titled offset frequency vs R2, C to determine R2 and C1 •Calculate f_{MAX}/f_{MIN} from the equation $f_{MAX}/f_{MIN} = f_o + f_L/f_o - f_L$ •Use f_{MAX}/f_{MIN} with curve titled f_{MAX}/f_{MIN} vs R2/R1 to determine ratio R2/R1 to obtain R1	•Given: f_{MAX} •Calculate f_0 from the equation $f_o = f_{MAX}/2$ •Use f_0 with curve titled center frequency vs R1, C to determine R1 and C1	•Given: f_{MIN} and f_{MAX} •Use f_{MIN} with curve titled offset frequency vs R2, C to determine R2 and C1 •Calculate f_{MAX}/f_{MIN} •Use f_{MAX}/f_{MIN} with curve titled f_{MAX}/f_{MIN} vs R2/R1 to determine ratio R2/R1 to obtain R1

FIGURE 1.

Detailed Circuit Description (Continued)

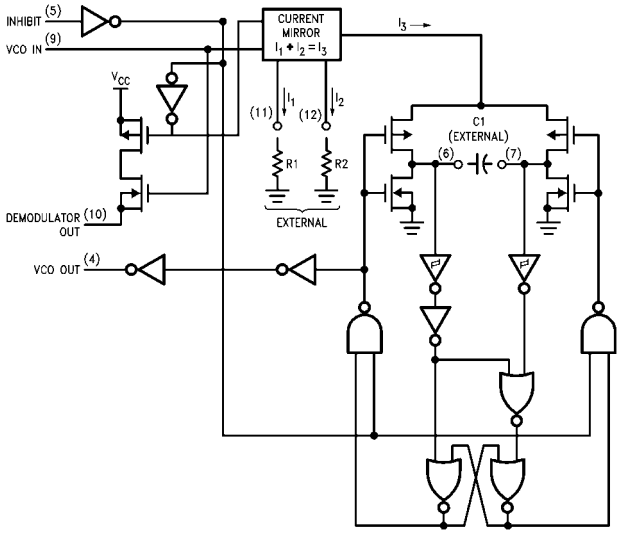


FIGURE 2. Logic Diagram for VCO

The input to the VCO is a very high impedance CMOS input and so it will not load down the loop filter, easing the filters design. In order to make signals at the VCO input accessible without degrading the loop performance a source follower transistor is provided. This transistor can be used by connecting a resistor to ground and its drain output will follow the VCO input signal.

An inhibit signal is provided to allow disabling of the VCO and the source follower. This is useful if the internal VCO is not being used. A logic high on inhibit disables the VCO and source follower.

The output of the VCO is a standard high speed CMOS output with an equivalent LSTTL fanout of 10. The VCO output is approximately a square wave. This output can either directly feed the comparator input of the phase comparators or feed external prescalers (counters) to enable frequency synthesis.

PHASE COMPARATORS

All three phase comparators share two inputs, Signal In and Comparator In. The Signal In has a special DC bias network that enables AC coupling of input signals. If the signals are not AC coupled then this input requires logic levels the same as standard 74HC. The Comparator input is a standard digital input. Both input structures are shown in Figure 3.

The outputs of these comparators are essentially standard 74HC voltage outputs. (Comparator II is 3-STATE.)

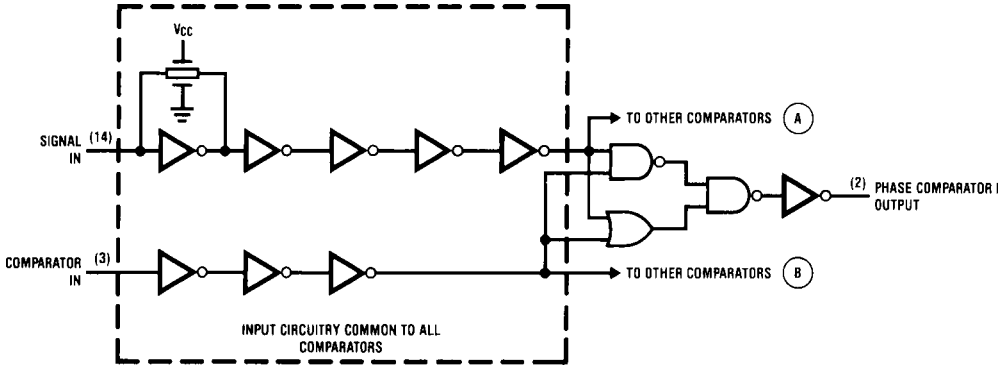


FIGURE 3. Logic Diagram for Phase Comparator I and the common input circuit for all three comparators

Detailed Circuit Description (Continued)

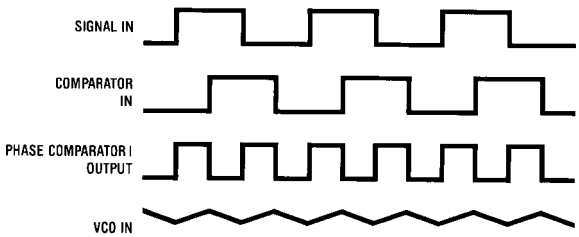


FIGURE 4. Typical Phase Comparator I. Waveforms

Thus in normal operation V_{CC} and ground voltage levels are fed to the loop filter. This differs from some phase detectors which supply a current output to the loop filter and this should be considered in the design. (The CD4046 also provides a voltage.)

Figure 5 shows the state tables for all three comparators.

PHASE COMPARATOR I

This comparator is a simple XOR gate similar to the 74HC86, and its operation is similar to an overdriven balanced modulator. To maximize lock range the input frequencies must have a 50% duty cycle. Typical input and output waveforms are shown in Figure 4. The output of the phase detector feeds the loop filter which averages the output voltage. The frequency range upon which the PLL will lock onto if initially out of lock is defined as the capture range. The capture range for phase detector I is dependent on the loop filter employed. The capture range can be as large as the lock range which is equal to the VCO frequency range.

To see how the detector operates refer to Figure 4. When two square wave inputs are applied to this comparator, an output waveform whose duty cycle is dependent on the phase difference between the two signals results. As the phase difference increases the output duty cycle increases and the voltage after the loop filter increases. Thus in order to achieve lock, when the PLL input frequency increases the VCO input voltage must increase and the phase difference between comparator in and signal in will increase. At an input frequency equal f_{MIN}, the VCO input is at 0V and this requires the phase detector output to be ground hence the two input signals must be in phase. When the input frequency is f_{MAX} then the VCO input must be V_{CC} and the phase detector inputs must be 180° out of phase.

The XOR is more susceptible to locking onto harmonics of the signal input than the digital phase detector II. This can be seen by noticing that a signal 2 times the VCO frequency results in the same output duty cycle as a signal equal the VCO frequency. The difference is that the output frequency of the 2f example is twice that of the other example. The loop filter and the VCO range should be designed to prevent locking on to harmonics.

PHASE COMPARATOR II

This detector is a digital memory network. It consists of four flip-flops and some gating logic, a three state output and a phase pulse output as shown in Figure 6. This comparator acts only on the positive edges of the input signals and is thus independent of signal duty cycle.

Phase comparator II operates in such a way as to force the PLL into lock with 0 phase difference between the VCO output and the signal input positive waveform edges. Figure 7 shows some typical loop waveforms. First assume that the signal input phase is leading the comparator input. This means that the VCO's frequency must be increased to bring its leading edge into proper phase alignment. Thus the phase detector II output is set high. This will cause the loop filter to charge up the VCO input increasing the VCO frequency. Once the leading edge of the comparator input is detected the output goes 3-STATE holding the VCO input at the loop filter voltage. If the VCO still lags the signal then the phase detector will again charge up to VCO input for the time between the leading edges of both waveforms.

Detailed Circuit Description (Continued)

Phase Comparator State Diagrams

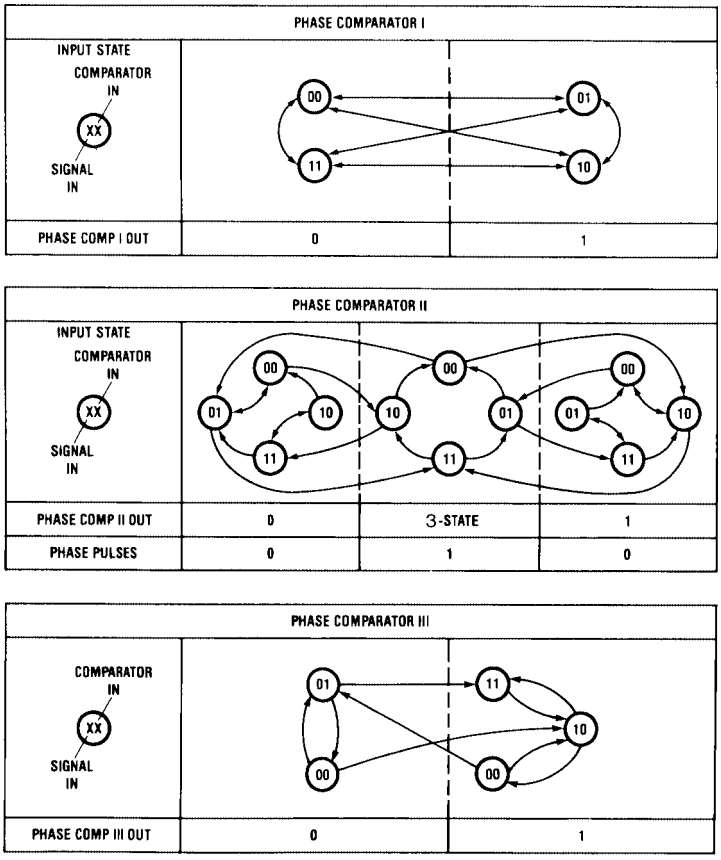


FIGURE 5. PLL State Tables

Detailed Circuit Description (Continued)

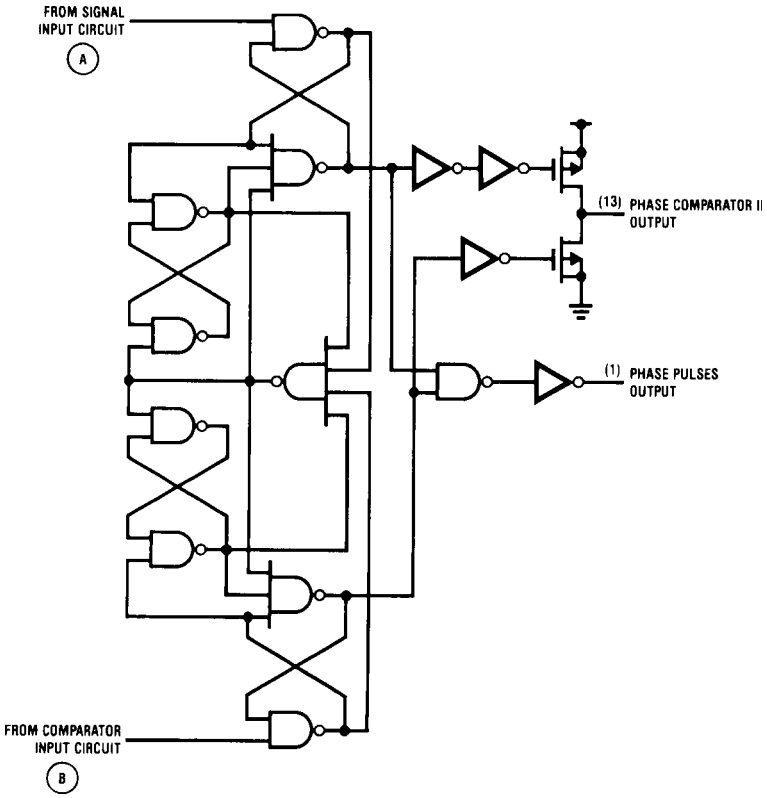


FIGURE 6. Logic Diagram for Phase Comparator II

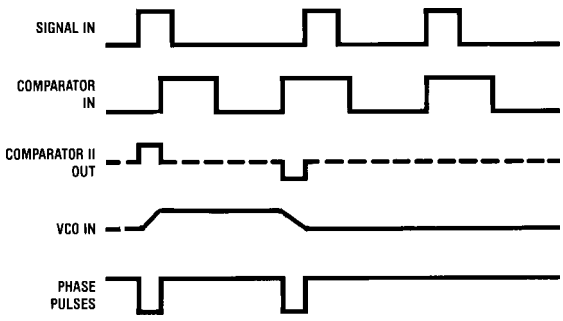


FIGURE 7. Typical Phase Comparator II Output Waveforms

Detailed Circuit Description (Continued)

If the VCO leads the signal then when the leading edge of the VCO is seen the output of the phase comparator goes LOW. This discharges the loop filter until the leading edge of the signal is detected at which time the output 3-STATE itself again. This has the effect of slowing down the VCO to again make the rising edges of both waveform coincident.

When the PLL is out of lock the VCO will be running either slower or faster than the signal input. If it is running slower the phase detector will see more signal rising edges and so the output of the phase comparator will be HIGH a majority of the time, raising the VCO's frequency. Conversely, if the VCO is running faster than the signal the output of the detector will be LOW most of the time and the VCO's output frequency will be decreased.

As one can see when the PLL is locked the output of phase comparator II will be almost always 3-STATE except for minor corrections at the leading edge of the waveforms. When the detector is 3-STATE the phase pulse output is HIGH. This output can be used to determine when the PLL is in the locked condition.

This detector has several interesting characteristics. Over the entire VCO frequency range there is no phase difference between the comparator input and the signal input. The lock range of the PLL is the same as the capture range. Minimal power is consumed in the loop filter since in lock the detector output is a high impedance. Also when no signal is present the detector will see only VCO leading edges, and so the comparator output will stay LOW forcing the VCO to f_{MIN} operating frequency.

Phase comparator II is more susceptible to noise causing the phase lock loop to unlock. If a noise pulse is seen on the signal input, the comparator treats it as another positive edge of the signal and will cause the output to go HIGH until the VCO leading edge is seen, potentially for a whole signal input period. This would cause the VCO to speed up during that time. When using the phase comparator I the output of that phase detector would be disturbed for only the short duration of the noise spike and would cause less upset.

PHASE COMPARATOR III

This comparator is a simple S-R Flip-Flop which can function as a phase comparator Figure 8. It has some similar characteristics to the edge sensitive comparator. To see how this detector works assume input pulses are applied to the signal and comparator inputs as shown in Figure 9. When the signal input leads the comparator input the flop is set. This will charge up the loop filter and cause the VCO to speed up, bringing the comparator into phase with the signal input. When using short pulses as input this comparator behaves very similar to the second comparator. But one can see that if the signal input is a long pulse, the output of the comparator will be forced to a one no matter how many comparator input pulses are received. Also if the VCO input is a square wave (as it is) and the signal input is pulse then the VCO will force the comparator output LOW much of the time. Therefore it is ideal to condition the signal and comparator input to short pulses. This is most easily done by using a series capacitor.

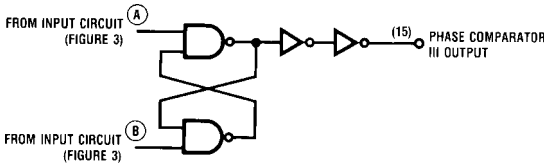


FIGURE 8. Phase Comparator III Logic Diagram

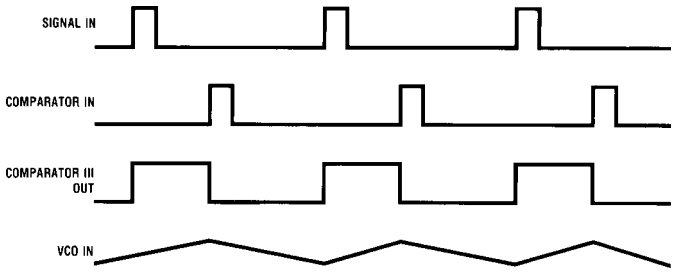
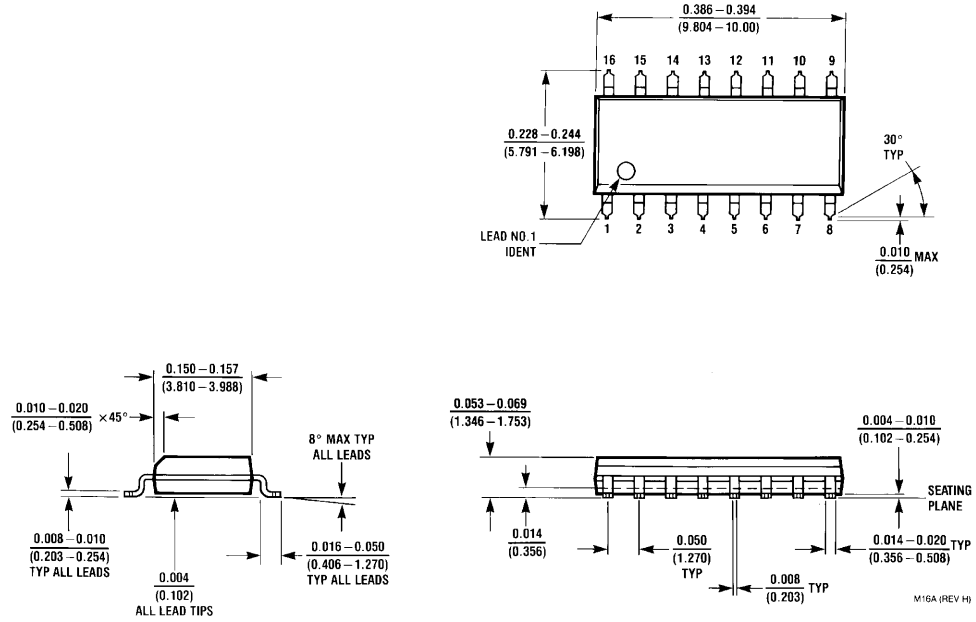


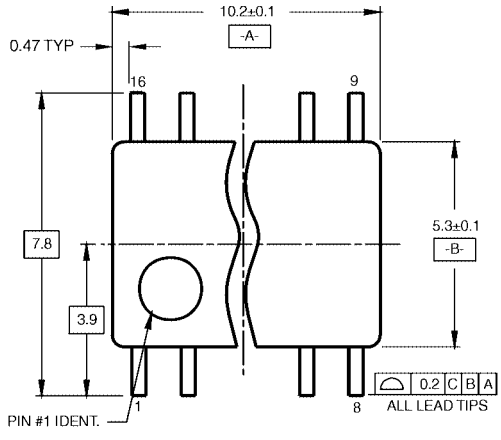
FIGURE 9. Typical Waveforms for Phase Comparator III

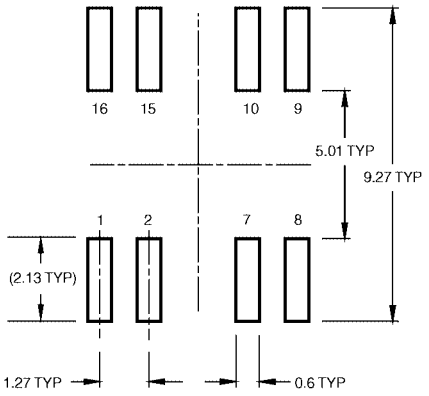
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





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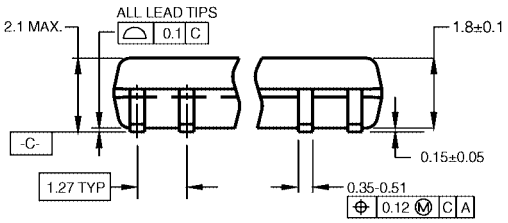
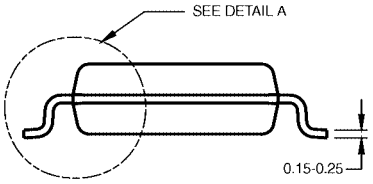




DIMENSIONS ARE IN MILLIMETERS

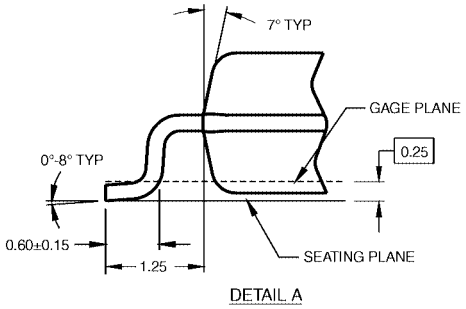
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

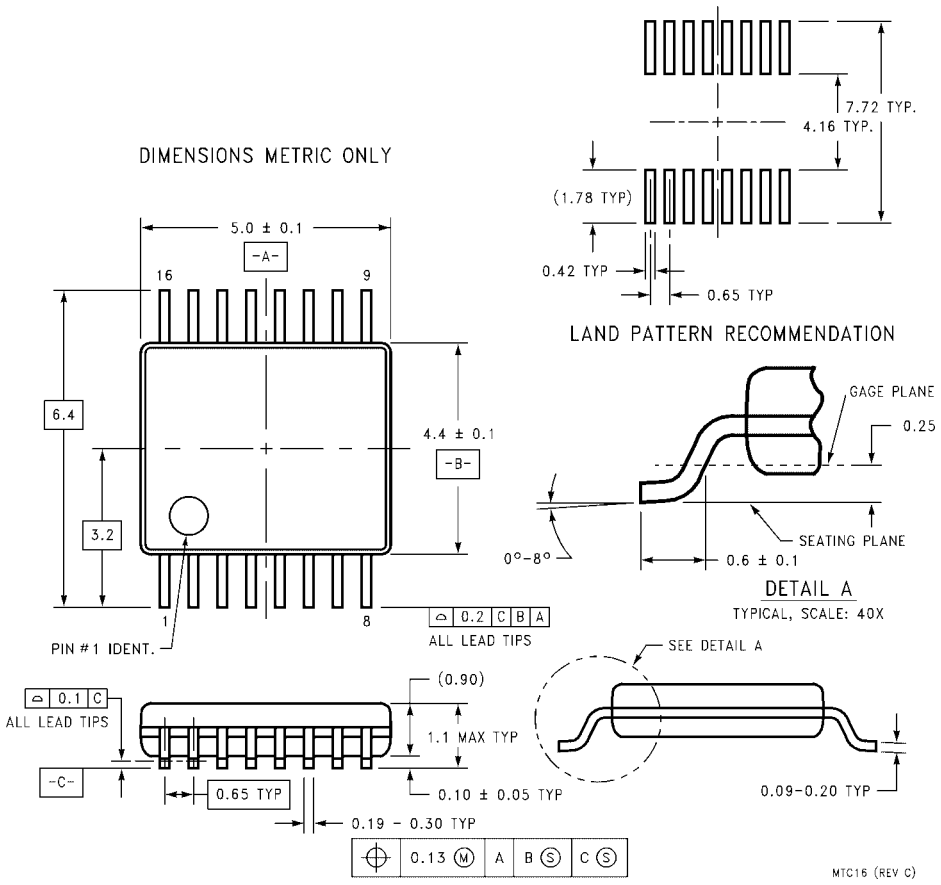
M16DRevB1



DETAIL A

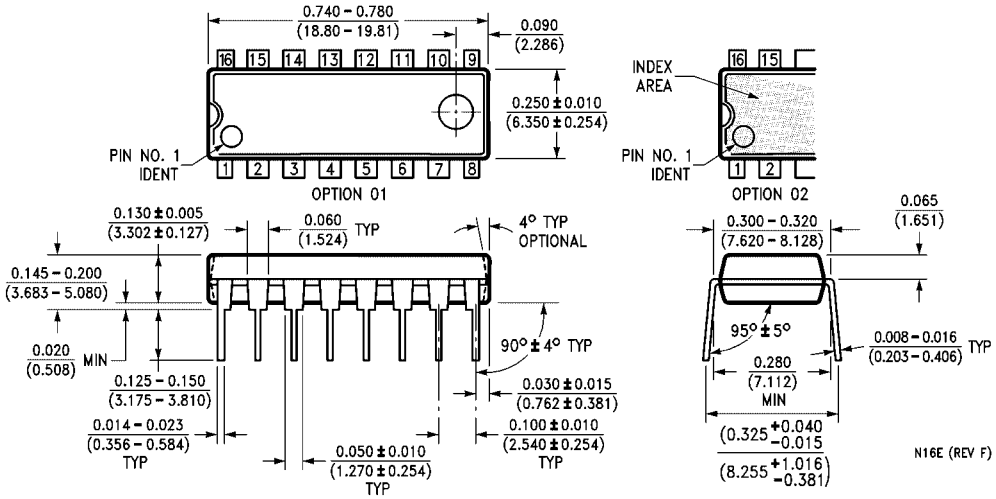
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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