# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

# 74HC/HCT365

## Hex buffer/line driver; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

# Hex buffer/line driver; 3-state 74HC/HCT365

## FEATURES

- Non-inverting outputs
- Output capability: bus driver
- $I_{CC}$ category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT365 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT365 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($\overline{OE}_1$, $\overline{OE}_2$).

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

The “365” is identical to the “366” but has non-inverting outputs.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f$ = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| $t_{PHL}/ t_{PLH}$ | propagation delay nA to nY | $C_L$ = 15 pF; $V_{CC}$ = 5 V | 9 | 11 | ns |
| $C_I$ | input capacitance | | 3,5 | 3,5 | pF |
| $C_{PD}$ | power dissipation capacitance per buffer | notes 1 and 2 | 40 | 40 | pF |

### Notes

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz

   $f_o$ = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   $C_L$ = output load capacitance in pF

   $V_{CC}$ = supply voltage in V

2. For HC the condition is $V_I$ = GND to $V_{CC}$

   For HCT the condition is $V_I$ = GND to $V_{CC}$ − 1.5 V

## ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

**PIN DESCRIPTION**

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 15 | $\overline{OE}_1$, $\overline{OE}_2$ | output enable inputs (active LOW) |
| 2, 4, 6, 10, 12, 14 | 1A to 6A | data inputs |
| 3, 5, 7, 9, 11, 13 | 1Y to 6Y | data outputs |
| 8 | GND | ground (0 V) |
| 16 | $V_{CC}$ | positive supply voltage |

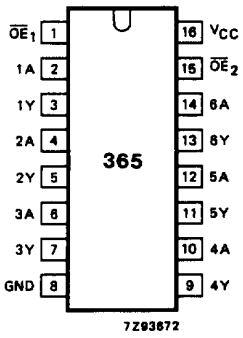



Fig.1 Pin configuration.

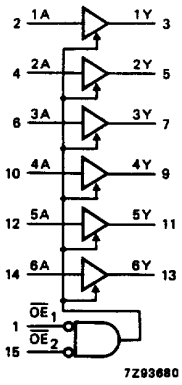



Fig.2

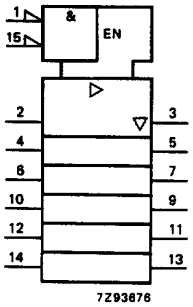



Fig.3 IEC logic symbol.

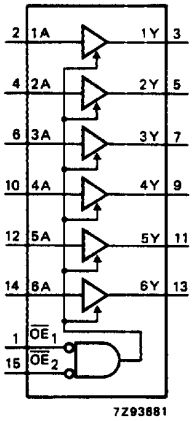



Fig.4 Functional diagram.

**FUNCTION TABLE**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}_1$ | $\overline{OE}_2$ | nA | nY |
| L | L | L | L |
| L | L | H | H |
| X | H | X | Z |
| H | X | X | Z |

**Notes**

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   Z = high impedance OFF-state

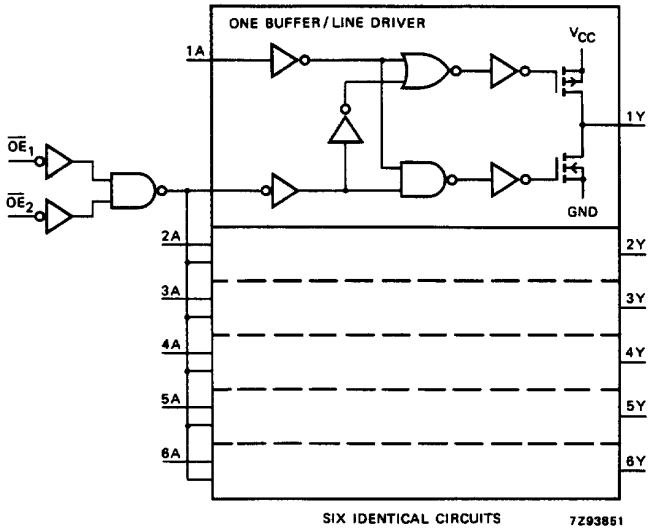



Fig.5 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
$I_{CC}$ category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to+85 | | −40 to+125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay nA to nY | | 30<br>11<br>9 | 95<br>19<br>16 | | 120<br>24<br>20 | | 145<br>29<br>25 | ns | 2.0<br>4.5<br>6.0 | Fig.6 |
| $t_{PZH}$/ $t_{PZL}$ | 3-state output enable time $\overline{OE}_n$ to nY | | 47<br>17<br>14 | 150<br>30<br>26 | | 190<br>38<br>33 | | 225<br>45<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{PHZ}$/ $t_{PLZ}$ | 3-state output disable time $\overline{OE}_n$ to nY | | 61<br>22<br>18 | 150<br>30<br>26 | | 190<br>38<br>33 | | 225<br>45<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{THL}$/ $t_{TLH}$ | output transition time | | 14<br>5<br>4 | 60<br>12<br>10 | | 75<br>15<br>13 | | 90<br>18<br>15 | ns | 2.0<br>4.5<br>6.0 | Fig.6 |

### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
$I_{CC}$ category: MSI

### Note to HCT types

The value of additional quiescent supply current ($\Delta I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

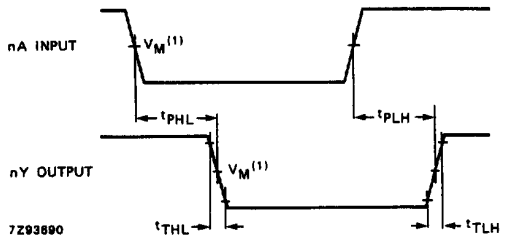
| INPUT | UNIT LOAD COEFFICIENT |
|---|---|
| $\overline{OE}_1$ | 1.00 |
| $\overline{OE}_2$ | 0.90 |
| nA | 1.00 |

### AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

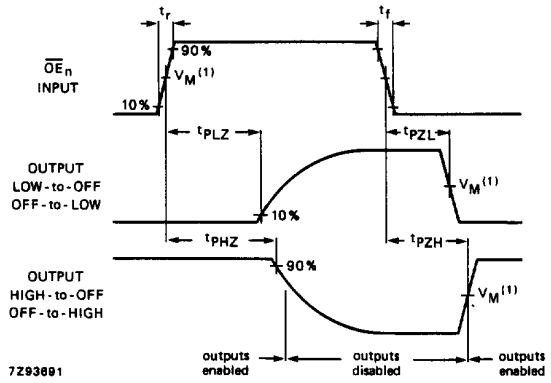
| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | –40 to+85 | | –40 to+125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay nA to nY | | 14 | 25 | | 31 | | 38 | ns | 4.5 | Fig.6 |
| $t_{PZH}/ t_{PZL}$ | 3-state output enable time $\overline{OE}_n$ to nY | | 18 | 35 | | 44 | | 53 | ns | 4.5 | Fig.7 |
| $t_{PHZ}/ t_{PLZ}$ | 3-state output disable time $\overline{OE}_n$ to nY | | 23 | 35 | | 44 | | 53 | ns | 4.5 | Fig.7 |
| $t_{THL}/ t_{TLH}$ | output transition time | | 5 | 12 | | 15 | | 18 | ns | 4.5 | Fig.6 |

## AC WAVEFORMS




(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.




(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.7 Waveforms showing the 3-state enable and disable times.

## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.