FAIRCHILD SEMICONDUCTOR™

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74F899
9-Bit Latchable Transceiver with Parity Generator/Checker

General Description

The 74F899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. It has a guaranteed current sinking capability of 24 mA at the A-bus and 64 mA at the B-bus.

The 74F899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

Features

- Latchable transceiver with output sink of 24 mA at the A-bus and 64 mA at the B-bus
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enables for A-to-B and B-to-A directions
- Select pin for ODD/$\overline{\text{EVEN}}$ parity
- $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ output pins for parity checking
- Ability to simultaneously generate and check parity
- May be used in systems applications in place of the 74F543 and 74F280
- May be used in system applications in place of the 74F657 and 74F373 (no need to change T/$\overline{\text{R}}$ to check parity)

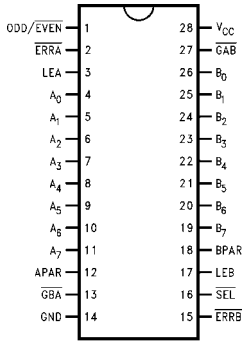
Ordering Code:

Order Number	Package Number	Package Description
74F899SC	M28B	28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F899QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square

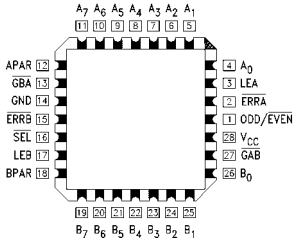
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

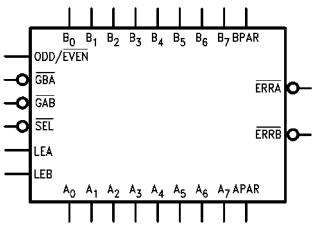
Pin Assignment for SOIC



Pin Assignment for PCC



Logic Symbol



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Input Loading/Fan-Out

Pin Names	Description	HIGH/LOW	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_7	Data Inputs/	1.0/1.0	20 µA/–0.6 mA
	Data Outputs	150/40	–3 mA/24 mA
B_0–B_7	Data Inputs/	1.0/1.0	20 µA/–0.6 mA
	Data Outputs	600/106.6	–12 mA/64 mA
APAR	A Bus Parity	1.0/1.0	20 µA/–0.6 mA
	Input/Output	150/40	–3 mA/24 mA
BPAR	B Bus Parity	1.0/1.0	20 µA/–0.6 mA
	Input/Output	600/106.6	–12 mA/64 mA
ODD/$\overline{\text{EVEN}}$	Parity Select Input	1.0/1.0	20 µA/–0.6 mA
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	Output Enable Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{\text{SEL}}$	Mode Select Input	1.0/1.0	20 µA/–0.6 mA
LEA, LEB	Latch Enable Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error Signal Outputs	50/33.3	–1 mA/20 mA

Pin Descriptions

Pin Names	Description
A_0–A_7	A Bus Data Inputs/Data Outputs
B_0–B_7	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs
ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ Parity Select, Active LOW for EVEN Parity
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	Output Enables for A or B Bus, Active LOW
$\overline{\text{SEL}}$	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

Functional Description

The 74F899 has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select ($\overline{\text{SEL}}$) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by $\overline{\text{ERRB}}$ ($\overline{\text{ERRA}}$).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is HIGH. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table).

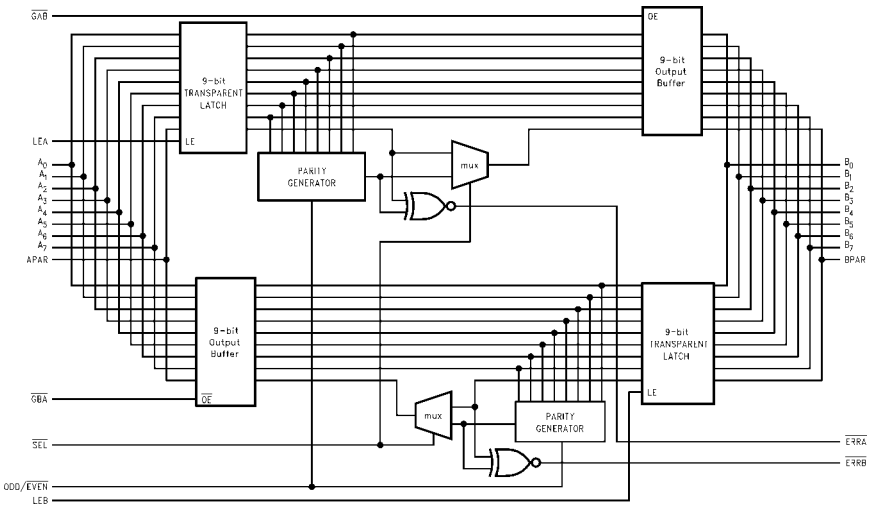
Function Table

Inputs					Operation
$\overline{GAB}$	$\overline{GBA}$	$\overline{SEL}$	LEA	LEB	
H	H	X	X	X	Busses A and B are 3-STATE.
H	L	L	L	H	Generates parity from B[0:7] based on O/$\overline{E}$ (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	L	H	H	Generates parity from B[0:7] based on O/$\overline{E}$. Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$. Generated parity also fed back through the A latch for generate/check as $\overline{ERRA}$.
H	L	L	X	L	Generates parity from B latch data based on O/$\overline{E}$. Generated parity → APAR. Generated parity checked against latched BPAR and output as $\overline{ERRB}$.
H	L	H	X	H	BPAR/B[0:7] → APAR/A0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	H	H	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{ERRB}$. Generated parity also fed back through the A latch for generate/check as $\overline{ERRA}$.
L	H	L	H	L	Generates parity for A[0:7] based on O/$\overline{E}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	L	H	H	Generates parity from A[0:7] based on O/$\overline{E}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$. Generated parity also fed back through the B latch for generate/check as $\overline{ERRB}$.
L	H	L	L	X	Generates parity from A latch data based on O/$\overline{E}$. Generated parity → BPAR. Generated parity checked against latched APAR and output as $\overline{ERRA}$.
L	H	H	H	L	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	H	H	H	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{ERRA}$. Generated parity also fed back through the B latch for generate/check as $\overline{ERRB}$.

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

Note 1: O/$\overline{E}$ = ODD/$\overline{EVEN}$

Functional Block Diagram



Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V		I_{OH} = −1 mA
		10% V_{CC}	2.4					I_{OH} = −3 mA
		10% V_{CC}	2.0					I_{OH} = −15 mA (B_n, BPAR)
		5% V_{CC}	2.7					I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V		I_{OL} = 20 mA (A_n, APAR, $\overline{ERRA}$, $\overline{ERRB}$)
		5% V_{CC}			0.55			I_{OL} = 24 mA (A_n, APAR, $\overline{ERRA}$, $\overline{ERRB}$)
		10% V_{CC}			0.55			I_{OL} = 64 mA (B_n, BPAR)
V_{TH}	Input Threshold Voltage			1.45		V		±0.1V, Sweep Edge Rate must be > 1V/50 ns
V_{OLV}	Negative Ground Bounce Voltage			1.0		V		Observed on “quiet” output during simultaneous switching of remaining outputs
V_{OLP}	Positive Ground Bounce Voltage			1.0		V		Observed on “quiet” output during simultaneous switching of remaining outputs
I_{IL}	Input Low Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V (ODD/$\overline{EVEN}$, $\overline{GBA}$, $\overline{GAB}$, $\overline{SEL}$, LEA, LEB)
I_{BVIT}	Input HIGH Current Breakdown (I/O)				0.5	mA	Max	V_{IN} = 5.5V (A_n, B_n, A_{PAR}, B_{PAR})
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input Low Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{IH+} I_{OZH}	Output Leakage Current				70	µA	Max	$V_{I/O}$ = 2.7V (A_n, B_n, APAR, BPAR)

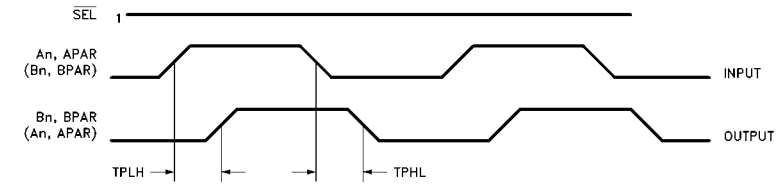
DC Electrical Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
I_{IL+}	Output Leakage			–650	µA	Max	$V_{I/O}$ = 0.5V
I_{OZL}	Current						(A_n, B_n, APAR, BPAR)
I_{OS}	Output Short-Circuit Current	–60		–150	mA	Max	V_{OUT} = 0V
							(A_n, APAR, $\overline{ERRA}$, $\overline{ERRB}$)
		–100		–225		Max	V_{OUT} = 0V (B_n, BPAR)
I_{ZZ}	Bus Drainage Test			500	µA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		132	155	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		178	210	mA	Max	V_O = LOW, GAB = LOW,
							GBA = HIGH, V_{IL} = LOW
I_{CCZ}	Power Supply Current		160	190	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

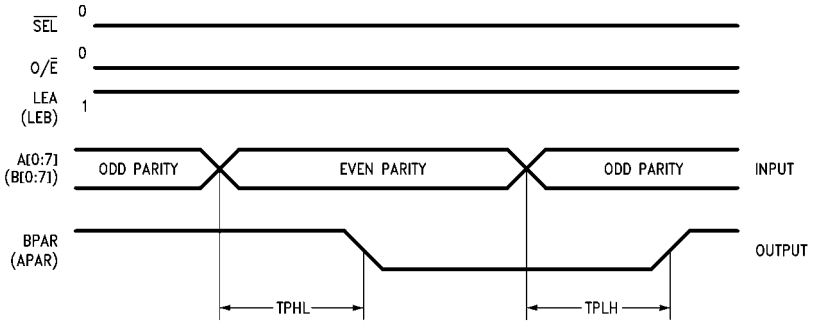
Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = 0°C to +70°C, V_{CC} = +5.0V, C_L = 50 pF		Units	Figure Number
		Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	4.0	7.5	13.0	4.0	14.0	ns	Figure 1
t_{PHL}	A_n, APAR to B_n, BPAR	4.0	8.5	13.0	4.0	14.0		
t_{PLH}	Propagation Delay	7.5	12.0	17.0	7.5	18.0	ns	Figure 2
t_{PHL}	A_n, B_n to BPAR, APAR	7.5	12.5	17.0	7.5	18.0		
t_{PLH}	Propagation Delay	7.5	12.0	17.0	7.5	18.0	ns	Figure 3
t_{PHL}	A_n, B_n to $\overline{ERRA}$, $\overline{ERRB}$	7.5	12.5	17.0	7.5	18.0		
t_{PLH}	Propagation Delay	4.5	7.5	11.0	4.5	12.0	ns	Figure 4
t_{PHL}	ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$	4.5	8.0	11.0	4.5	12.0		
t_{PLH}	Propagation Delay	4.5	7.5	11.5	4.5	12.5	ns	Figure 5
t_{PHL}	ODD/$\overline{EVEN}$ to APAR, BPAR	4.5	8.5	11.5	4.5	12.5		
t_{PLH}	Propagation Delay	5.5	9.0	13.0	5.5	14.0	ns	Figure 6
t_{PHL}	APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$	5.5	9.5	13.0	5.5	14.0		
t_{PLH}	LEA/LEB to	9.5	13.0	17.5	7.5	18.0	ns	Figure 7
t_{PHL}	$\overline{ERRA}$ /$\overline{ERRB}$	9.7		17.5	7.5	18.0		
t_{PLH}	Propagation Delay	3.0	6.0	10.0	3.0	11.0	ns	Figure 10
t_{PHL}	$\overline{SEL}$ to APAR, BPAR	3.0	7.0	10.0	3.0	11.0		
t_{PLH}	Propagation Delay	3.5	7.0	10.0	3.5	11.0	ns	Figure 11
t_{PHL}	LEB to A_n, APAR	3.5	8.0	10.0	3.5	11.0		
t_{PLH}	Propagation Delay	3.5	6.5	10.0	3.5	11.0	ns	Figure 11
t_{PHL}	LEA to B_n, BPAR	3.5	7.5	10.0	3.5	11.0		
t_{PZH}	Output Enable Time	1.0	4.5	10.0	1.0	11.0	ns	Figure 8, Figure 9
t_{PZL}	$\overline{GBA}$ or $\overline{GAB}$ to A_n,	1.0	6.5	10.0	1.0	11.0		
	APAR or B_n, BPAR							
t_{PHZ}	Output Disable Time	1.0	4.0	7.0	1.0	8.0	ns	Figure 8, Figure 9
t_{PLZ}	$\overline{GBA}$ or $\overline{GAB}$ to A_n,	1.0	4.0	7.0	1.0	8.0		
	APAR or B_n, BPAR							
t_S(H)	Setup Time, HIGH or LOW	5.0	1.6		5.0		ns	Figure 12, Figure 13
t_S(L)	A_n, B_n to LEA, LEB	5.0	1.8		5.0			
t_H(H)	Hold Time, HIGH or LOW	0	–1.7		0		ns	Figure 12, Figure 13
t_H(L)	A_n, B_n to LEA, LEB	0	–1.5		0			
t_W	Pulse Width for LEA, LEB	6.0	2.0		6.0		ns	Figure 14

AC Path



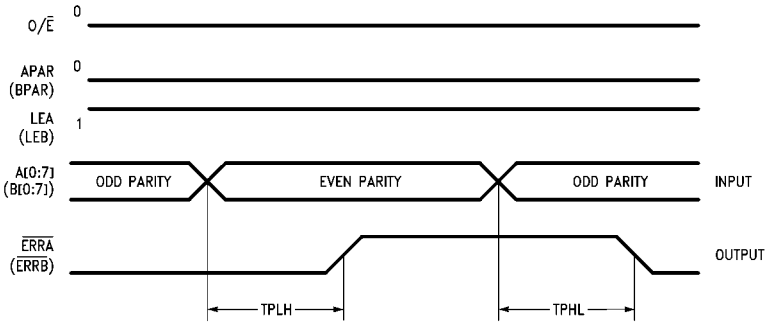
A_n, APAR → B_n, BPAR
(B_n, BPAR → A_n, APAR)

FIGURE 1.



A_n → BPAR
(B_n → APAR)

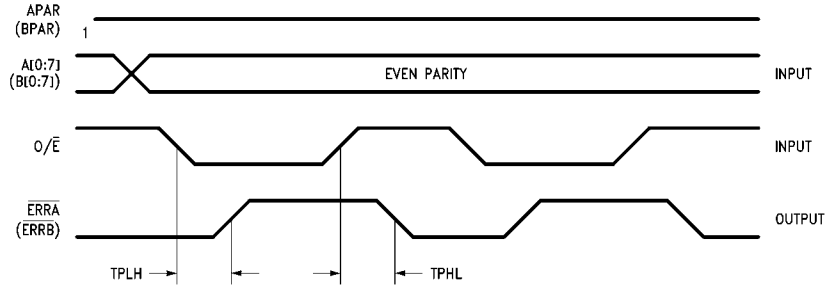
FIGURE 2.



A_n → $\overline{ERRA}$
(B_n → $\overline{ERRB}$)

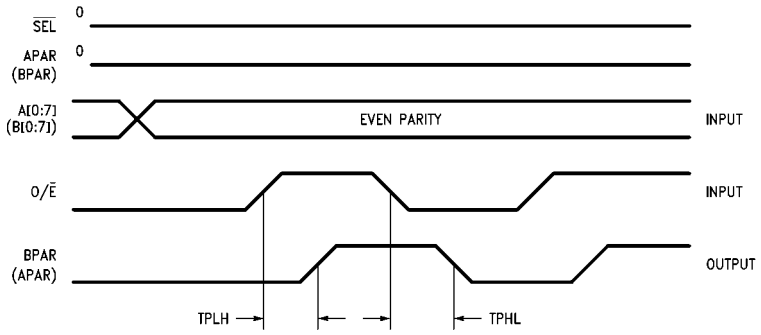
FIGURE 3.

AC Path (Continued)



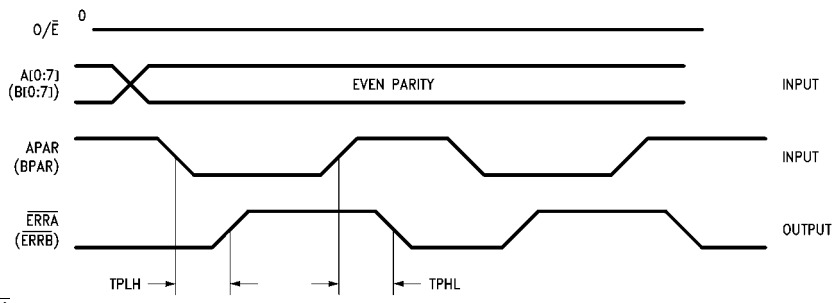
O/$\overline{E}$ → $\overline{ERRA}$
O/$\overline{E}$ → $\overline{ERRB}$

FIGURE 4.



O/$\overline{E}$ → BPAR
(O/$\overline{E}$ → APAR)

FIGURE 5.



APAR → $\overline{ERRA}$
(BPAR → $\overline{ERRB}$)

FIGURE 6.

AC Path (Continued)

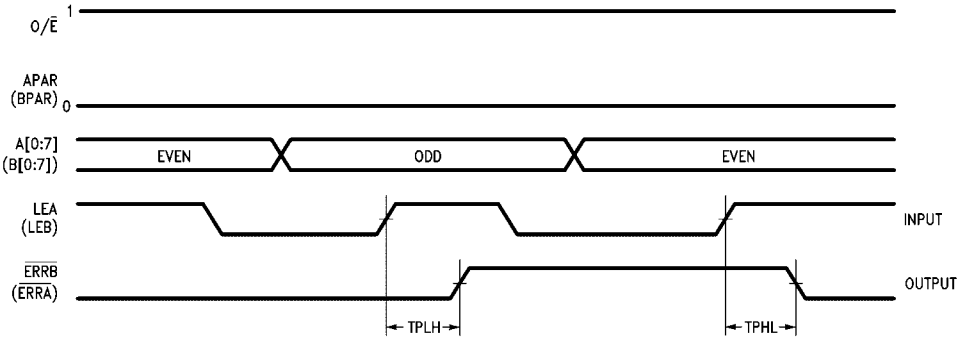
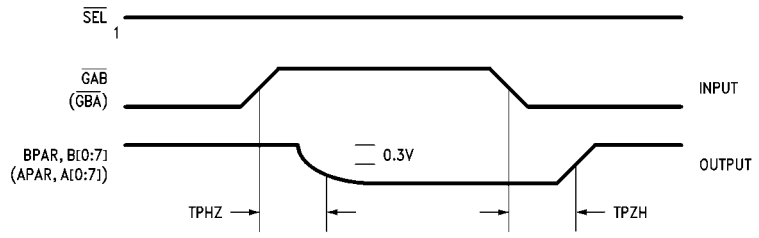
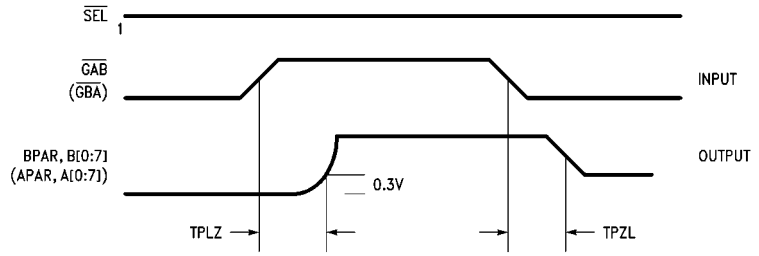


FIGURE 7.



ZH, HZ

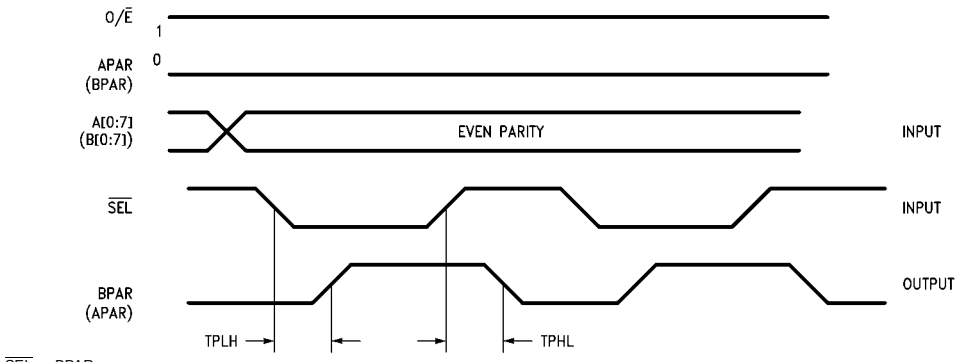
FIGURE 8.



ZL, LZ

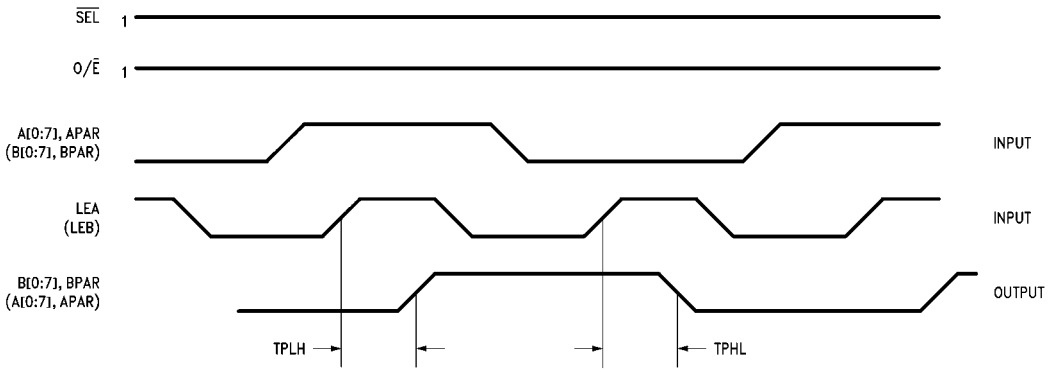
FIGURE 9.

AC Path (Continued)



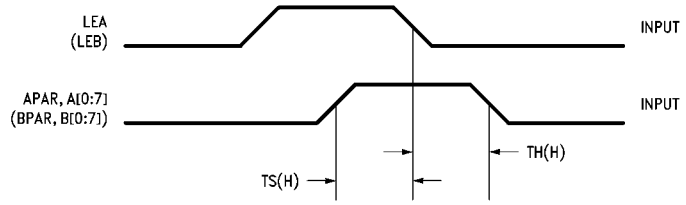
SEL → BPAR
(SEL → APAR)

FIGURE 10.



LEA → BPAR, B[0:7]
(LEB → APAR, A[0:7])

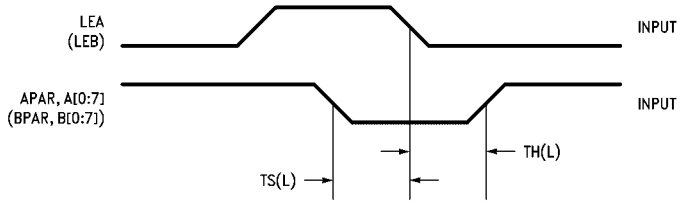
FIGURE 11.



TS(H), TH(H)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

FIGURE 12.

AC Path (Continued)



TS(L), TH(L)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

FIGURE 13.

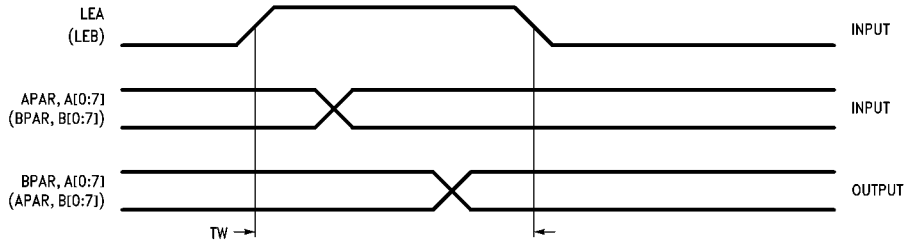
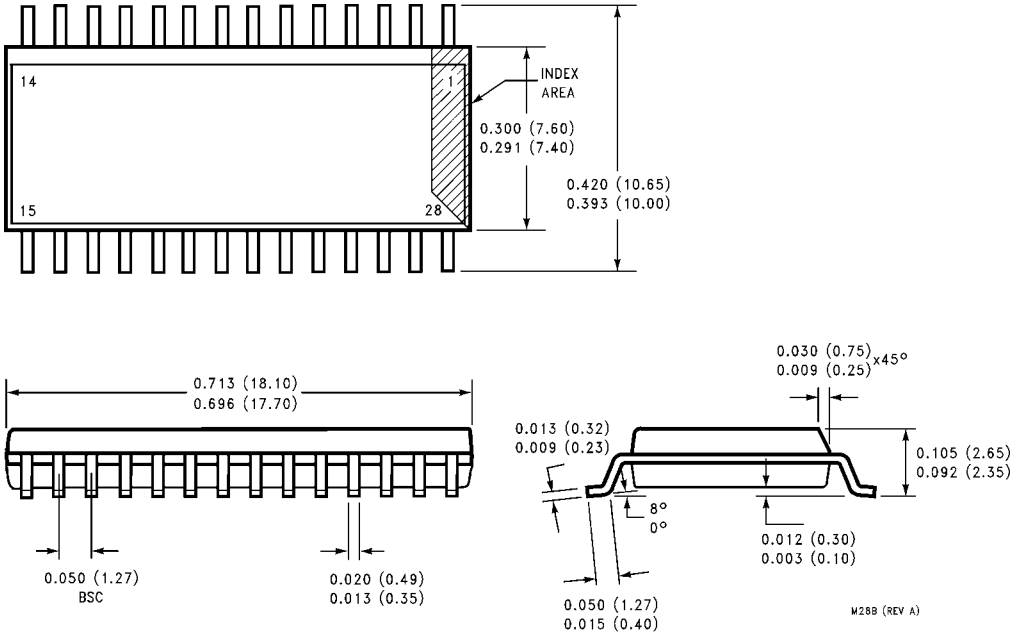


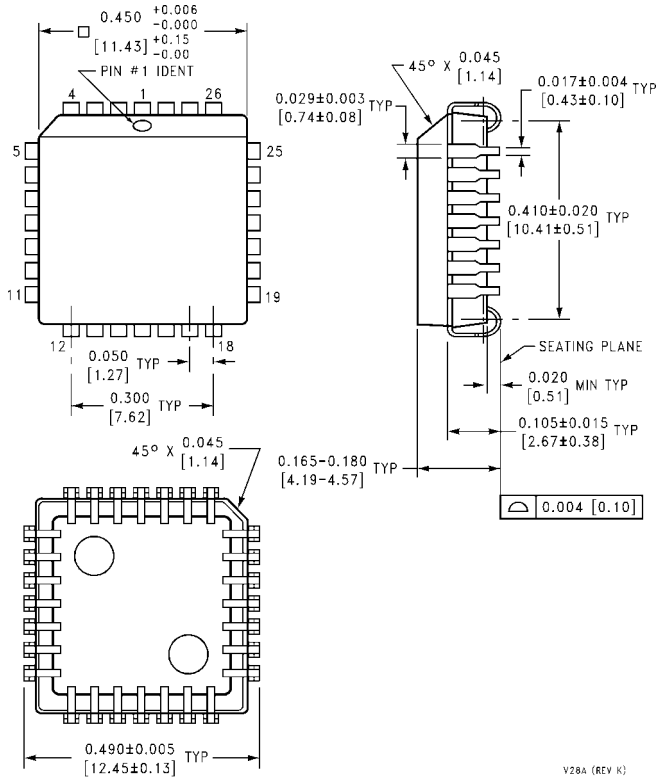
FIGURE 14.

Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M28B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A

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LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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