FAIRCHILD SEMICONDUCTOR™

April 1988
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74F182
Carry Lookahead Generator

General Description

The 74F182 is a high-speed carry lookahead generator. It is generally used with the 74F181 or 74F381 4-bit arithmetic logic units to provide high-speed lookahead over word lengths of more than four bits.

Features

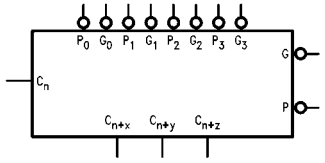
- Provides lookahead carries across a group of four ALUs
- Multi-level lookahead high-speed arithmetic operation over long word lengths

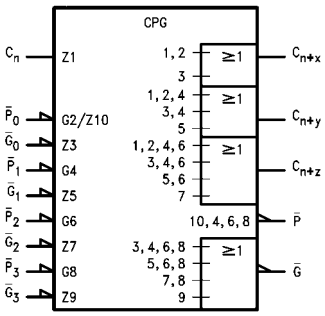
Ordering Code:

Order Number	Package Number	Package Description
74F182SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F182PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

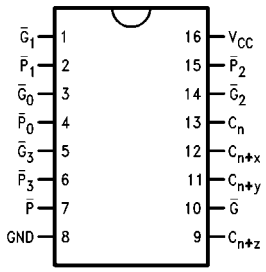
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols





Connection Diagram



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Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
C_n	Carry Input	1.0/2.0	20 µA/–1.2 mA
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)	1.0/14.0	20 µA/–8.4 mA
$\overline{G}_1$	Carry Generate Input (Active LOW)	1.0/16.0	20 µA/–9.6 mA
$\overline{G}_3$	Carry Generate Input (Active LOW)	1.0/8.0	20 µA/–4.8 mA
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)	1.0/8.0	20 µA/–4.8 mA
$\overline{P}_2$	Carry Propagate Input (Active LOW)	1.0/6.0	20 µA/–3.6 mA
$\overline{P}_3$	Carry Propagate Input (Active LOW)	1.0/4.0	20 µA/–2.4 mA
$C_{n+x} - C_{n+z}$	Carry Outputs	50/33.3	–1 mA/20 mA
$\overline{G}$	Carry Generate Output (Active LOW)	50/33.3	–1 mA/20 mA
$\overline{P}$	Carry Propagate Output (Active LOW)	50/33.3	–1 mA/20 mA

Functional Description

The 74F182 carry lookahead generator accepts up to four pairs of Active LOW Carry Propagate ($\overline{P}_0$–$\overline{P}_3$) and Carry Generate ($\overline{G}_0$–$\overline{G}_3$) signals and an Active HIGH Carry input (C_n) and provides anticipated Active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 74F182 also has Active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead. The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

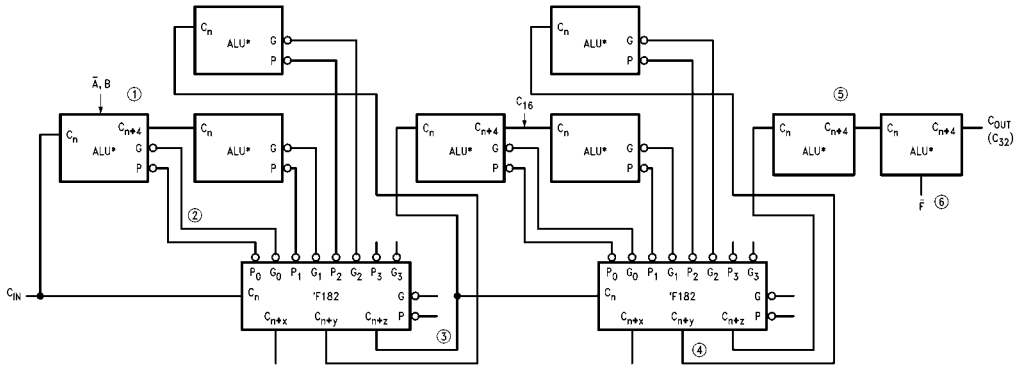
$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

$$G = \overline{G}_3 + \overline{P}_3 \overline{G}_2 + \overline{P}_3 \overline{P}_2 \overline{G}_1 + \overline{P}_3 \overline{P}_2 \overline{P}_1 \overline{G}_0$$

$$P = \overline{P}_2 \overline{P}_2 \overline{P}_1 \overline{P}_0$$

Also, the 74F182 can be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections (Figure 1) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last 74F181 or 74F381.



*ALUs may be either 74F181 or 74F381

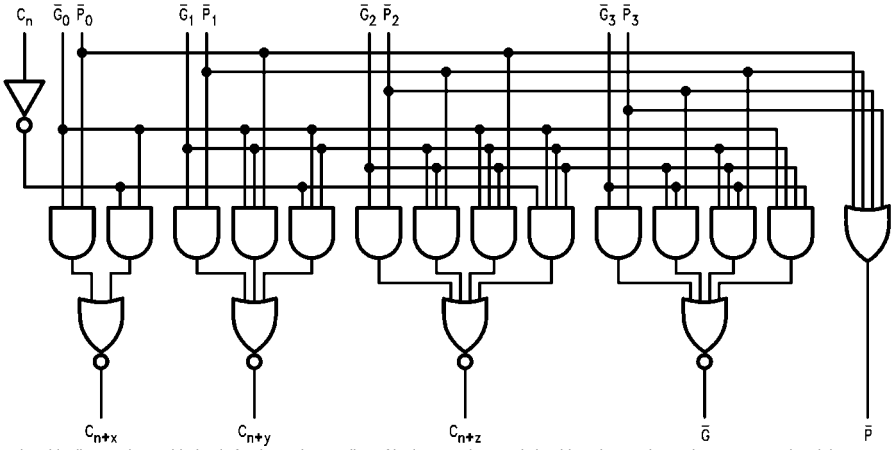
FIGURE 1. 32-Bit ALU with Rippled Carry between 16-Bit Lookahead ALUs

Truth Table

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

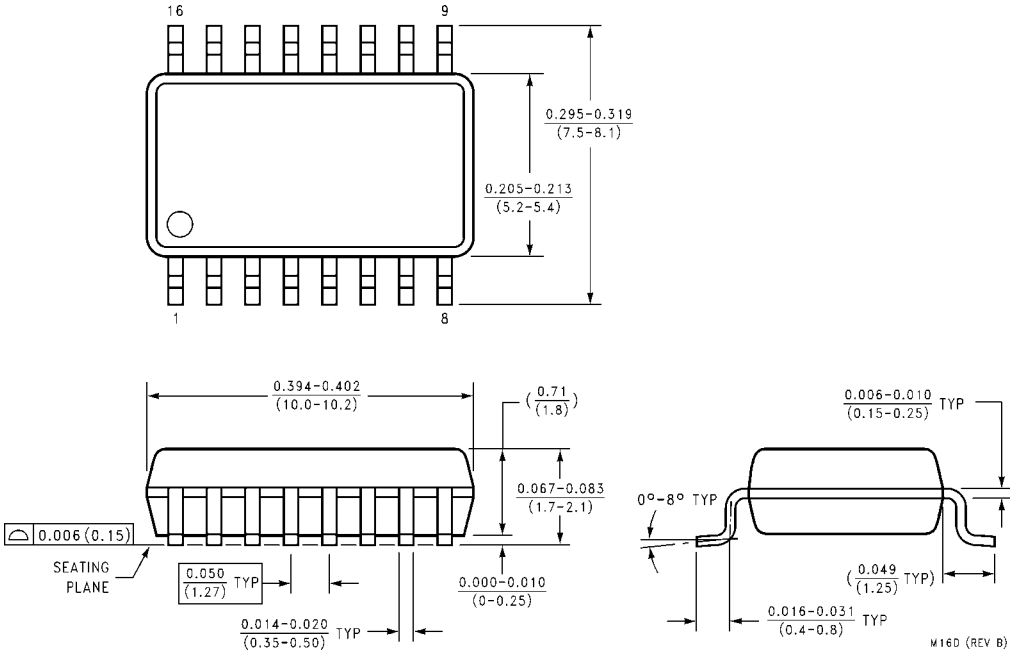
DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−1.2	mA	Max	V_{IN} = 0.5V (C_n)
					−2.4			V_{IN} = 0.5V ($\overline{P}_3$)
					−3.6			V_{IN} = 0.5V ($\overline{P}_2$)
					−4.8			V_{IN} = 0.5V ($\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$)
					−8.4			V_{IN} = 0.5V ($\overline{G}_0$, $\overline{G}_2$)
					−9.6			V_{IN} = 0.5V ($\overline{G}_1$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			18.4	28.0	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			23.5	36.0	mA	Max	V_O = LOW

AC Electrical Characteristics

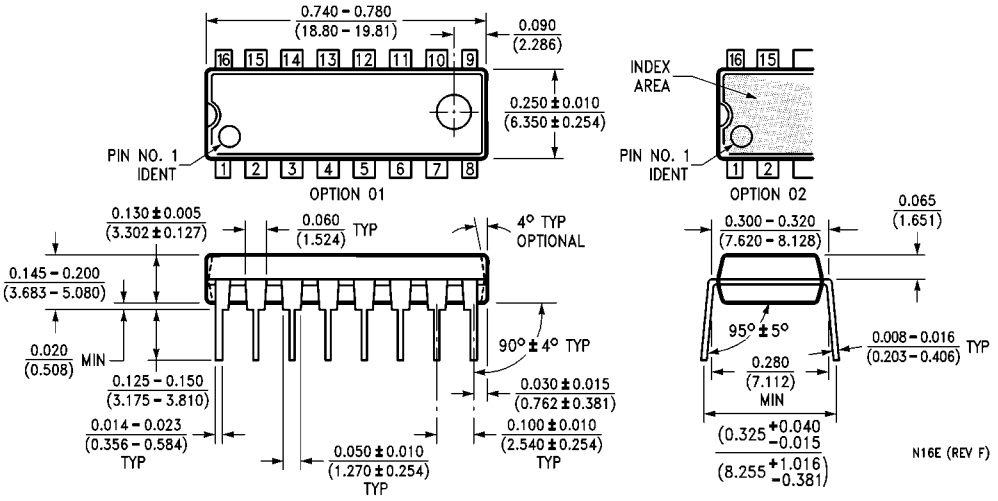
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0	6.6	8.5	3.0	12.0	3.0	9.5	ns
t_{PHL}	C_n to C_{n+x}, C_{n+y}, C_{n+z}	3.0	6.8	9.0	3.0	11.0	3.0	10.0	
t_{PLH}	Propagation Delay	2.5	6.2	8.0	2.5	11.0	2.5	9.0	ns
t_{PHL}	$\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$ to	1.5	3.7	5.0	1.0	7.0	1.5	6.0	
	C_{n+x}, C_{n+y}, or C_{n+z}								
t_{PLH}	Propagation Delay	2.5	6.5	8.5	2.5	11.0	2.5	9.5	ns
t_{PHL}	$\overline{G}_0$, $\overline{G}_1$, or $\overline{G}_2$ to	1.5	3.9	5.2	1.0	7.0	1.5	6.0	
	C_{n+x}, C_{n+y}, or C_{n+z}								
t_{PLH}	Propagation Delay	3.0	7.9	10.0	3.0	12.0	3.0	11.0	ns
t_{PHL}	$\overline{P}_1$, $\overline{P}_2$, or $\overline{P}_3$ to $\overline{G}$	3.0	6.0	8.0	2.5	10.0	3.0	9.0	
t_{PLH}	Propagation Delay	3.0	8.3	10.5	3.0	12.0	3.0	11.5	ns
t_{PHL}	$\overline{G}_n$ to $\overline{G}$	3.0	5.7	7.5	2.5	10.0	3.0	8.5	
t_{PLH}	Propagation Delay	3.0	5.7	7.5	2.5	10.0	3.0	8.5	ns
t_{PHL}	$\overline{P}_n$ to $\overline{P}$	2.5	4.1	5.5	2.5	8.0	2.5	6.5	

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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