FAIRCHILD SEMICONDUCTOR®

April 2007

74F161A, 74F163A
Synchronous Presettable Binary Counter

Features

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count frequency of 120MHz

General Description

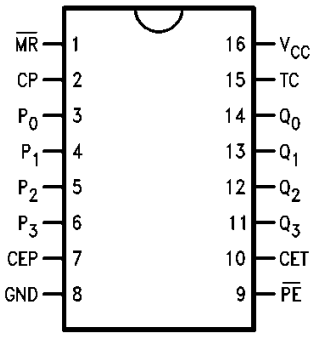
The 74F161A and 74F163A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multi-stage counters. The 74F161A has an asynchronous Master-Reset input that overrides all other inputs and forces the outputs LOW. The 74F163A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The 74F161A and 74F163A are high-speed versions of the 74F161 and 74F163.

Ordering Information

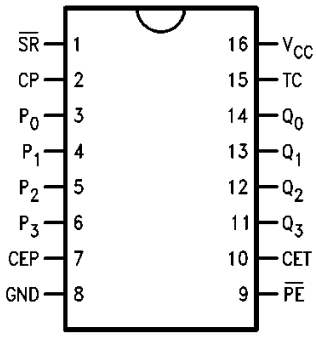
Order Number	Package Number	Package Description
74F161ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F161ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F161APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74F163ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F163ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F163APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

Connection Diagrams



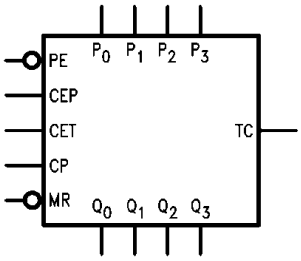
74F161A



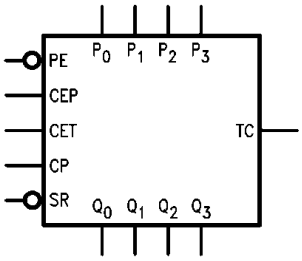
74F163A

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Logic Symbols

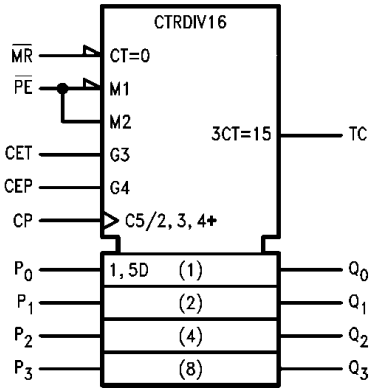


74F161A



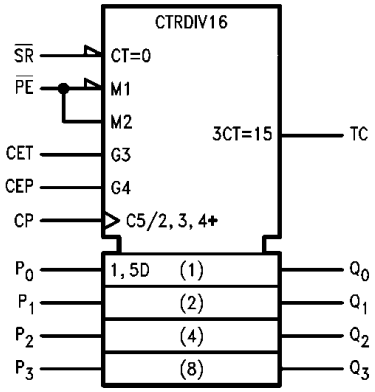
74F163A

IEEE/IEC



74F161A

IEEE/IEC



74F163A

Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH / LOW	Input I_{IH} / I_{IL} Output I_{OH} / I_{OL}
CEP	Count Enable Parallel Input	1.0 / 1.0	20µA / -0.6mA
CET	Count Enable Trickle Input	1.0 / 2.0	20µA / -1.2mA
CP	Clock Pulse Input (Active Rising Edge)	1.0 / 1.0	20µA / -0.6 mA
$\overline{MR}$ (74F161A)	Asynchronous Master Reset Input (Active LOW)	1.0 / 1.0	20µA / -0.6 mA
$\overline{SR}$ (74F163A)	Synchronous Reset Input (Active LOW)	1.0 / 2.0	20µA / -1.2 mA
P_0–P_3	Parallel Data Inputs	1.0 / 1.0	20µA / -0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0 / 2.0	20µA / -1.2mA
Q_0–Q_3	Flip-Flop Outputs	50 / 33.3	-1mA / 20mA
TC	Terminal Count Output	50 / 33.3	-1mA / 20mA

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Functional Description

The 74F161A and 74F163A count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 74F161A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (74F161A), synchronous reset (74F163A), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, 74F161A), Synchronous Reset ($\overline{SR}$, 74F163A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('F161A) or $\overline{SR}$ (74F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 74F161A and 74F163A use D-type edge triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multi-stage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 74F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations:

Count Enable = CEP • CET • $\overline{PE}$

TC = $Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

Mode Select Table

$\overline{SR}$(1)	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level

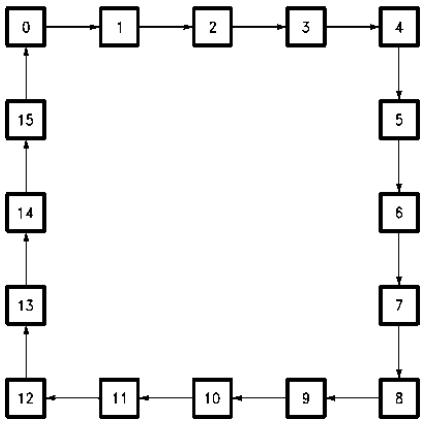
L = LOW Voltage Level

X = Immaterial

Note:

1. For 74F163A only

State Diagram



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Block Diagram

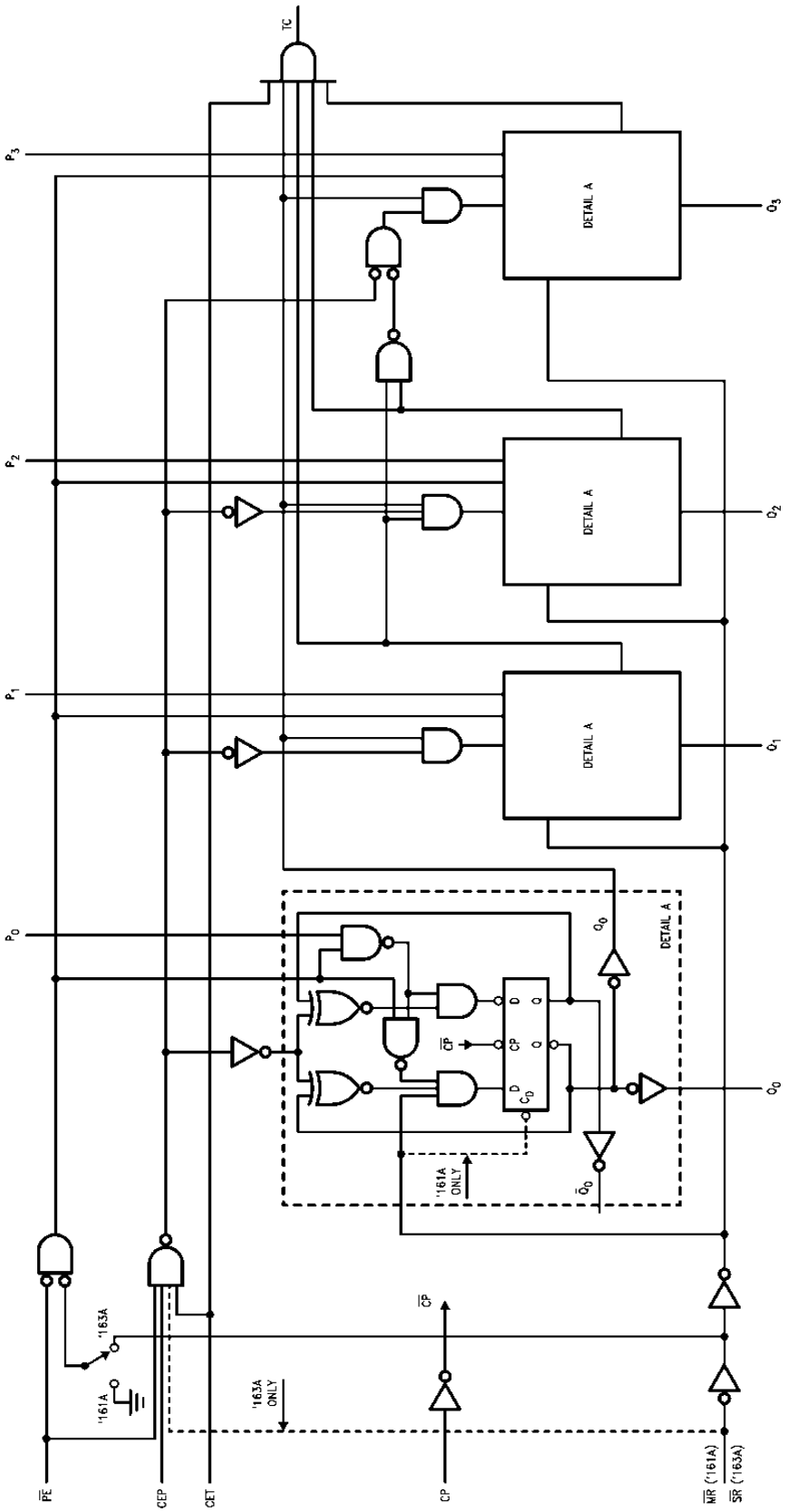


Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T_{STG}	Storage Temperature	–65°C to +150°C
T_A	Ambient Temperature Under Bias	–55°C to +125°C
T_J	Junction Temperature Under Bias	–55°C to +150°C
V_{CC}	V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
V_{IN}	Input Voltage(2)	–0.5V to +7.0V
I_{IN}	Input Current(2)	–30mA to +5.0mA
V_O	Voltage Applied to Output in HIGH State (with V_{CC} = 0V) Standard Output 3-STATE Output	 –0.5V to V_{CC} –0.5V to +5.5V
	Current Applied to Output in LOW State (Max.)	twice the rated I_{OL} (mA)
	ESD Last Passing Voltage (Min.)	4000V

Note:

2. Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T_A	Free Air Ambient Temperature	0°C to +70°C
V_{CC}	Supply Voltage	+4.5V to +5.5V

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DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		Recognized as a HIGH Signal	2.0			V
V_{IL}	Input LOW Voltage		Recognized as a LOW Signal			0.8	V
V_{CD}	Input Clamp Diode Voltage	Min.	I_{IN} = –18mA			–1.2	V
V_{OH}	Output HIGH Voltage 10% V_{CC}	Min.		2.5			V
	Output HIGH Voltage 5% V_{CC}			2.7			
V_{OL}	Output LOW Voltage 10% V_{CC}	Min.	I_{OL} = 20mA			0.5	V
I_{IH}	Input HIGH Current	Max.	V_{IN} = 2.7V			5.0	µA
I_{BVI}	Input HIGH Current Breakdown Test	Max.	V_{IN} = 7.0V			7.0	µA
I_{CEX}	Output HIGH Leakage Current	Max.	V_{OUT} = V_{CC}			50	µA
V_{ID}	Input Leakage Test	0.0	I_{ID} = 1.9µA, All Other Pins Grounded	4.75			V
I_{OD}	Output Leakage Circuit Current	0.0	V_{IOD} = 150mV, All Other Pins Grounded			3.75	µA
I_{IL}	Input LOW Current	Max.	V_{IN} = 0.5V (CEP, CP, $\overline{MR}$, P_0–P_3)			–0.6	mA
			V_{IN} = 0.5V (CET, $\overline{PE}$, $\overline{SR}$)			–1.2	
I_{OS}	Output Short-Circuit Current	Max.	V_{OUT} = 0.0V	–60		–150	mA
I_{CC}	Power Supply Voltage	Max.			37	55	mA

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AC Electrical Characteristics

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF			T_A = –55°C to +125°C, V_{CC} = +5.0V, C_L = 50pF		T_A = 0°C to 70°C, V_{CC} = +5.0V, C_L = 50pF		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Count Frequency		100						MHz
t_{PLH}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH)	3.5	5.5	7.5	3.5	9.0	3.5	8.5	ns
t_{PHL}		3.5	7.5	10.0	3.5	11.5	3.5	11.0	
t_{PLH}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input LOW)	4.0	6.0	8.5	4.0	10.0	4.0	9.5	ns
t_{PHL}		4.0	6.0	8.5	4.0	10.0	4.0	9.5	
t_{PLH}	Propagation Delay, CP to TC	5.0	10.0	14.0	5.0	16.5	5.0	15.0	ns
t_{PHL}		5.0	10.0	14.0	5.0	15.5	5.0	15.0	
t_{PLH}	Propagation Delay, CET to TC	2.5	4.5	7.5	2.5	9.0	2.5	8.5	ns
t_{PHL}		2.5	4.5	7.5	2.5	9.0	2.5	8.5	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n (74F161A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns
t_{PHL}	Propagation Delay, $\overline{MR}$ to TC (74F161A)	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns

AC Operating Requirements

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V		T_A = –55°C to +125°C, V_{CC} = +5.0V		T_A = 0°C to 70°C, V_{CC} = +5.0V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_S(H)$	Setup Time, HIGH or LOW, P_n to CP	5.0		5.5		5.0		ns
$t_S(L)$		5.0		5.5		5.0		
$t_H(H)$	Hold Time, HIGH or LOW, P_n to CP	2.0		2.5		2.0		ns
$t_H(L)$		2.0		2.5		2.0		
$t_S(H)$	Setup Time, HIGH or LOW, $\overline{PE}$ or $\overline{SR}$ to CP	11.0		13.5		11.5		ns
$t_S(L)$		8.5		10.5		9.5		
$t_H(H)$	Hold Time, HIGH or LOW, $\overline{PE}$ or $\overline{SR}$ to CP	2.0		3.6		2.0		ns
$t_H(L)$		0		0		0		
$t_S(H)$	Setup Time, HIGH or LOW, CEP or CET to CP	11.0		13.0		11.5		ns
$t_S(L)$		5.0		6.0		5.0		
$t_H(H)$	Hold Time, HIGH or LOW, CEP or CET to CP	0		0		0		ns
$t_H(L)$		0		0		0		
$t_W(H)$	Clock Pulse Width (Load), HIGH or LOW	5.0		5.0		5.0		ns
$t_W(L)$		5.0		5.0		5.0		
$t_W(H)$	Clock Pulse Width (Count), HIGH or LOW	4.0		5.0		4.0		ns
$t_W(L)$		6.0		8.0		7.0		
$t_W(L)$	$\overline{MR}$ Pulse Width, LOW (74F161A)	5.0		5.0		5.0		ns
t_{REC}	Recovery Time, $\overline{MR}$ to CP (74F161A)	6.0		6.0		6.0		ns

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Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

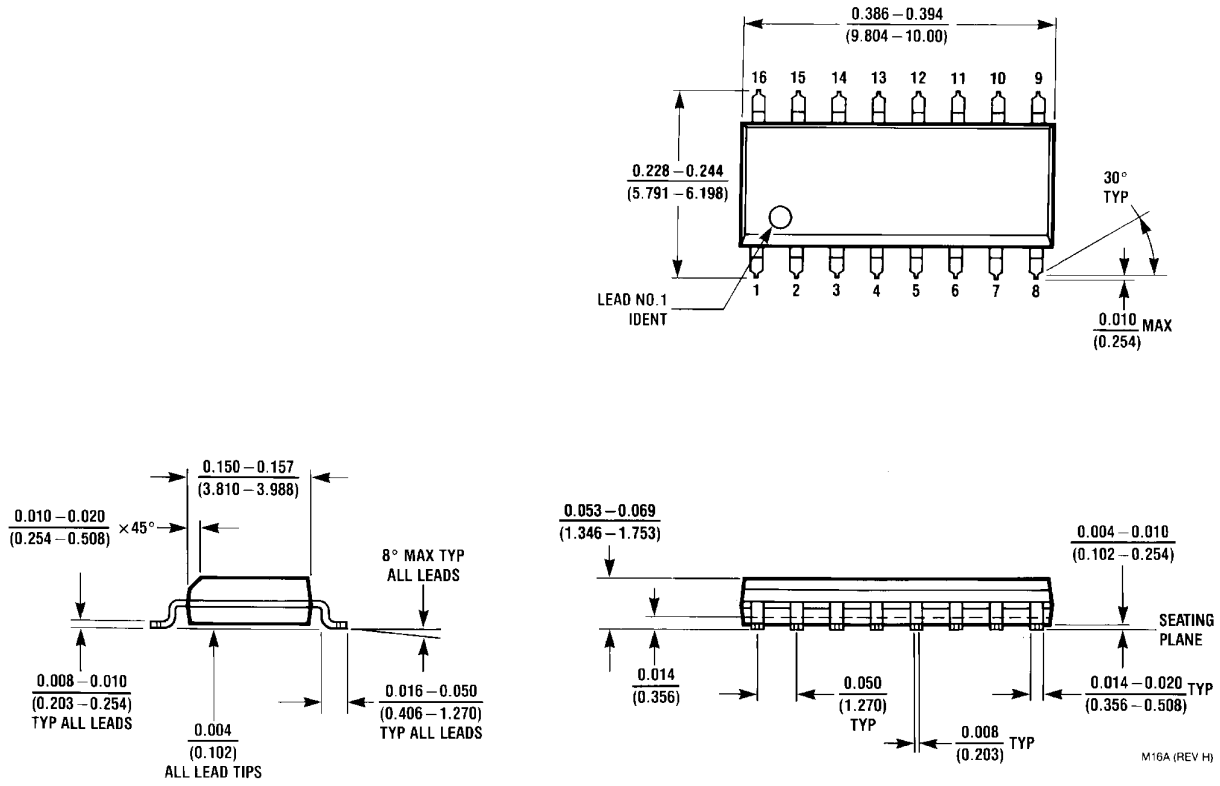
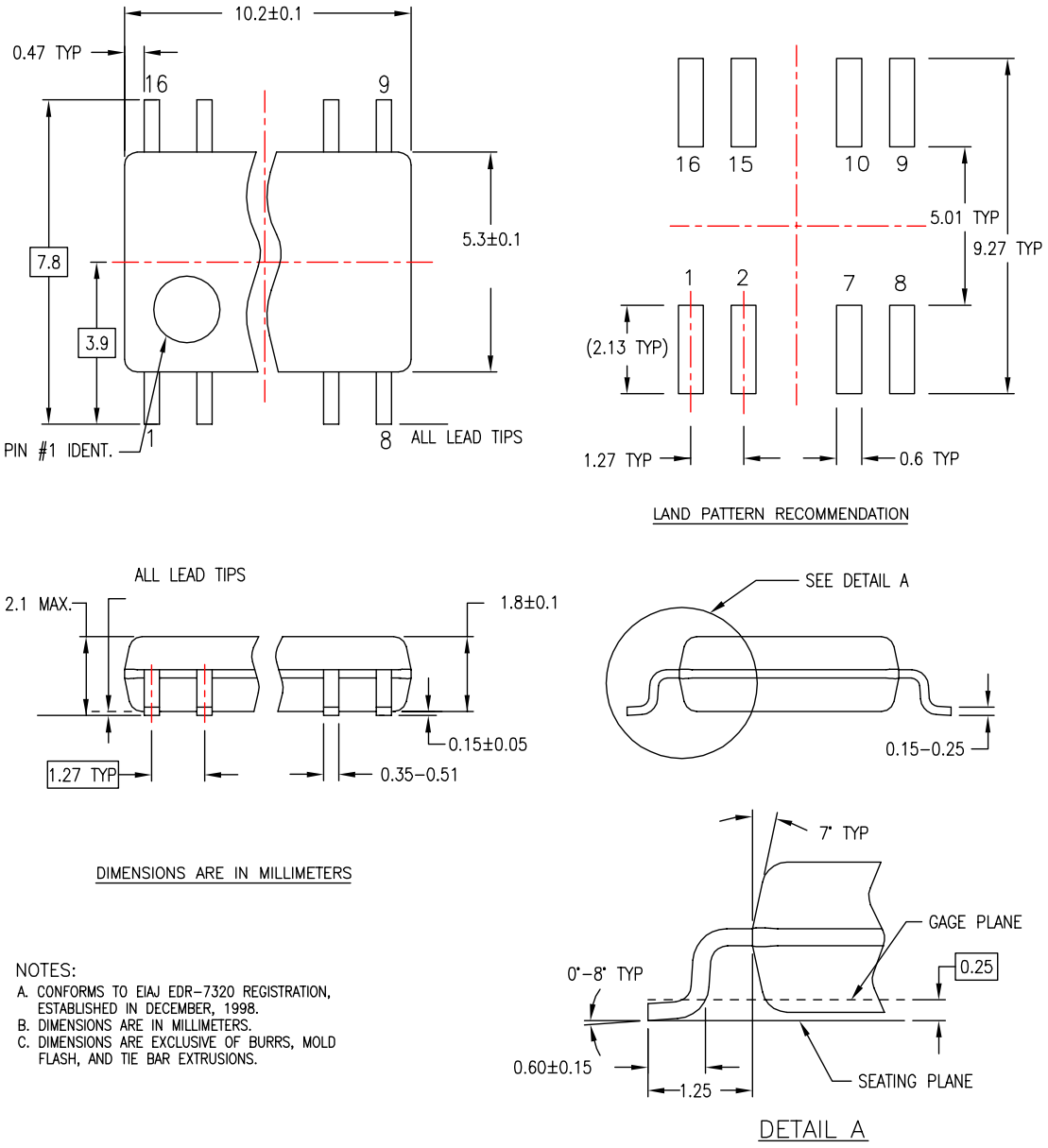


Figure 2. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DREVC

Figure 3. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

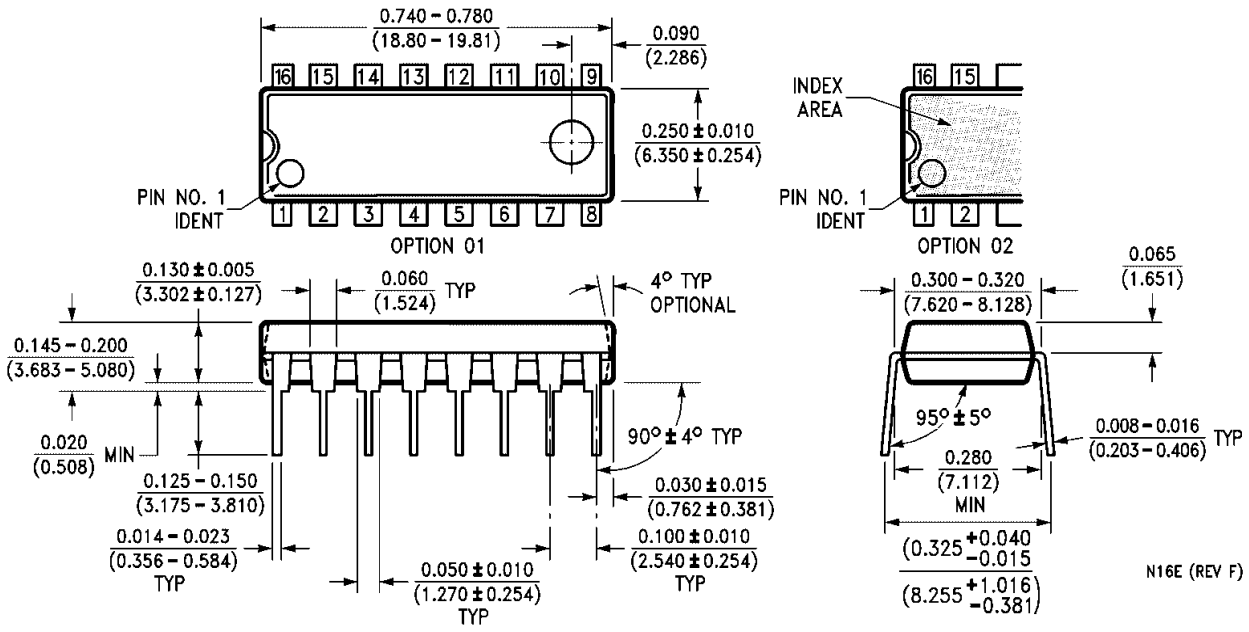


Figure 4. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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