# 74AUP2G38

## Low-power dual 2-input NAND gate (open-drain)

Rev. 01 — 16 October 2006 Product data sheet

## 1. General description

The 74AUP2G38 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire $V_{CC}$ range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire $V_{CC}$ range from 0.8 V to 3.6 V.

This device is fully specified for partial Power-down applications using $I_{OFF}$.
The $I_{OFF}$ circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74AUP2G38 provides the dual 2-input NAND gate with open-drain output. The output of the device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

## 2. Features

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114-D Class 3A exceeds 5000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101-C exceeds 1000 V
- Low static power consumption; $I_{CC}$ = 0.9 µA (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of $V_{CC}$
- $I_{OFF}$ circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

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## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74AUP2G38DC | –40 °C to +125 °C | VSSOP8 | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm | SOT765-1 |
| 74AUP2G38GT | –40 °C to +125 °C | XSON8 | plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm | SOT833-1 |
| 74AUP2G38GM | –40 °C to +125 °C | XQFN8 | plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm | SOT902-1 |

## 4. Marking

**Table 2. Marking**

| Type number | Marking code |
|---|---|
| 74AUP2G38DC | a38 |
| 74AUP2G38GT | a38 |
| 74AUP2G38GM | a38 |

## 5. Functional diagram

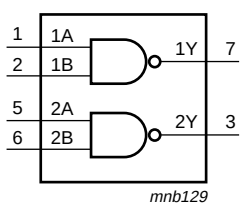



**Fig 1. Logic symbol**

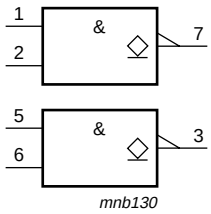



**Fig 2. IEC logic symbol**

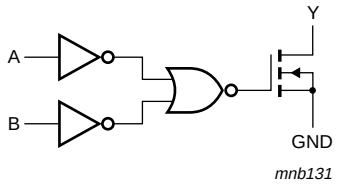



**Fig 3. Logic diagram (one gate)**

## 6. Pinning information

### 6.1 Pinning

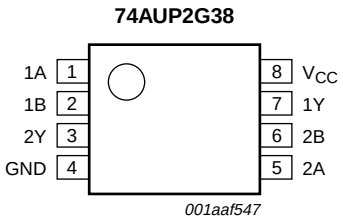
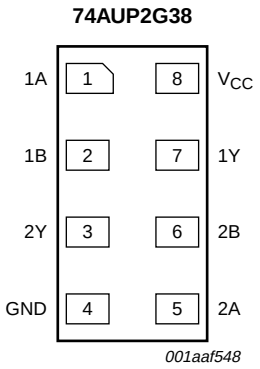



**Fig 4. Pin configuration SOT765-1 (VSSOP8)**

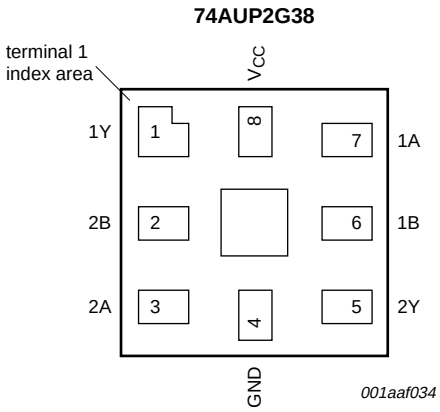


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Transparent top view

**Fig 5. Pin configuration SOT833-1 (XSON8)**




Transparent top view

**Fig 6. Pin configuration SOT902-1 (XQFN8)**

## 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | | Description |
|---|---|---|---|
| | SOT765-1 and SOT833-1 | SOT902-1 | |
| 1A | 1 | 7 | data input 1A |
| 1B | 2 | 6 | data input 1B |
| 2Y | 3 | 5 | data output 2Y |
| GND | 4 | 4 | ground (0 V) |
| 2A | 5 | 3 | data input 2A |
| 2B | 6 | 2 | data input 2B |
| 1Y | 7 | 1 | data output 1Y |
| $V_{CC}$ | 8 | 8 | supply voltage |

# 7. Functional description

**Table 4. Function table[1]**

| Input | | Output |
|---|---|---|
| nA | nB | nY |
| L | L | Z |
| L | H | Z |
| H | L | Z |
| H | H | L |

[1] H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF state.


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## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +4.6 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | - | –50 | mA |
| $V_I$ | input voltage | | [1] | –0.5 | +4.6 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | | - | ±50 | mA |
| $V_O$ | output voltage | Active mode and Power-down mode | [1] | –0.5 | +4.6 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | | - | +20 | mA |
| $I_{CC}$ | supply current | | | - | 50 | mA |
| $I_{GND}$ | ground current | | | - | –50 | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –40 °C to +125 °C | [2] | - | 250 | mW |

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For VSSOP8 packages: above 110 °C the value of $P_{tot}$ derates linearly with 8.0 mW/K.
For XSON8 and XQFN8 packages: above 45 °C the value of $P_{tot}$ derates linearly with 2.4 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 0.8 | 3.6 | V |
| $V_I$ | input voltage | | 0 | 3.6 | V |
| $V_O$ | output voltage | Active mode and Power-down mode | 0 | 3.6 | V |
| $T_{amb}$ | ambient temperature | | –40 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 0.8 V to 3.6 V | 0 | 200 | ns/V |


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## 10. Static characteristics

**Table 7. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$T_{amb}$ = 25 °C** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 0.8 V | 0.70 × $V_{CC}$ | - | - | V |
| | | $V_{CC}$ = 0.9 V to 1.95 V | 0.65 × $V_{CC}$ | - | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.6 | - | - | V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 0.8 V | - | - | 0.30 × $V_{CC}$ | V |
| | | $V_{CC}$ = 0.9 V to 1.95 V | - | - | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | - | 0.9 | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = 20 μA; $V_{CC}$ = 0.8 V to 3.6 V | - | - | 0.1 | V |
| | | $I_O$ = 1.1 mA; $V_{CC}$ = 1.1 V | - | - | 0.3 × $V_{CC}$ | V |
| | | $I_O$ = 1.7 mA; $V_{CC}$ = 1.4 V | - | - | 0.31 | V |
| | | $I_O$ = 1.9 mA; $V_{CC}$ = 1.65 V | - | - | 0.31 | V |
| | | $I_O$ = 2.3 mA; $V_{CC}$ = 2.3 V | - | - | 0.31 | V |
| | | $I_O$ = 3.1 mA; $V_{CC}$ = 2.3 V | - | - | 0.44 | V |
| | | $I_O$ = 2.7 mA; $V_{CC}$ = 3.0 V | - | - | 0.31 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 3.0 V | - | - | 0.44 | V |
| $I_I$ | input leakage current | $V_I$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V | - | - | ±0.1 | μA |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V to 3.6 V | - | - | ±0.1 | μA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V | - | - | ±0.2 | μA |
| $\Delta I_{OFF}$ | additional power-off leakage current | $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V to 0.2 V | - | - | ±0.2 | μA |
| $I_{CC}$ | supply current | $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V | - | - | 0.5 | μA |
| $\Delta I_{CC}$ | additional supply current | $V_I$ = $V_{CC}$ − 0.6 V; $I_O$ = 0 A; $V_{CC}$ = 3.3 V | - | - | 40 | μA |
| $C_I$ | input capacitance | $V_{CC}$ = 0 V to 3.6 V; $V_I$ = GND or $V_{CC}$ | - | 0.7 | - | pF |
| $C_O$ | output capacitance | $V_O$ = GND; $V_{CC}$ = 0 V | - | 0.9 | - | pF |



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**Table 7. Static characteristics** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$T_{amb}$ = −40 °C to +85 °C** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 0.8 V | 0.70 × $V_{CC}$ | - | - | V |
| | | $V_{CC}$ = 0.9 V to 1.95 V | 0.65 × $V_{CC}$ | - | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.6 | - | - | V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 0.8 V | - | - | 0.30 × $V_{CC}$ | V |
| | | $V_{CC}$ = 0.9 V to 1.95 V | - | - | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | - | 0.9 | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = 20 µA; $V_{CC}$ = 0.8 V to 3.6 V | - | - | 0.1 | V |
| | | $I_O$ = 1.1 mA; $V_{CC}$ = 1.1 V | - | - | 0.3 × $V_{CC}$ | V |
| | | $I_O$ = 1.7 mA; $V_{CC}$ = 1.4 V | - | - | 0.37 | V |
| | | $I_O$ = 1.9 mA; $V_{CC}$ = 1.65 V | - | - | 0.35 | V |
| | | $I_O$ = 2.3 mA; $V_{CC}$ = 2.3 V | - | - | 0.33 | V |
| | | $I_O$ = 3.1 mA; $V_{CC}$ = 2.3 V | - | - | 0.45 | V |
| | | $I_O$ = 2.7 mA; $V_{CC}$ = 3.0 V | - | - | 0.33 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 3.0 V | - | - | 0.45 | V |
| $I_I$ | input leakage current | $V_I$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V | - | - | ±0.5 | µA |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V to 3.6 V | - | - | ±0.5 | µA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V | - | - | ±0.5 | µA |
| $\Delta I_{OFF}$ | additional power-off leakage current | $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V to 0.2 V | - | - | ±0.6 | µA |
| $I_{CC}$ | supply current | $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V | - | - | 0.9 | µA |
| $\Delta I_{CC}$ | additional supply current | $V_I$ = $V_{CC}$ − 0.6 V; $I_O$ = 0 A; $V_{CC}$ = 3.3 V | - | - | 50 | µA |



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**Table 7. Static characteristics** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$T_{amb}$ = −40 °C to +125 °C** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 0.8 V | 0.75 × $V_{CC}$ | - | - | V |
| | | $V_{CC}$ = 0.9 V to 1.95 V | 0.70 × $V_{CC}$ | - | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.6 | - | - | V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 0.8 V | - | - | 0.25 × $V_{CC}$ | V |
| | | $V_{CC}$ = 0.9 V to 1.95 V | - | - | 0.30 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | - | 0.9 | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = 20 µA; $V_{CC}$ = 0.8 V to 3.6 V | - | - | 0.11 | V |
| | | $I_O$ = 1.1 mA; $V_{CC}$ = 1.1 V | - | - | 0.33 × $V_{CC}$ | V |
| | | $I_O$ = 1.7 mA; $V_{CC}$ = 1.4 V | - | - | 0.41 | V |
| | | $I_O$ = 1.9 mA; $V_{CC}$ = 1.65 V | - | - | 0.39 | V |
| | | $I_O$ = 2.3 mA; $V_{CC}$ = 2.3 V | - | - | 0.36 | V |
| | | $I_O$ = 3.1 mA; $V_{CC}$ = 2.3 V | - | - | 0.50 | V |
| | | $I_O$ = 2.7 mA; $V_{CC}$ = 3.0 V | - | - | 0.36 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 3.0 V | - | - | 0.50 | V |
| $I_I$ | input leakage current | $V_I$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V | - | - | ±0.75 | µA |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V to 3.6 V | - | - | ±0.75 | µA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V | - | - | ±0.75 | µA |
| $\Delta I_{OFF}$ | additional power-off leakage current | $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V to 0.2 V | - | - | ±0.75 | µA |
| $I_{CC}$ | supply current | $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V | - | - | 1.4 | µA |
| $\Delta I_{CC}$ | additional supply current | $V_I$ = $V_{CC}$ − 0.6 V; $I_O$ = 0 A; $V_{CC}$ = 3.3 V | - | - | 75 | µA |



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## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 8*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +125 °C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max (85 °C) | Max (125 °C) | |
| **$C_L$ = 5 pF** | | | | | | | | | |
| $t_{pd}$ | propagation delay | nA or nB to nY; see Figure 7 [2] | | | | | | | |
| | | $V_{CC}$ = 0.8 V | - | 13.5 | - | - | - | - | ns |
| | | $V_{CC}$ = 1.1 V to 1.3 V | 1.9 | 4.6 | 10.4 | 1.8 | 11.4 | 12.6 | ns |
| | | $V_{CC}$ = 1.4 V to 1.6 V | 1.5 | 3.3 | 6.5 | 1.4 | 7.4 | 8.2 | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.2 | 2.9 | 5.1 | 1.1 | 5.9 | 6.5 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 2.2 | 3.8 | 0.9 | 4.5 | 4.9 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0.9 | 2.3 | 4.0 | 0.8 | 4.5 | 4.9 | ns |
| **$C_L$ = 10 pF** | | | | | | | | | |
| $t_{pd}$ | propagation delay | nA or nB to nY; see Figure 7 [2] | | | | | | | |
| | | $V_{CC}$ = 0.8 V | - | 16.3 | - | - | - | - | ns |
| | | $V_{CC}$ = 1.1 V to 1.3 V | 2.3 | 5.6 | 12.3 | 2.1 | 13.7 | 15.1 | ns |
| | | $V_{CC}$ = 1.4 V to 1.6 V | 1.8 | 4.1 | 7.6 | 1.7 | 8.8 | 9.7 | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.6 | 3.8 | 6.1 | 1.4 | 7.1 | 7.8 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.4 | 2.9 | 4.6 | 1.2 | 5.4 | 5.9 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.3 | 3.2 | 5.7 | 1.1 | 6.4 | 7.0 | ns |
| **$C_L$ = 15 pF** | | | | | | | | | |
| $t_{pd}$ | propagation delay | nA or nB to nY; see Figure 7 [2] | | | | | | | |
| | | $V_{CC}$ = 0.8 V | - | 19.0 | - | - | - | - | ns |
| | | $V_{CC}$ = 1.1 V to 1.3 V | 2.6 | 6.6 | 14.2 | 2.4 | 15.8 | 17.4 | ns |
| | | $V_{CC}$ = 1.4 V to 1.6 V | 2.1 | 4.8 | 8.7 | 1.9 | 10.1 | 11.1 | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.9 | 4.6 | 7.6 | 1.7 | 8.5 | 9.3 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.6 | 3.6 | 5.6 | 1.5 | 6.3 | 6.9 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.6 | 4.1 | 7.5 | 1.4 | 8.3 | 9.1 | ns |
| **$C_L$ = 30 pF** | | | | | | | | | |
| $t_{pd}$ | propagation delay | nA or nB to nY; see Figure 7 [2] | | | | | | | |
| | | $V_{CC}$ = 0.8 V | - | 27.0 | - | - | - | - | ns |
| | | $V_{CC}$ = 1.1 V to 1.3 V | 3.6 | 9.5 | 19.5 | 3.2 | 21.8 | 24.0 | ns |
| | | $V_{CC}$ = 1.4 V to 1.6 V | 2.9 | 7.0 | 11.5 | 2.6 | 13.6 | 15.0 | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.6 | 7.0 | 12.1 | 2.3 | 13.3 | 14.6 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 2.4 | 5.4 | 8.9 | 2.1 | 9.9 | 10.9 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 2.3 | 6.5 | 12.7 | 2.1 | 13.9 | 15.3 | ns |



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**Table 8. Dynamic characteristics** *…continued*

*Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 8*

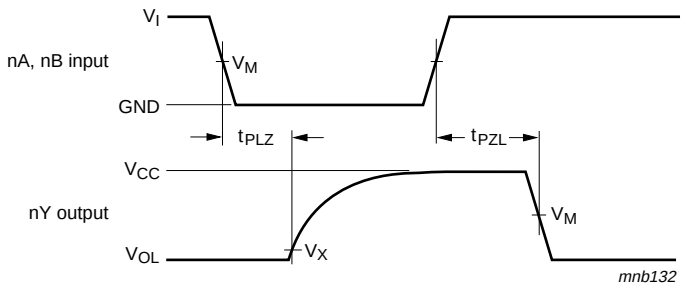
| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +125 °C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max (85 °C) | Max (125 °C) | |
| **$C_L$ = 5 pF, 10 pF, 15 pF and 30 pF** | | | | | | | | | |
| $C_{PD}$ | power dissipation capacitance | f = 1 MHz; $V_I$ = GND to $V_{CC}$ [3] | | | | | | | |
| | | $V_{CC}$ = 0.8 V | - | 0.6 | - | - | - | - | pF |
| | | $V_{CC}$ = 1.1 V to 1.3 V | - | 0.7 | - | - | - | - | pF |
| | | $V_{CC}$ = 1.4 V to 1.6 V | - | 0.8 | - | - | - | - | pF |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | 0.9 | - | - | - | - | pF |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | 1.1 | - | - | - | - | pF |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | 1.4 | - | - | - | - | pF |

[1] All typical values are measured at nominal $V_{CC}$.

[2] $t_{pd}$ is the same as $t_{PZL}$ and $t_{PLZ}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N$ where:
$f_i$ = input frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching.

## 12. Waveforms




Measurement points are given in Table 9.

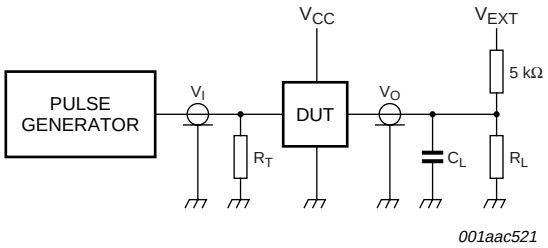
Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage drop that occur with the output load.

**Fig 7. The data input (nA or nB) to output (nY) propagation delays**

**Table 9. Measurement points**

| Supply voltage | Input | Output | |
|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ | $V_X$ |
| 0.8 V to 1.6 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.1 V |
| 1.65 V to 2.7 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.15 V |
| 3.0 V to 3.6 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.3 V |


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Test data is given in Table 10.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

**Fig 8. Load circuitry for switching times**

**Table 10. Test data**

| Supply voltage | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $C_L$ | $R_L$ [1] | $t_{PLH}$, $t_{PHL}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 0.8 V to 3.6 V | 5 pF, 10 pF, 15 pF and 30 pF | 5 kΩ or 1 MΩ | open | GND | $2 \times V_{CC}$ |

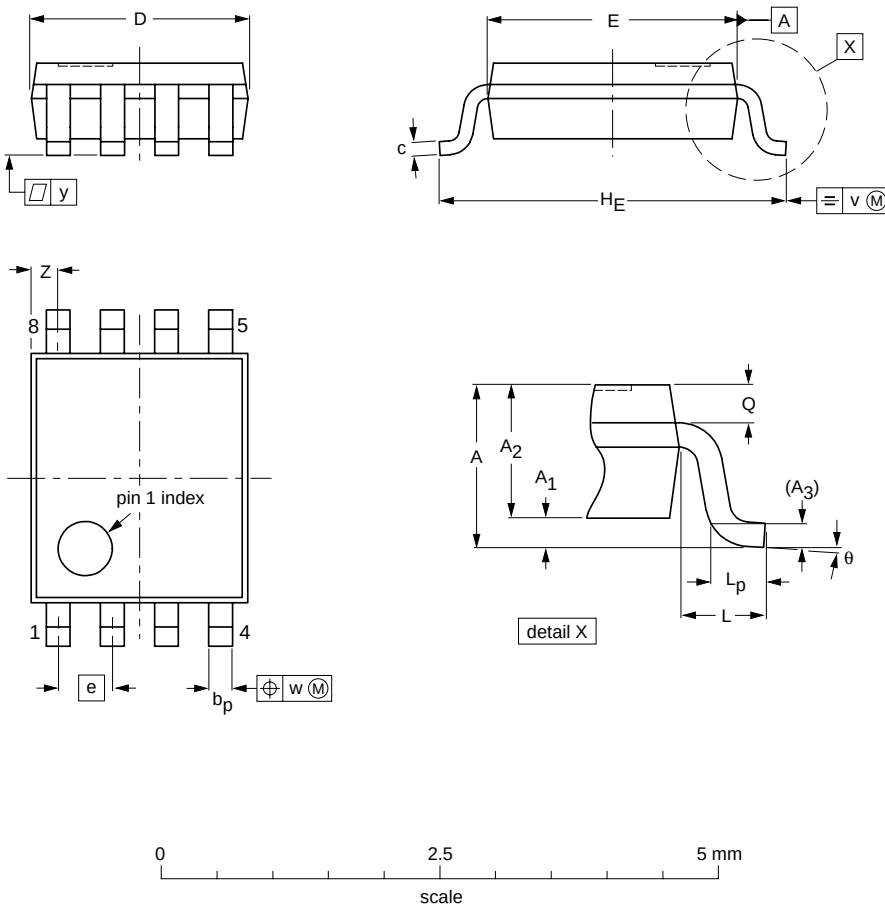
[1] For measuring enable and disable times $R_L$ = 5 kΩ, for measuring propagation delays, setup and hold times and pulse width $R_L$ = 1 MΩ.



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## 13. Package outline

**VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm** **SOT765-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.15<br>0.00 | 0.85<br>0.60 | 0.12 | 0.27<br>0.17 | 0.23<br>0.08 | 2.1<br>1.9 | 2.4<br>2.2 | 0.5 | 3.2<br>3.0 | 0.4 | 0.40<br>0.15 | 0.21<br>0.19 | 0.2 | 0.13 | 0.1 | 0.4<br>0.1 | 8°<br>0° |

**Notes**

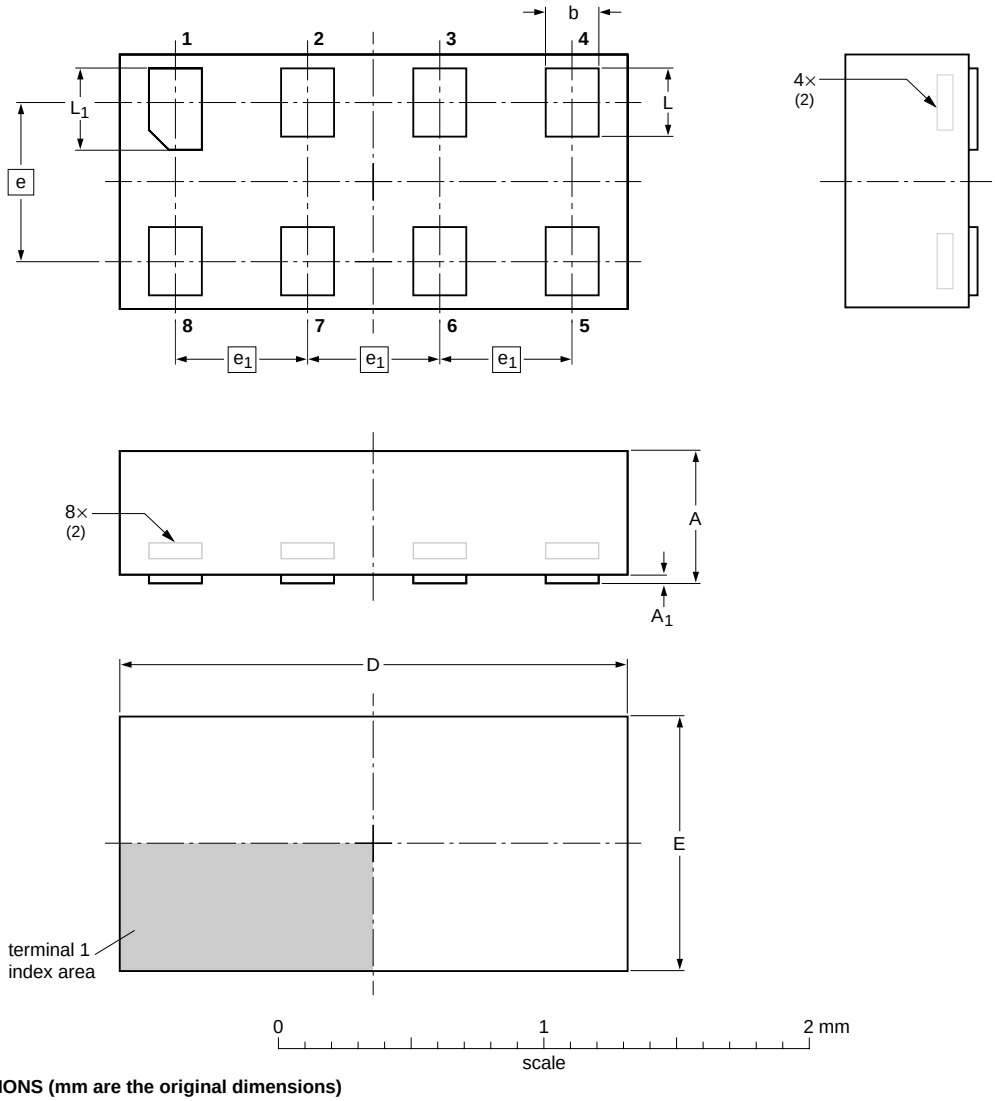
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT765-1 | | MO-187 | | | | 02-06-07 |

**Fig 9. Package outline SOT765-1 (VSSOP8)**


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**XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm** **SOT833-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max | A1 max | b | D | E | e | e1 | L | L1 |
|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.04 | 0.25<br>0.17 | 2.0<br>1.9 | 1.05<br>0.95 | 0.6 | 0.5 | 0.35<br>0.27 | 0.40<br>0.32 |

**Notes**

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

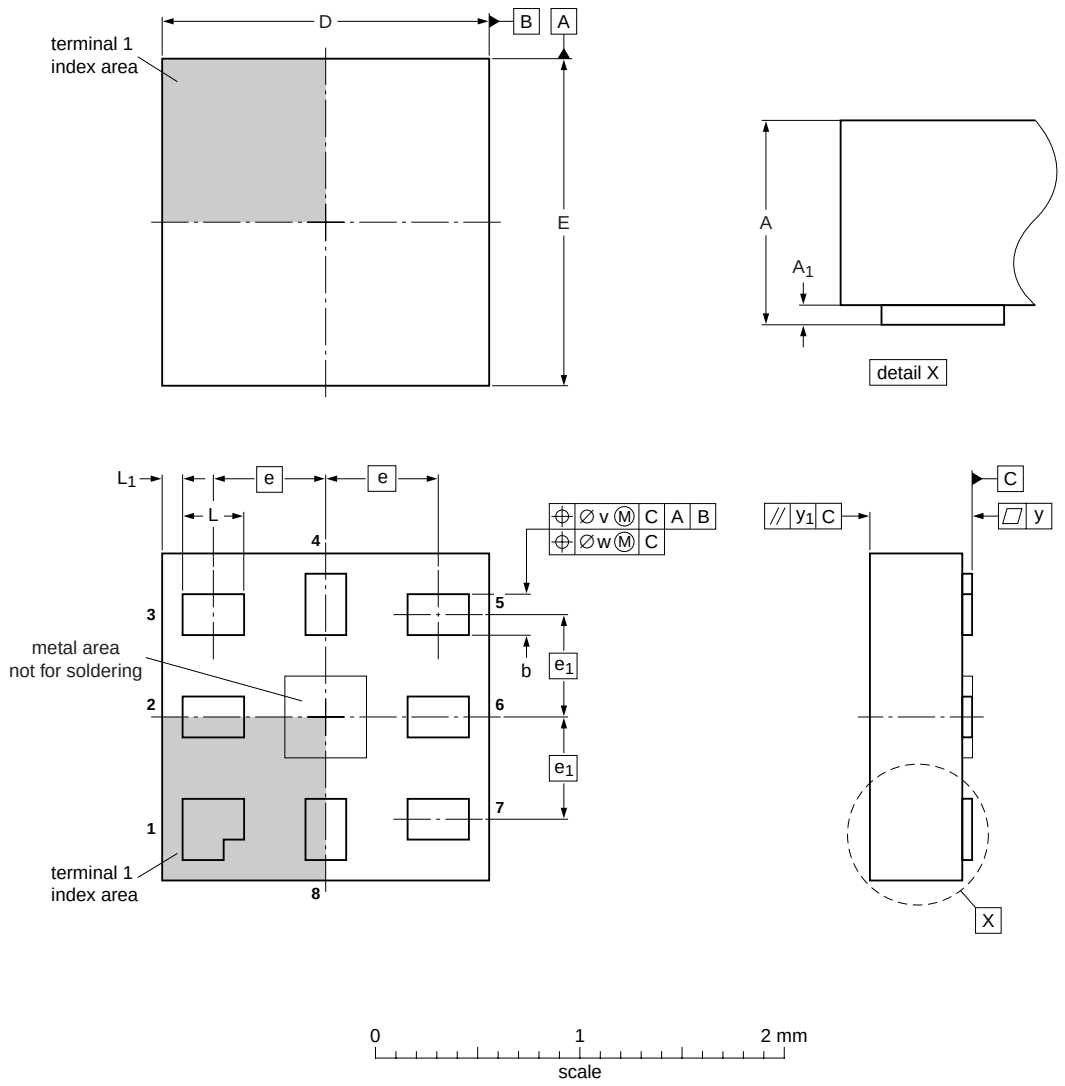
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT833-1 | - - - | MO-252 | - - - | | | ~~04-07-22~~<br>04-11-09 |

**Fig 10. Package outline SOT833-1 (XSON8)**



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**XQFN8: plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm** **SOT902-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.05<br>0.00 | 0.25<br>0.15 | 1.65<br>1.55 | 1.65<br>1.55 | 0.55 | 0.5 | 0.35<br>0.25 | 0.15<br>0.05 | 0.1 | 0.05 | 0.05 | 0.05 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT902-1 | - - - | MO-255 | - - - | | | ~~05-11-16~~<br>05-11-25 |

**Fig 11. Package outline SOT902-1 (XQFN8)**



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## 14. Abbreviations

**Table 11. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 15. Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74AUP2G38_1 | 20061016 | Product data sheet | - | - |



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# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 18. Contents


1 General description . . . . . 1
2 Features . . . . . 1
3 Ordering information . . . . . 2
4 Marking . . . . . 2
5 Functional diagram . . . . . 2
6 Pinning information . . . . . 2
6.1 Pinning . . . . . 2
6.2 Pin description . . . . . 3
7 Functional description . . . . . 3
8 Limiting values . . . . . 4
9 Recommended operating conditions . . . . . 4
10 Static characteristics . . . . . 5
11 Dynamic characteristics . . . . . 8
12 Waveforms . . . . . 9
13 Package outline . . . . . 11
14 Abbreviations . . . . . 14
15 Revision history . . . . . 14
16 Legal information . . . . . 15
16.1 Data sheet status . . . . . 15
16.2 Definitions . . . . . 15
16.3 Disclaimers . . . . . 15
16.4 Trademarks . . . . . 15
17 Contact information . . . . . 15
18 Contents . . . . . 16


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