DATA SHEET

74ABTL3205

10-bit BTL transceiver with registers

Product specification

1995 Jun 16

Philips
Semiconductors

PHILIPS

10-bit BTL transceiver with registers 74ABTL3205

FEATURES

- 10-bit BTL transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Tight output skew (0.5nsec typical)
- Glitch-free power up/down operation
- Low I_{CC} current
- Supports live insertion
- High density packaging
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

This transceiver is a 10 bit bidirectional transceiver and is intended to provide the electrical interface to a high performance wired-OR bus.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to “Backplane Transceiver Logic” (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading (<6pF) by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

To support live insertion, OEB is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. The BIAS V pin is a low current input which will reverse bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package. The LOGIC V_{CC} and BUS V_{CC} pins are also isolated internally to minimize noise and may be externally decoupled separately or simply tied together.

This transceiver function is intended to operate in a half-duplex mode. Low current in standby mode is obtained by powering down unused circuitry. Likewise, transmit circuitry is powered down when in receive mode and receive circuitry is powered down while in transmit mode.

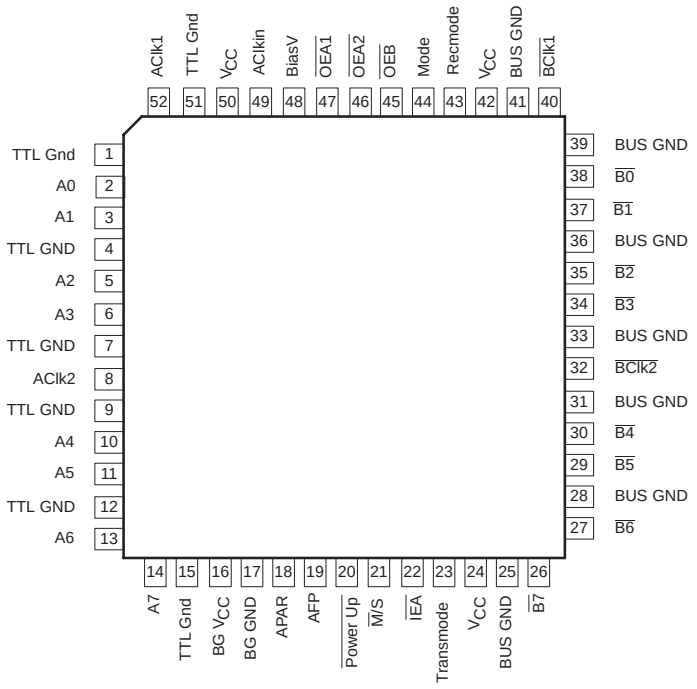
QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Bn}$		3.3 3.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to An		3.6 3.5	ns
C_{OB}	Output capacitance ($\overline{B0}$ - $\overline{B8}$) only)		6	pF
I_{OL}	Output current ($\overline{B0}$ - $\overline{B8}$) only)		100	mA
I_{CC}	Supply current	Standby	1	mA
		An to $\overline{Bn}$	7	
		$\overline{Bn}$ to An	18	

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52-PIN PQFP	–40°C to +85°C	74ABTL3205 BB	74ABTL3205 BB	SOT379-1

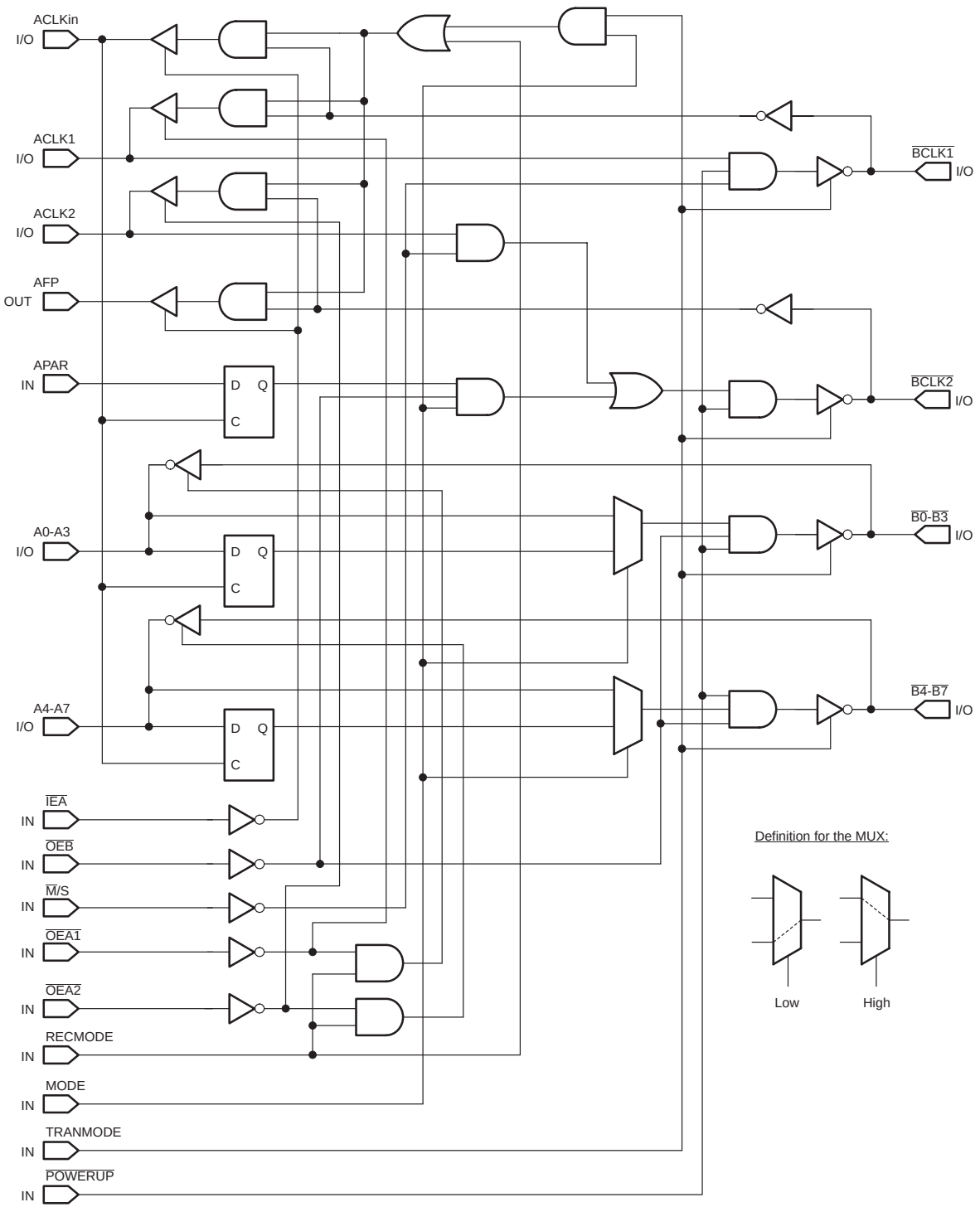
PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	FUNCTION	ASSERTION	I/O	LOGIC
OEA1	Output enable data receiver group 1	Low	Input	TTL
OEA2	Output enable data receiver group 2	Low	Input	TTL
OEB	Output enable data transmitter	Low	Input	TTL
IEA	Output enable clock and framepulse receiver	Low	Input	TTL
M/S	Master/Slave select: L: Master, enable clock transmitter H: Slave, disable clock transmitter		Input	TTL
Mode	 Low: Data through mode High: Registered data mode		Input	TTL
Power Up	Power up mode, held low during power up to disable clock and data transmitters	Low	Input	TTL
Recmode	Enables receiver	High	Input	TTL
Tranmode	Enables transmitter	High	Input	TTL
AClk1	Clock or data path		I/O	TTL
AClkIn	 IEA = H → Input for busclock IEA = L → Output for busclock		I/O	TTL
A0..A3	data group 1		I/O	TTL
AClk2	Clock or data path		I/O	TTL
AFPIn	Alternate data path		Output	TTL
APAR	Alternate data path		Input	TTL
A4..A7	data group 2		I/O	TTL
BClk1	Clock or data path		I/O	BTL
B0..B3	data group 1		I/O	BTL
BClk2	Clock or data path		I/O	BTL
B4..B7	data group 2		I/O	BTL

LOGIC DIAGRAM



FUNCTION TABLE

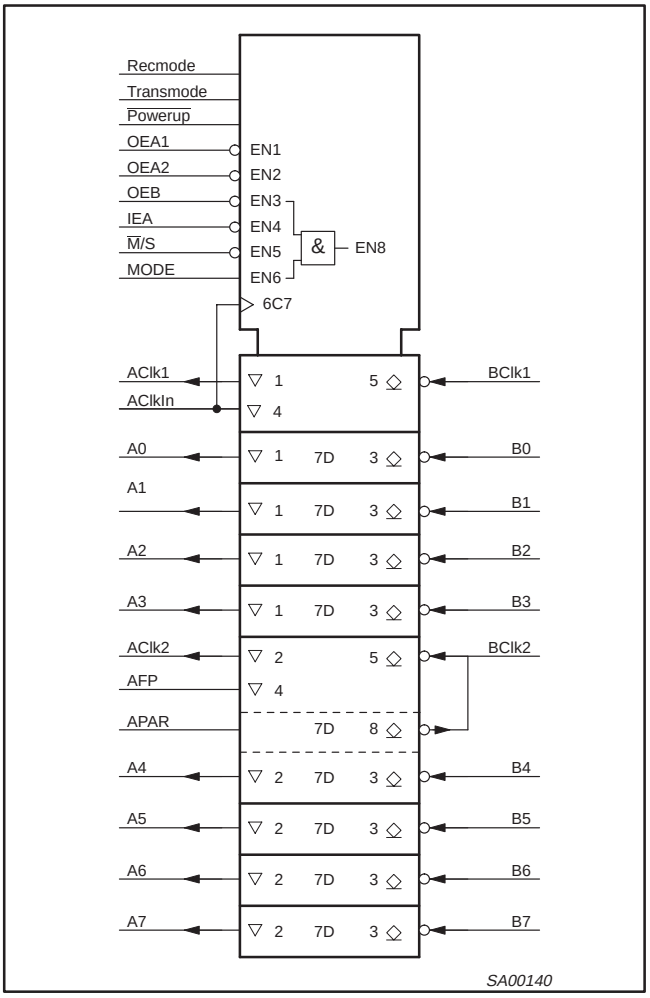
MODE	INPUTS																
	An	$\overline{Bn}$	ACLK in	ACLK 1	ACLK 2	$\overline{BCLK1}$	$\overline{BCLK2}$	$\overline{OEA1}$	$\overline{OEA2}$	$\overline{OEB}$	APAR	$\overline{IEA}$	$\overline{M}$/S	MODE	REC MODE	TRAN MODE	$\overline{POWER UP}$
An to Bn (REGISTERED)	l	O	↑	X	X	X	X	H	H	L	X	H	X	H	L	H	H
	h	O	↑	X	X	X	X	H	H	L	X	H	X	H	L	H	H
AN to Bn (THROUGH)	L	O	X	X	X	X	X	H	H	L	X	X	X	L	L	H	H
	H	O	X	X	X	X	X	H	H	L	X	X	X	L	L	H	H
B0-B3 to A0-A3 (THROUGH)	O	L	X	X	X	X	X	L	X	H	X	X	X	X	H	L	L
	O	H	X	X	X	X	X	L	X	H	X	X	X	X	H	L	L
B4-B7 to A4-A7 (THROUGH)	O	L	X	X	X	X	X	X	L	H	X	X	X	X	H	L	L
	O	H	X	X	X	X	X	X	L	H	X	X	X	X	H	L	L
ACLK1 to BCLK1	X	X	X	L	X	O	X	H	X	X	X	X	L	X	X	H	H
	X	X	X	H	X	O	X	H	X	X	X	X	L	X	X	H	H
ACLK2 to BCLK2	X	X	X	X	L	X	O	X	H	H	X	X	L	L	X	H	H
	X	X	X	X	H	X	O	X	H	H	X	X	L	L	X	H	H
BCLK1 to ACLK1	X	X	X	O	X	L	X	L	X	X	X	X	X	X	H	L	X
	X	X	X	O	X	H	X	L	X	X	X	X	X	X	H	L	X
BCLK2 to ACLK2	X	X	X	X	O	X	L	X	L	X	X	X	X	X	H	L	X
	X	X	X	X	O	X	H	X	L	X	X	X	X	X	H	L	X
APAR to BCLK2	X	X	↑	X	X	X	X	X	X	L	l	X	H	H	X	H	H
	X	X	↑	X	X	X	X	X	X	L	h	X	H	H	X	H	H
BCLK2 to AFPIn	X	X	X	X	X	X	L	X	X	X	X	L	X	X	H	L	X
	X	X	X	X	X	X	H	X	X	X	X	L	X	X	H	L	X
BCLK1 to ACLKin	X	X	O	X	X	L	X	H	H	L	O	L	H	H	L	H	H
	X	X	O	X	X	H	X	H	H	L	O	L	H	H	L	H	H

MODE	OUTPUTS							
	An	$\overline{Bn}$	ACLK in	ACLK1	ACLK2	$\overline{BCLK1}$	$\overline{BCLK2}$	AF Pin
An to Bn (REGISTERED)	Input	H*	X	X	X	X	X	X
	Input	L	X	X	X	X	X	X
AN to Bn (THROUGH)	Input	H*	X	X	X	X	X	X
	Input	L	X	X	X	X	X	X
B0-B3 to A0-A3 (THROUGH)	H	Input	Input	X	X	X	X	X
	L	Input	Input	X	X	X	X	X
B4-B7 to A4-A7 (THROUGH)	H	Input	Input	X	X	X	X	X
	L	Input	Input	X	X	X	X	X
ACLK1 to BCLK1	X	X	X	Input	X	H*	X	X
	X	X	X	Input	X	L	X	X
ACLK2 to BCLK2	X	X	X	X	Input	X	H*	X
	X	X	X	X	Input	X	L	X
BCLK1 to ACLK1	X	X	X	H	X	Input	X	X
	X	X	X	L	X	Input	X	X
BCLK2 to ACLK2	X	X	X	X	H	X	Input	X
	X	X	X	X	L	X	Input	X
APAR to BCLK2	X	X	Input	X	X	X	H*	X
	X	X	Input	X	X	X	L	X
BCLK2 to AFPIn	X	X	X	X	X	X	Input	H*
	X	X	X	X	X	X	Input	L
BCLK1 to ACLKin	X	X	H	X	X	Input	X	X
	X	X	L	X	X	Input	X	X

NOTES:

H = High voltage level
L = Low voltage level
h = High voltage level one set-up time prior to Low to High ACLKin transition
l = Low voltage level one set-up time prior to Low to High ACLKin transition
↑ = Low to High transition
Z = High impedance (off) state
H* = Goes to level of pull-up voltage
X = Don't care
O = Output

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted, these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage	TTL Signals	–1.2 to +7.0	V
		BTL Signals	–1.2 to +5.5	V
I_{IN}	Input current		–18 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +V_{CC}	/v
I_{OUT}	Current applied to output in Low output state	A0 - A8	48	mA
		$\overline{B0}$ - $\overline{B8}$	200	mA
T_{amb}	Operating free-air temperature range		–40 to +85	°C
T_{STG}	Storage temperature		–65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{BTL}$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V		0.5	100	µA
I_{OFF}	Power-off output current	$\overline{BTL}$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V		10	100	µA
V_{OH}	High-level output voltage	TTL	V_{CC} = MIN, V_{IL} = MAX,[4] V_{IH} = MIN, I_{OH} = –3mA	2.5	2.85	3.4	V
			V_{CC} = MIN to MAX, [4] V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –10µA			V_{CC} – 1.1	V
V_{OL}	Low-level output voltage	TTL	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA		0.35	0.5	V
		$\overline{BTL}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 100mA	0.75	1.0	1.10	V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 4mA	0.5	0.7		V
V_{IK}	Input clamp voltage	TTL	V_{CC} = MIN, I_I = I_{IK}		0.8	–1.2	V
		$\overline{BTL}$	V_{CC} = MIN, I_I = –18mA		0.8	–1.2	V
I_I	Input current at maximum input voltage	TTL	V_{CC} = MAX, V_I = 0.5V or 5.5V		0.1	±50	µA
I_{IH}	High-level input current	$\overline{TTL}$	V_{CC} = MAX, V_I = 2.7V, $\overline{Bn}$ = AIn = 0V		0.1	20	µA
		$\overline{BTL}$	V_{CC} = MAX, V_I = 1.9V		0.1	100	µA
			V_{CC} = MAX, V_I = 3.5V[5]	100			mA
I_{IL}	Low-level input current	TTL	V_{CC} = MAX, V_I = 0.5V		0.1	–20	µA
		$\overline{BTL}$	V_{CC} = MAX, V_I = 0.75V		0.1	–100	µA
I_{OZH}	Off-state output current	TTL	V_{CC} = MAX, V_O = 2.7V		0.1	50	µA
I_{OZL}	Off-state output current	TTL	V_{CC} = MAX, V_O = 0.5V		20	–50	µA
I_{OS}	Short-circuit output current[3]	TTL	V_{CC} = MAX, V_O = 0.0V	–60	130	–150	mA
I_{CC}	Supply current (total)	Recmode Low Tranmode Low	V_{CC} = MAX		1	3	mA
		Recmode Low Tranmode High	V_{CC} = MAX Mode = Low		7	12	mA
		Recmode Low Tranmode High	V_{CC} = MAX Mode = High		13	21	mA
		Recmode High Tranmode Low	V_{CC} = MAX		18	25	mA
		Recmode High Tranmode High	V_{CC} = MAX		29	43	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
5. For B port input voltage between 3 and 5 volts I_{IH} will be greater than 100µA, but the parts will continue to function normally.

TTL signals CLKin, CLK-1/CLK-OUT, CLK-2/FP-OUT, /FP-IN, /PARITY t,A0..A7, OEB, MASTER/SLAVE, MODE, OEA1, OEA2

BTL signals CLK1BTL, CLK2BTL, B0..B7

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{BIASV}	Bias pin DC current	V_{CC} = 0 to 5.25V, $\overline{Bn}$ = 0 to 2.0 V	4.5		5.5	V
I_{BIASV}	Bias pin DC current	V_{CC} = 0 to 4.75 V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			1	mA
		V_{CC} = 4.5 to 5.5V, $\overline{Bn}$ = 0 to 2.0 V, Bias V = 4.5 to 5.5V			10	µA
$\sqrt{Bn}$	Bus voltage during prebias	$\overline{B0}$ – $\overline{B8}$ = 0V, Bias V = 5.0V	1.62		2.1	V

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, C_L = 500Ω			T_{amb} = –40°C to +85°C, V_{CC} = 5V ± 10%, C_L = 50pF, C_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to An	Waveform 2	2.0 1.8	3.6 3.5	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PLH} t_{PHL}	Propagation delay, BCLK1 to ACLK1	Waveform 2	2.0 1.8	3.8 3.6	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PLH} t_{PHL}	Propagation delay BCLK1 to ACLKin	Waveform 2	2.0 1.8	3.7 3.7	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PLH} t_{PHL}	Propagation delay BCLK2 to ACLK2	Waveform 2	2.0 1.8	3.7 3.9	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PLH} t_{PHL}	Propagation delay BCLK2 to AFP	Waveform 2	2.0 1.8	3.8 3.9	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PZH} t_{PLZ}	Output Enable time $\overline{OEA1}$, $\overline{OEA2}$, $\overline{IEA}$ to An	Waveform 1, 2	2.0 1.8	3.8 2.5	6.5 6.1	2.0 1.8	7.3 6.7	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEA1}$, $\overline{OEA2}$, $\overline{IEA}$ to An	Waveform 4, 5	1.6 2.0	2.5 3.3	5.6 7.8	1.4 1.8	5.7 8.2	ns
t_{TLH} t_{THL}	Output transition time, An Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				3.0 1.7	7.0 4.0	ns
$t_{SK}(p)$	Pulse skew[2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 3		2.0				ns

NOTES:
1. $|t_{PN}$ actual – t_{PM} actual$|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle. (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5V C_D = 30pF, R_U = 18.5Ω			T_{amb} = –40°C to +85°C V_{CC} = 5V ± 10% C_L = 30pF, R_U = 18.5Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Bn}$	Waveform 2	1.0 1.0	3.3 2.7	4.7 4.5	1.0 1.0	5.7	ns
t_{PLH} t_{PHL}	Propagation delay, ACLKin to $\overline{Bn}$	Waveform 1, 2	2.0 2.0	4.6 4.5	5.9 5.9	2.0 2.0	6.3 6.3	ns
t_{PLH} t_{PHL}	Propagation delay ACLKin to BCLK2	Waveform 1, 2	2.0 2.0	4.6 4.5	7.3 7.3	2.0 2.0	7.6 7.6	ns
t_{PLH} t_{PHL}	Propagation delay ACLK1 to BCLK1	Waveform 2	1.0 1.0	3.2 2.9	4.7 4.5	1.0 1.0	5.1 4.7	ns
t_{PLH} t_{PHL}	Propagation delay ACLK2 to BCLK2	Waveform 2	1.0 1.0	3.1 3.1	5.7 5.5	1.0 1.0	6.0 5.6	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}$ to $\overline{Bn}$ or BCLK2	Waveform 1, 2	1.0 1.0	3.8 3.4	6.8 6.4	1.0 1.0	7.6 6.9	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.6		2.5 2.0	1.0 0.6	3.0 2.5	ns
$t_{SK}(p)$	Pulse skew2 $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 3		2.0				ns

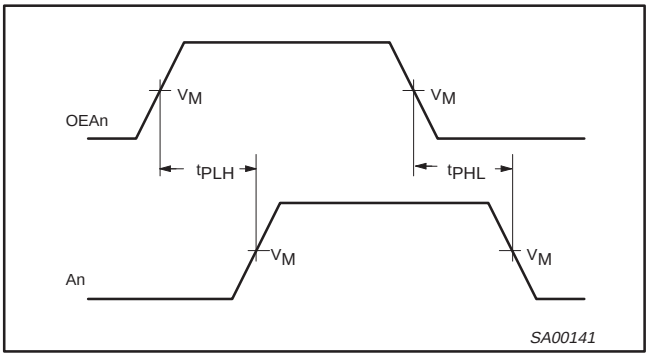
NOTES:
1. $|t_{PN}$ actual $- t_{PM}$ actual$|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle. (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC SETUP REQUIREMENTS

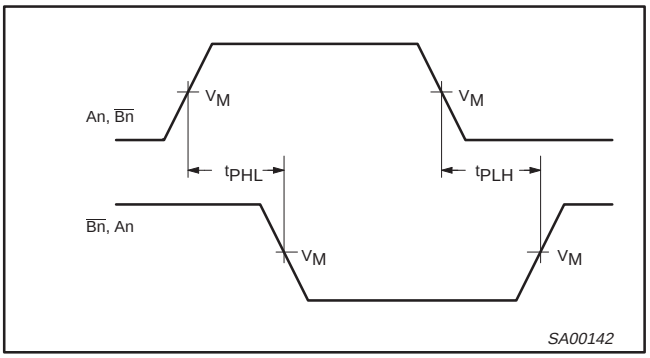
SYMBOL	PARAMETER	TEST CONDITION	LIMITS				UNIT
			T_{amb} = +25°C V_{CC} = 5V		T_{amb} = –40°C to +85°C V_{CC} = 5V ± 10%		
			C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 18.5Ω (B side)				
			MIN	TYP	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time An to ACLKin	Waveform 6	1.9 1.3		2.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time An to ACLKin	Waveform 6	1.8 2.0		2.3 2.0		ns

AC WAVEFORMS

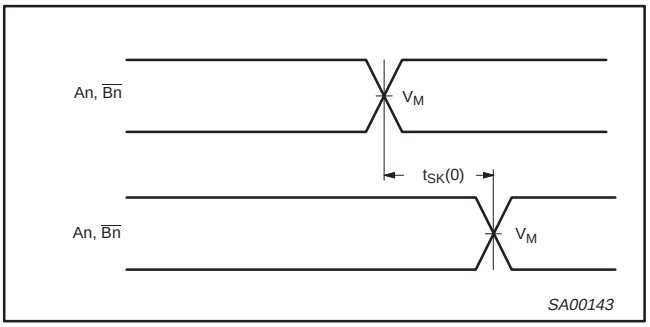
V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others



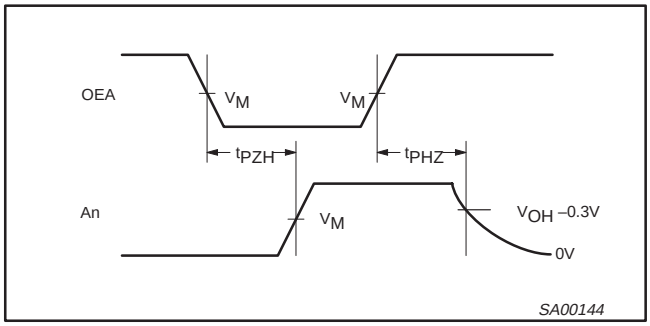
Waveform 1. Propagation Delay for Data or Output Enable to Output



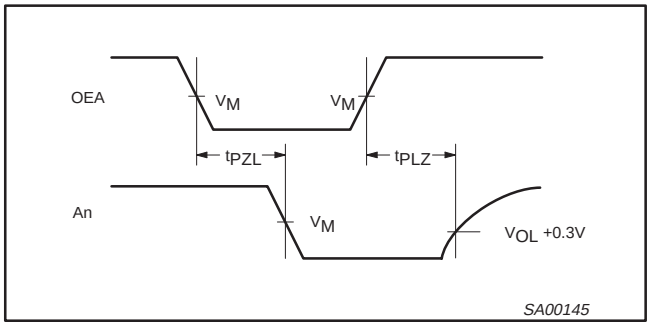
Waveform 2. Propagation Delay for Data to Output



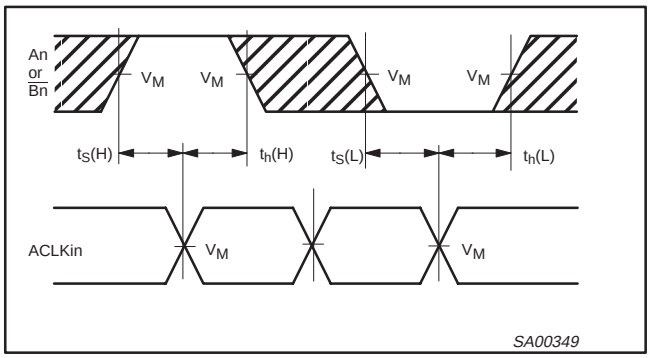
Waveform 3. Output Skews



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

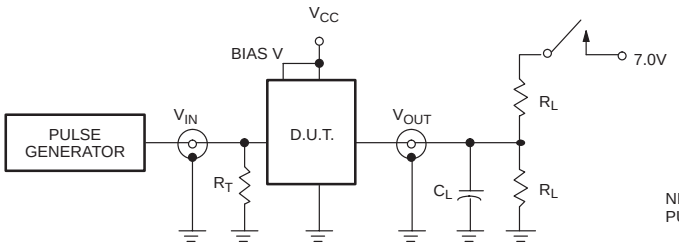


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 6. Data Setup and Hold Times

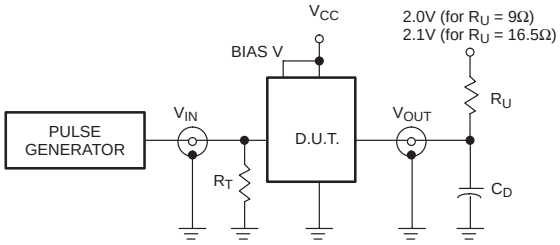
TEST CIRCUIT AND WAVEFORMS



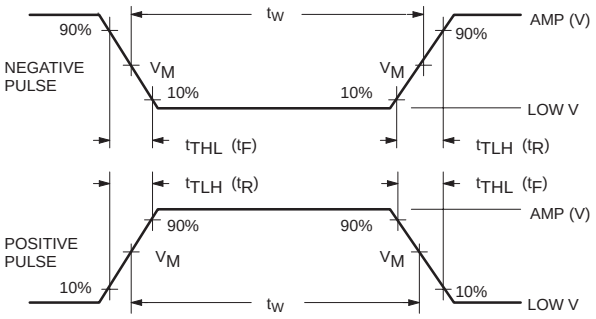
Test Circuit for 3-State Outputs on A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit for Outputs on B Port



V_M = 1.55V for Bn or $\overline{Bn}$, V_M = 1.5V for all others

Input Pulse Definition

ABTL	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

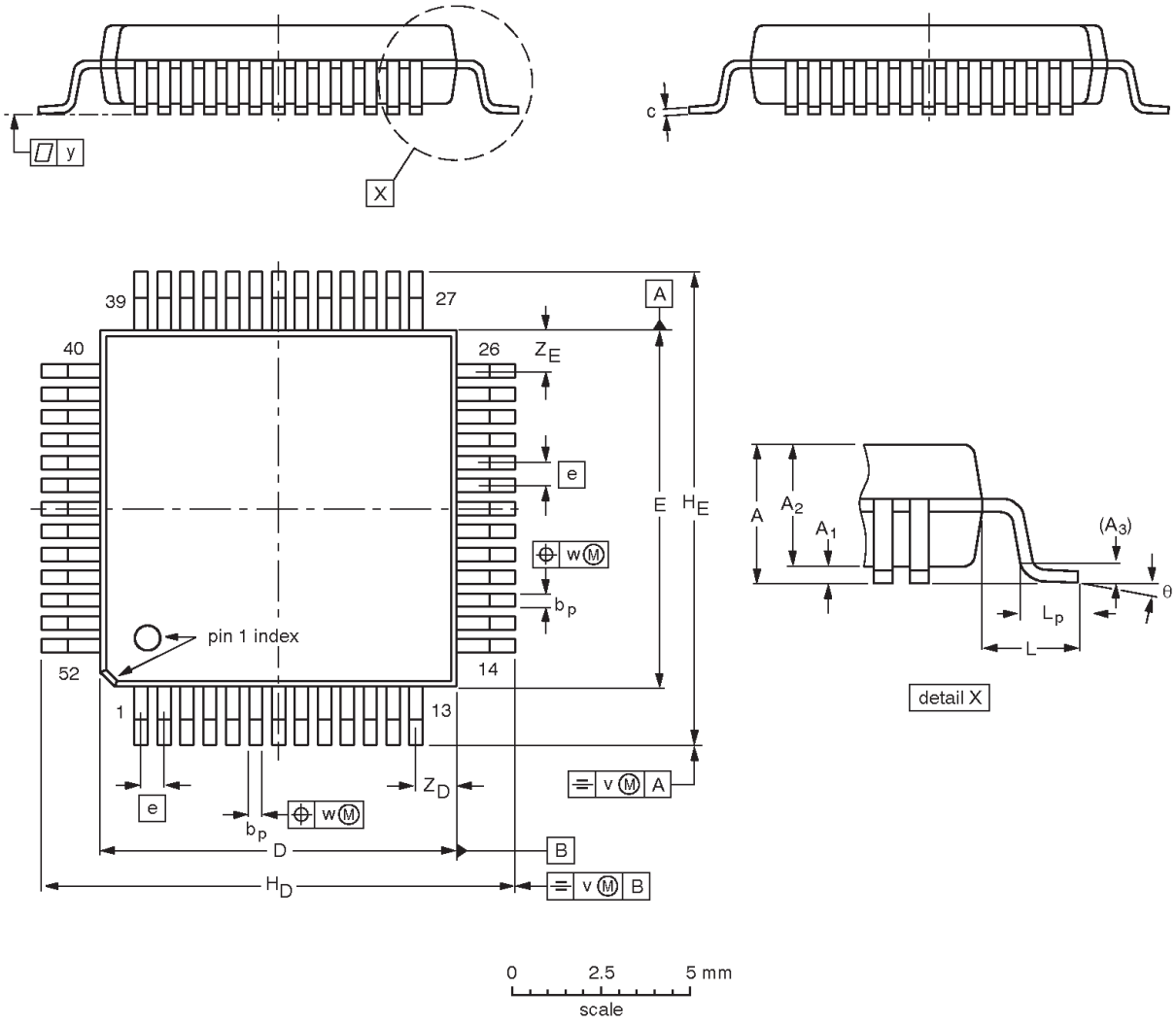
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.

SA00146

QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm SOT379-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.45	0.45 0.25	2.10 1.95	0.25	0.38 0.22	0.23 0.13	10.1 9.9	10.1 9.9	0.65	13.45 12.95	13.45 12.95	1.60	0.95 0.65	0.20	0.12	0.10	1.24 0.95	1.24 0.95	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT379-1		MO-108				~~95-02-04~~ 97-08-04

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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