73S8023C
Smart Card Interface

Simplifying System Integration™

DATA SHEET

April 2009

DESCRIPTION

The Teridian 73S8023C is a low-power, high efficiency, single smart card interface IC suitable for 3V and 5V cards. It provides full electrical compliance with ISO-7816-3 and EMV 4.0 (EMV2000) specifications.

Hardware support for any type of synchronous cards (memory cards) is provided.

Interfacing with the system controller is done through the control bus; composed of digital inputs to control the interface, and one interrupt output to inform the system controller of the card presence and faults. Data exchange with the card is managed from the system controller using the I/O line (and eventually the auxiliary I/O lines).

A chip select input allows multiple 73S8023C ICs to share the same control bus. When chip select is set low, the host microcontroller inputs are latched and outputs are taken to a high impedance state.

The card clock signal can be generated by an on-chip oscillator using an external crystal or by connecting an external clock signal.

The 73S8023C device incorporates an ISO-7816-3 activation/deactivation sequencer that controls the card signals. Emergency card deactivation is initiated upon card extraction or upon any fault generated by the protection circuitry.

The 73S8023C requires only a single 2.7 V to 3.6 V power supply, and features a high-efficiency embedded DC-DC converter. This architecture, plus a Power Down digital input that allow placing the IC in a very low-power mode making the 73S8023C particularly suitable for low-power applications (cell-phones, PDAs, payphones, hand-held POS terminals…).

ADVANTAGES

- Supports both synchronous and asynchronous smart cards
- Replacement for TDA8002, with up to 600 mW in power savings (@ EMV ICCmax condition) !
- The inductor-based DC-DC converter provides higher current and efficiency
  - → Ideal for battery-powered applications
  - → Suitable for high current cards and SAMs: (100 mA max)
  - → Single 2.7 V to 3.6 V power supply allows removal of 5 V from the system
- Power down mode: 2 µA typical
- Package: Small Format (5x5mm) 32-QFN

FEATURES

- **Card Interface:**
  - Complies with ISO-7816-3, EMV 4.0
  - A DC-DC Converter provides 3V / 5V to the card from an external power supply input
  - High-efficiency converter: > 80% @ V_{DD}=3.3 V, V_{CC}=5 V and I_{CC} = 65 mA
  - Up to 100 mA supplied to the card
  - ISO-7816-3 Activation / Deactivation sequencer with emergency automated deactivation
  - Protection includes 2 voltage supervisors which detect voltage drops on card V_{CC} and on V_{DD} power supply
  - The V_{DD} voltage supervisor threshold value can be externally adjusted
  - True over-current detection (150 mA max.)
  - 2 card detection inputs, 1 for either possible switch configuration
  - Full support of synchronous cards
- **System Controller Interface:**
  - 3 Digital inputs control the card activation / deactivation, card reset and card voltage
  - 3 Digital inputs control the card clock (division rate and card clock source selection)
  - 1 Digital output, interrupt to the system controller, allows the system controller to monitor the card presence and faults
  - 1 Power down digital input (places the 73S8023C in a very low-power mode (card deactivated)
  - 1 Chip select digital input for parallel operation of several 73S8023C ICs.
  - 1 External clock input (STROBE), used for synchronous operation
  - 1 Digital output clock, buffered version of signal on XTALIN
  - Crystal oscillator or host clock (XTALIN), up to 27 MHz
- **Power Supply: V_{DD} 2.7 V to 3.6 V**
- **6 kV ESD Protection on the card interface**

APPLICATIONS

- Point of Sales and Transaction Terminals
- Payphones
- Set-Top-Boxes, DVD / HDD Recorders
- Payment card interfaces in portable devices (PDAs, mobile phones…)

© 2009 Teridian Semiconductor Corporation

FUNCTIONAL DIAGRAM

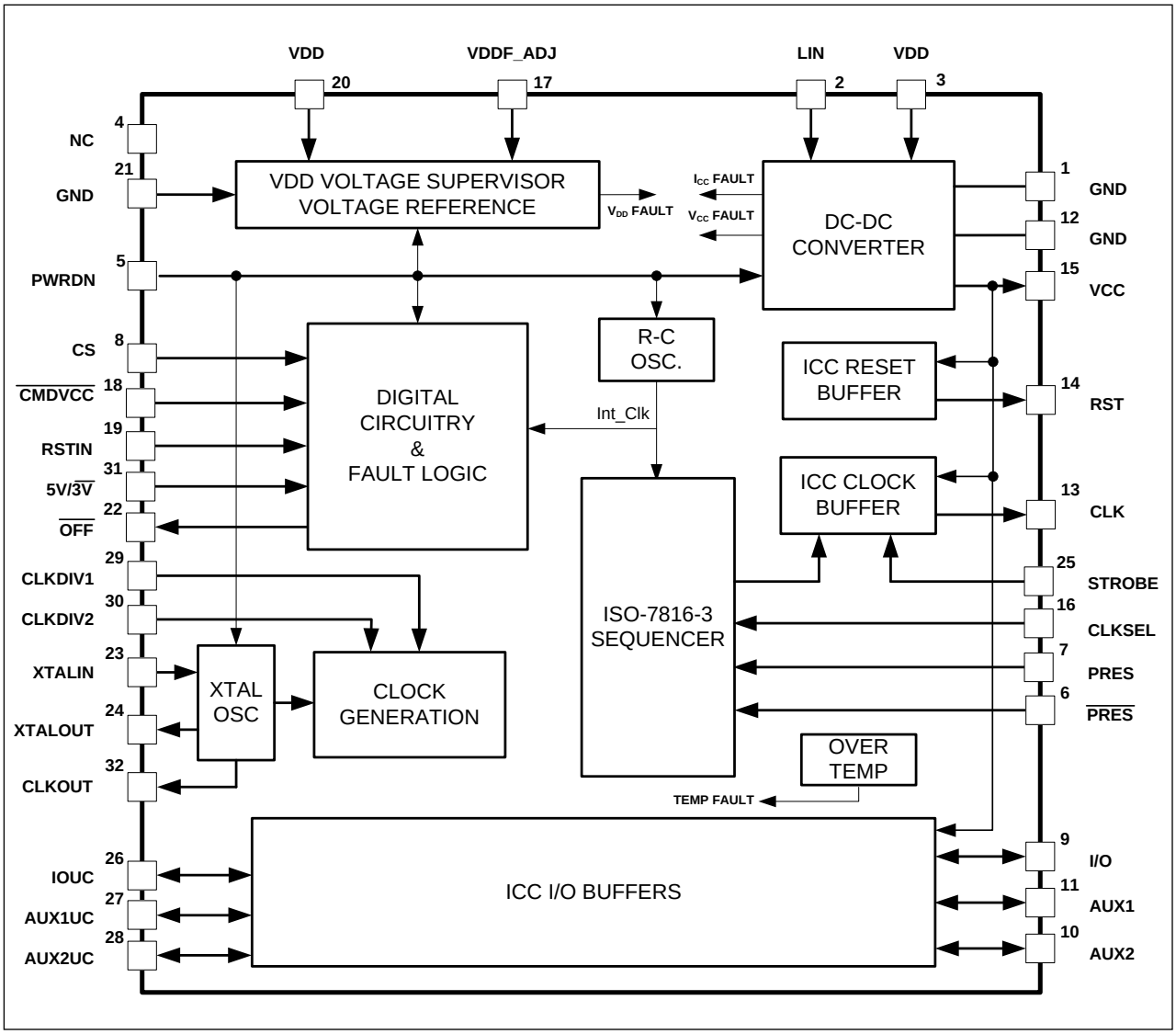


Figure 1: 73S8023C Block Diagram

Table of Contents

1 Pin Description 5
1.1 Card Interface 5
1.2 Miscellaneous Inputs and Outputs 5
1.3 Power Supply and Ground 5
1.4 Microcontroller Interface 6
2 System Controller Interface 7
3 Oscillator 8
4 DC-DC Converter – Card Power Supply 8
5 Voltage Supervision 9
6 Power Down 10
7 Over-Temperature Monitor 10
8 Activation and Deactivation 11
8.1 Activation Sequence (Synchronous Mode) 11
8.2 Deactivation Sequence (Synchronous Mode) 11
8.3 Activation Sequence (Asynchronous Mode) 12
8.4 Deactivation Sequence (Asynchronous Mode) 14
9 $\overline{\text{OFF}}$ and Fault Detection 14
10 I/O Circuitry and Timing 15
11 Typical Application Schematic 17
12 Electrical Specification 18
12.1 Absolute Maximum Ratings 18
12.2 Recommended Operating Conditions 18
12.3 Package Thermal Parameters 18
12.4 Card Interface Characteristics 19
12.5 Digital Signals 22
12.6 DC Characteristics 23
12.7 Voltage / Temperature Fault Detection Circuits 23
13 Mechanical Drawing (32-QFN) 24
14 Package Pin Designation (32-QFN) 25
15 Ordering Information 26
16 Related Documentation 26
17 Contact Information 26
Revision History 27

Figures

Figure 1: 73S8023C Block Diagram 2
Figure 2: Power Down Mode Operation: CS = high 10
Figure 3: Activation Sequence – Synchronous Mode 11
Figure 4: Synchronous Deactivation Operation – CKSEL = High 12
Figure 5: Asynchronous Activation Sequence – RSTIN Low When $\overline{\text{CMDVCC}}$ Goes Low 13
Figure 6: Asynchronous Activation Sequence – Timing Diagram #2 13
Figure 7: Asynchronous Deactivation Sequence 14
Figure 8: Timing Diagram – Management of the Interrupt Line $\overline{\text{OFF}}$ 15
Figure 9: I/O and I/OUC State Diagram 16
Figure 10: I/O – I/OUC Delays Timing Diagram 16
Figure 11: 73S8023C – Typical Application Schematic 17
Figure 12: DC – DC Converter efficiency (V_{CC} = 5 V) 20
Figure 13: DC – DC Converter Efficiency (V_{CC} = 3 V) 20
Figure 14: 32-QFN Mechanical Drawing 24
Figure 15: 32-QFN 73S8023C Pin Out 25

Table

Table 1: Choice of VCC Pin Capacitor 8

1 Pin Description

1.1 Card Interface

Name	Pin	Description
I/O	9	Card I/O: Data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
AUX1	11	AUX1: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
AUX2	10	AUX2: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
RST	14	Card reset: Provides reset (RST) signal to card.
CLK	13	Card clock: Provides clock (CLK) signal to card. The rate of this clock is determined by crystal oscillator frequency and CLKDIV selections.
PRES	7	Card Presence switch: Active high indicates card is present. Includes a pull-down current source.
$\overline{\text{PRES}}$	6	Card Presence switch: Active low indicates card is present. Includes a pull-up current source.
VCC	15	Card power supply: Logically controlled by sequencer, output of DC-DC converter. Requires an external filter capacitor to the card GND.
GND	12	Card ground.

1.2 Miscellaneous Inputs and Outputs

Name	Pin	Description
XTALIN	23	Crystal oscillator input: can either be connected to crystal or driven as a source for the card clock.
XTALOUT	24	Crystal oscillator output: connected to crystal. Left open if XTALIN is being used as external clock input.
VDDF_ADJ	17	V_{DD} fault threshold adjustment input: this pin can be used to adjust V_{DDF} value (that controls deactivation of the card). Must be left open if unused.
NC	4	Non-connected pin. Must be left open.

1.3 Power Supply and Ground

Name	Pin	Description
VDD	3, 20	System controller interface supply voltage: Supply voltage for internal power supply and DC-DC converter power supply source.
GND	1	DC-DC converter ground.
GND	21	Digital ground.
LIN	2	External inductor. Connect external inductor from pin 2 to V_{DD}. Keep the inductor close to pin 2.

1.4 Microcontroller Interface

<table>
<tr><th>Name</th><th>Pin</th><th>Description</th></tr>
<tr><td>CMDVCC</td><td>18</td><td>Command V_{CC} (negative assertion): Logic low on this pin causes the DC-DC converter to ramp the V_{CC} supply to the card and initiates a card activation sequence.</td></tr>
<tr><td>5V/$\overline{3V}$</td><td>31</td><td>5 volt / 3 volt card selection: Logic one selects 5 volts for V_{CC} and card interface, logic low selects 3 volt operation. When the part is to be used with a single card voltage, this pin should be tied to either GND or V_{DD}. However, it includes a high impedance pull-up resistor to default this pin high (selection of 5V card) when unconnected</td></tr>
<tr><td>PWRDN</td><td>5</td><td>Power Down control input: Active High. When Power Down (PD) mode is activated, all internal analog functions are disabled to place the 73S8023C in its lowest power consumption mode. The PD mode is allowed only out of a card session (PWRDN high is ignored when CMDVCC = 0). Must be tied to ground when power down function is not used.</td></tr>
<tr><td>CLKDIV1
CLKDIV2</td><td>29
30</td><td>Sets the divide ratio from the XTALIN oscillator (or external clock input) to the card clock. These pins include pull-down resistors.
<table>
<tr><th>CLKDIV1</th><th>CLKDIV2</th><th>Clock Rate</th></tr>
<tr><td>0</td><td>0</td><td>XTALIN/8</td></tr>
<tr><td>0</td><td>1</td><td>XTALIN/4</td></tr>
<tr><td>1</td><td>1</td><td>XTALIN/2</td></tr>
<tr><td>1</td><td>0</td><td>XTALIN</td></tr>
</table></td></tr>
<tr><td>OFF</td><td>22</td><td>Interrupt signal to the processor: Active Low. Multi-function indicating fault conditions and card presence. Open drain output configuration; it includes an internal 20 kΩ pull-up to $V_{DD.}$</td></tr>
<tr><td>RSTIN</td><td>19</td><td>Reset Input: This signal controls the RST signal to the card.</td></tr>
<tr><td>I/OUC</td><td>26</td><td>System controller data I/O to/from the card. Includes internal pull-up resistor to $V_{DD.}$</td></tr>
<tr><td>AUX1UC</td><td>27</td><td>System controller auxiliary data I/O to/from the card. Includes internal pull-up resistor to $V_{DD.}$</td></tr>
<tr><td>AUX2UC</td><td>28</td><td>System controller auxiliary data I/O to/from the card. Includes internal pull-up resistor to $V_{DD.}$</td></tr>
<tr><td>CS</td><td>8</td><td>When CS = 1, the control and signal pins are configured normally. When CS is set low, signals CMDVCC, RSTIN, PWRDN, 5V/#V, CLKDIV1, CLKDIV2, CLKSEL are latched. I/OUC, AUX1UC, and AUX2UC are set to high impedance pull-up mode and won't pass data to or from the smart card. OFF output is tri-stated.</td></tr>
<tr><td>CLKSEL</td><td>16</td><td>Selects CLK and RST operational mode. When CLKSEL is low (default), the circuit is configured for asynchronous card operation and the sequencer manages the control of CLK and RST. When CLKSEL is high, the signal CLK is a buffered copy of STROBE and the signal RST is directly controlled by RSTIN.</td></tr>
<tr><td>STROBE</td><td>25</td><td>When CLKSEL = 1, the signal CLK is controlled directly by STROBE.</td></tr>
<tr><td>CLKOUT</td><td>32</td><td>CLKOUT is the buffered version of the signal on pin XTALIN.</td></tr>
</table>

2 System Controller Interface

- The CS (chip select) input allows multiple devices to operate in parallel. When CS is high, the system interface signals operate as described. When CS is taken low, the system interface signals are latched internally. The pins I/OUC, AUX1UC, and AUX2UC are weakly pulled up and the $\overline{OFF}$ signal is put into a high impedance state.
- The CLKSEL signal selects between synchronous and asynchronous operation. When CLKSEL is low, asynchronous operation is selected. When CLKSEL is high, synchronous operation is selected.
- Digital inputs allow direct control of the card interface from the host as follows:
  - Pin $\overline{CMDVCC}$: When set low, starts an activation sequence if a card is present.
  - Pin 5V/$\overline{3V}$: Defines the card voltage.
- The card I/O and Reset signals have their corresponding controller I/Os to be connected directly to the host:
  - Pin RSTIN: controls the card RST signal. When enabled by the sequencer, RST is equal to RSTIN for both synchronous and asynchronous modes.
  - Pin I/OUC: data transfer to card I/O contact.
  - Pins AUX1UC and AUX2UC (auxiliary I/O lines associated to the auxiliary I/Os which are connected to the C4 and C8 card connector contacts).
- Two digital inputs control the card clock frequency division rate: CLKDIV1 and CLKDIV2 define the card clock frequency from the input clock frequency (crystal or external clock). The division rate is defined as follows:

CLKDIV2	CLKDIV1	CLK
0	0	⅛ XTAL
0	1	XTAL
1	0	¼ XTAL
1	1	½ XTAL

When the division rate is equal to 1 (CLKDIV2 =0 and CLKDIV1 = 1), the duty-cycle of the card clock depends on the duty-cycle and waveform of the signal applied on the pin XTALIN. When other division rates are used, the 73S8023C circuitry guarantees a duty-cycle in the range 45% to 55%, conforming to ISO-7816-3 and EMV 4.1 specifications.

- Interrupt output to the host: As long as the card is not activated, the $\overline{OFF}$ pin informs the host about the card presence only (low = no card in the reader). When $\overline{CMDVCC}$ is set low (Card activation sequence requested from the host), a low level on $\overline{OFF}$ means a fault has been detected (e.g. card removedl during a card session, or voltage fault, or thermal / over-current fault) that automatically initiates a deactivation sequence.
- Power Down: The PWRDN pin is a digital input that allows the host controller to put the 73S8023C in its Power Down state. This pin can only be activated outside of a card session.
- The CLKOUT signal is a buffered output of the signal applied to the XTALIN pin whether it is an external clock source or it is configured as a crystal oscillator. CLKOUT can be used when using multiple 73S8023C devices to share a single clock signal.
- The STROBE input directly drives the smart card CLK signal when operating in synchronous mode. STROBE is ignored in asynchronous mode.

3 Oscillator

The 73S8023C device has an on-chip oscillator that can generate the smart card clock using an external crystal (connected between the pins XTALIN and XTALOUT) to set the oscillator frequency. When the card clock signal is available from another source, it can be connected to the pin XTALIN, and the pin XTALOUT should be left unconnected. Signal CLKOUT is the buffered version of the signal on XTALIN.

4 DC-DC Converter – Card Power Supply

An internal DC-DC converter provides the card power supply. This converter is able to provide either 3 V or 5 V card voltage from the power supply applied on the V_{DD} pin. The digital ISO-7816-3 sequencer controls the converter. Card voltage selection is carried out by the digital input 5V/$\overline{3V}$.

The circuit is an inductive step-up converter/regulator. The external components required are 2 filter capacitors on the power-supply input V_{DD} (next to the LIN pin, 100 nF + 10 µF), an inductor, and an output filter capacitor on the card power supply V_{CC}. The circuit performs regulation by activating the step-up operation when V_{CC} is below a set point of 5.0 or 3.0 volts minus a comparator hysteresis voltage and the input supply V_{DD} is less than the set point for V_{CC}. When V_{DD} is greater than the set point for V_{CC} (V_{DD} = 3.6 V, V_{CC} =3 V) the circuit operates as a linear regulator.

Depending on the inductor values, the voltage converter can provide current on V_{CC} as high as 100 mA. The circuit provides over-current protection and limits I_{CC} to 150 mA. When an over-current condition is sensed, the circuit initiates a deactivation sequence from the control logic and reports back to the host controller a fault on the interrupt output $\overline{OFF}$.

Choice of the inductor

The nominal inductor value is 10 µH, rated for 400 mA. The inductor is connected between LIN (pin 2) and the V_{DD} supply voltage. The inductor value can be optimized to meet a particular configuration (I_{CC_MAX}). The inductor should be located on the PCB as close as possible to the LIN pin of the IC.

Choice of the V_{CC} capacitor

Depending on the applications, the requirements in terms of both the V_{CC} minimum voltage and the transient currents that the interface must provide to the card are different. Table 1 shows the recommended capacitors for each V_{CC} power supply configuration and applicable specification.

Table 1: Choice of VCC Pin Capacitor

Specification Requirement			Application	
Specification	**Min V_{CC} Voltage Allowed During Transient Current**	**Max Transient Current Charge**	**Capacitor Type**	**Capacitor Value**
EMV 4.1	4.6 V	30 nAs	X5R/X7R w/ ESR < 100 mΩ	3.3 µF
ISO-7816-3	4.5 V	20 nAs		1 µF
NDS	4.65 V	40 nAs		3.3 µF

5 Voltage Supervision

Two voltage supervisors constantly check the presence of the voltages V_{DD} and V_{CC}. A card deactivation sequence is triggered upon a fault detected by these voltage supervisors.

The digital circuitry is powered by the power supply applied on the VDD pin. V_{DD} also defines the voltage range for the interface with the system controller. The V_{DD} Voltage supervisor is also used to initialize the ISO-7816-3 sequencer at power-on, and also to deactivate the card at power-off or upon a fault. The voltage threshold of the V_{DD} voltage supervisor is internally set by default to 2.3 V nominal. However, it may be desirable, in some applications, to modify this threshold value. The pin VDDF_ADJ (pin 17) is used to connect an external resistor R_{EXT} to ground to raise the V_{DD} fault voltage to another value, V_{DDF}. The resistor value is defined as follows:

$$R_{EXT} = 180\ k\Omega\ /(V_{DDF} - 2.33)$$

An alternative (more accurate) method of adjusting the V_{DD} fault voltage is to use a resistive network of R3 from the pin to supply and R1 from the pin to ground (see Figure 11: 73S8023C – Typical Application Schematic). In order to set the new threshold voltage, the equivalent resistance must be determined. This resistance value will be designated Kx. Kx is defined as R1/(R1+R3). Kx is calculated as:

$Kx = (2.649 / V_{TH}) - 0.6042$ where V_{TH} is the desired new threshold voltage.

To determine the values of R1 and R3, use the following formulas:

$R3 = 72000 / Kx$ $R1 = R3*(Kx / (1 – Kx))$

Taking the example above, where a V_{DD} fault threshold voltage of 2.7 V is desired, solving for Kx gives:

→ $Kx = (2.649 / 2.7) - 0.6042 = 0.377$

Solving for R3 gives: → $R3 = 72000 / 0.377 = 191\ k\Omega$.
Solving for R1 gives: → $R1 = 191000 *(0.377 / (1 – 0.377)) = 115.6\ k\Omega$.

Using standard 1 % resistor values gives R3 = 191 kΩ and R1 = 115 kΩ. These values give an equivalent resistance of Kx = 0.376, a 0.3% error.

Using 1% external resistors and a parallel resistance of 72 k ohms will result in a +/- 6% tolerance in the value of VDD Fault. The sources of variation due to integrated circuit process variations and mismatches include the internal reference voltage (less than +/- 1%), the internal comparator hysteresis and offset (less than +/- 1.7% for part-to-part, processing and environment), the internal resistor value mismatch and value variations (less than 1.8%), and the external resistor values (1%).

If the 2.3 V default threshold is acceptable, this pin must be left unconnected.

6 Power Down

A power down function is provided via the PWRDN pin (active high). When activated, the Power Down (PD) mode disables all the internal analog functions, including the card analog interface, the oscillators and the DC-DC converter, to put the 73S8023C in its lowest power consumption mode. PD mode is only allowed in the deactivated condition (out of a card session, when the $\overline{\text{CMDVCC}}$ signal is driven high from the host controller).

The host controller invokes the power down state when it is desirable to save power. The signals PRES and $\overline{\text{PRES}}$ remain functional in PD mode such that a card insertion sets $\overline{\text{OFF}}$ high. The micro-controller must then set PWRDN low and wait for the internal stabilization time prior to starting any card session (prior to turning $\overline{\text{CMDVCC}}$ low).

Resumption of the normal mode occurs approximately 10 ms (stabilization of the internal oscillators and reset of the circuitry) after PWRDN is set low. No card activation should be invoked during this 10 ms time period. If a card is present, $\overline{\text{OFF}}$ can be used as an indication that the circuit has completed its recovery from power-down state. $\overline{\text{OFF}}$ will go high at the end of the stabilization period. Should $\overline{\text{CMDVCC}}$ go low during PWRDN = 1, or within the 10 ms internal stabilization / reset time, it will not be taken into account and the card interface will remain inactive. Since $\overline{\text{CMDVCC}}$ is taken into account on its edges, it should be toggled high and low again after the 10 ms to activate a card.

Figure 2 illustrates the sequencing of the PD and Normal modes. PWRDN must be connected to GND if the power down function is not used.

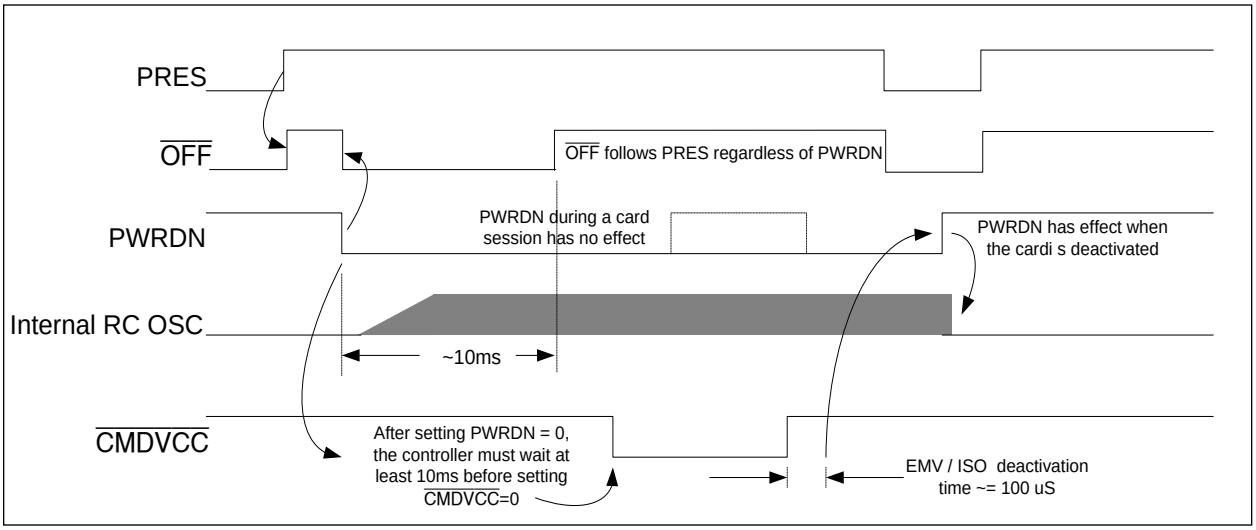


Figure 2: Power Down Mode Operation: CS = high

7 Over-temperature Monitor

A built-in detector monitors die temperature. When an over-temperature condition occurs, a card deactivation sequence is initiated, and an error or fault condition is reported to the system controller.

8 Activation and Deactivation

8.1 Activation Sequence (Synchronous Mode)

The 73S8023C smart card interface IC has an internal ~10 ms delay at power-on reset or on application of $V_{DD} > V_{DDF}$. No activation is allowed at this time. $\overline{CMDVCC}$ (edge triggered) must then be set low to activate the card.

The following steps list the activation sequence and the timing of the card control signals when the system controller sets $\overline{CMDVCC}$ low:

1. $\overline{CMDVCC}$ is set low.
2. Turn on V_{CC} and I/O (AUX1, AUX2) to reception mode at the end of (t_{ACT}).
3. RST is a copy of $\overline{RSTIN}$ and CLK is a copy of STROBE after (t_1).

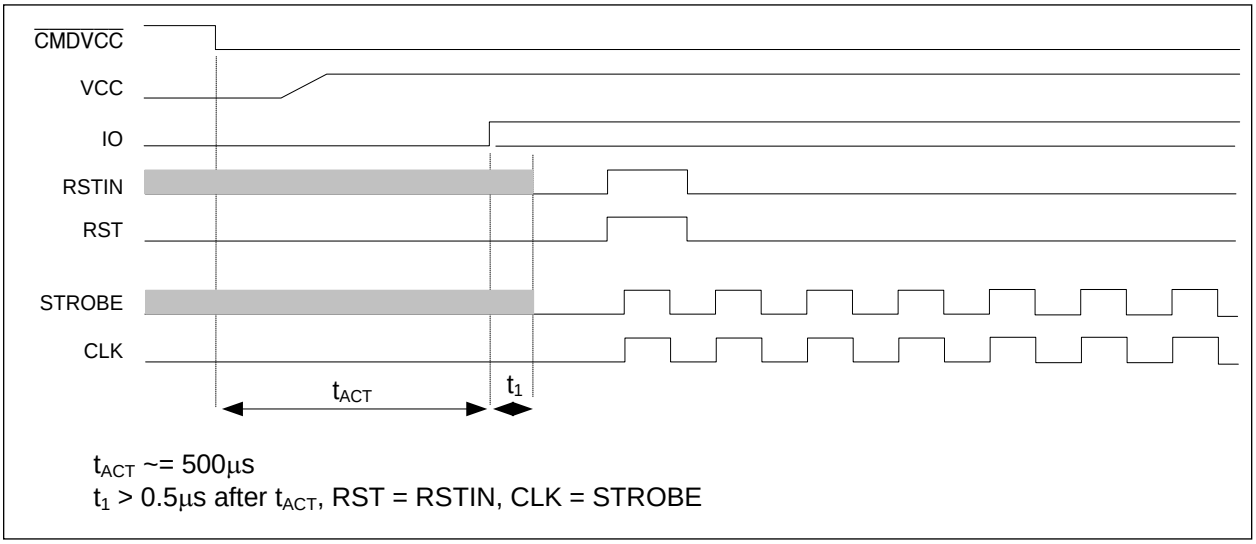


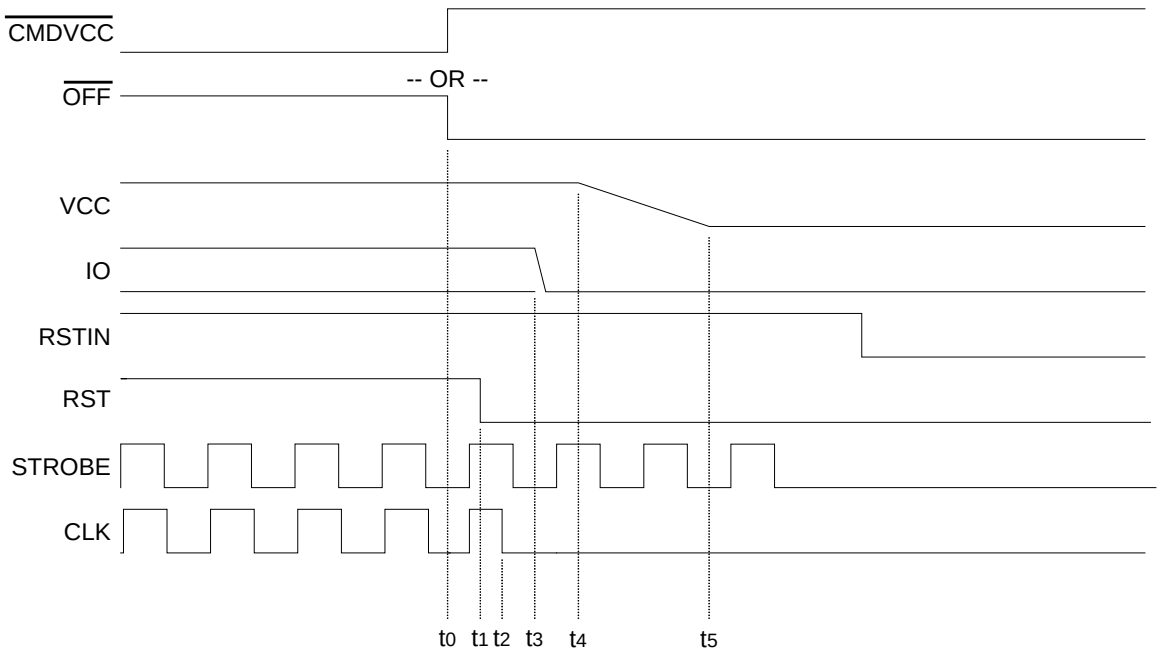
Figure 3: Activation Sequence – Synchronous Mode

8.2 Deactivation Sequence (Synchronous Mode)

Deactivation is initiated either by the system controller by setting the $\overline{CMDVCC}$ high, or automatically in the event of hardware faults. Hardware faults are over-current, overheating, V_{DD} fault and card extraction during the session and are indicated to the system controller by the fall of $\overline{OFF}$.

The following steps list the deactivation sequence and the timing of the card control signals when the system controller sets the $\overline{CMDVCC}$ high or a fault condition sets $\overline{OFF}$ low:

1. RST goes low at time t_1.
2. CLK stops low at time t_2.
3. I/O goes low at time t_3. Out of reception mode.
4. V_{CC} is shut down at time t_4. After a delay t_5 (discharge of the V_{CC} capacitor), V_{CC} is low.



t0 - Deactivation starts after **CMDVCC** is set high or **OFF** falls due to card removal or fault

t1 - RST falls approx. 0.5us after deactivation begins

t2 - CLK falls approx. 7.5us after RST falls

t3 - IO falls approx 2us after CLK falls

t4 - VCC is shut down

t5 - VCC goes to 0 after discharge of VCC capacitor, approx 100us after deactivation begins
(Note: Host should set STROBE low when $\overline{\text{CMDVCC}}$ is set high, otherwise CLK may be truncated. CLK truncation may occur if an $\overline{\text{OFF}}$ event is triggered)

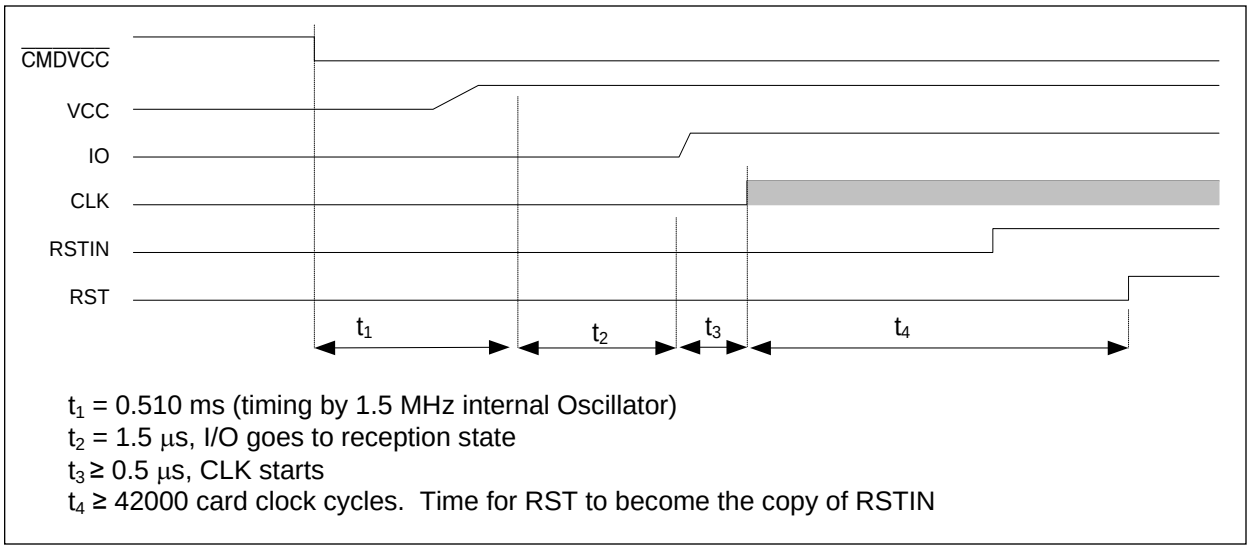
Figure 4: Synchronous Deactivation Operation – CKSEL = High

8.3 Activation Sequence (Asynchronous Mode)

The 73S8023C smart card interface IC has an internal 10 ms delay at power-on reset or upon application of $V_{DD} > V_{DDF}$ or upon exit of Power Down mode. The card interface may only be activated when $\overline{\text{OFF}}$ is high which indicates a card is present. No activation is allowed at this time. $\overline{\text{CMDVCC}}$ (edge triggered) must then be set low to activate the card.

The following steps list the activation sequence and the timing of the card control signals when the system controller sets $\overline{\text{CMDVCC}}$ low while the RSTIN is low:

1. $\overline{\text{CMDVCC}}$ is set low.
2. Next, the internal V_{CC} control circuit checks the presence of V_{CC} at the end of t_1. In normal operation, the voltage V_{CC} to the card becomes valid during t_1. If V_{CC} does not become valid, then $\overline{\text{OFF}}$ goes low to report a fault to the system controller, and the power V_{CC} to the card is turned off.
3. Turn I/O (AUX1, AUX2) to reception mode at the end of t_2.
4. CLK is applied to the card at the end of t_3.
5. RST is a copy of RSTIN after t_4. RSTIN may be set high before t_4, however the sequencer won't set RST high until 42000 clock cycles after the start of CLK.

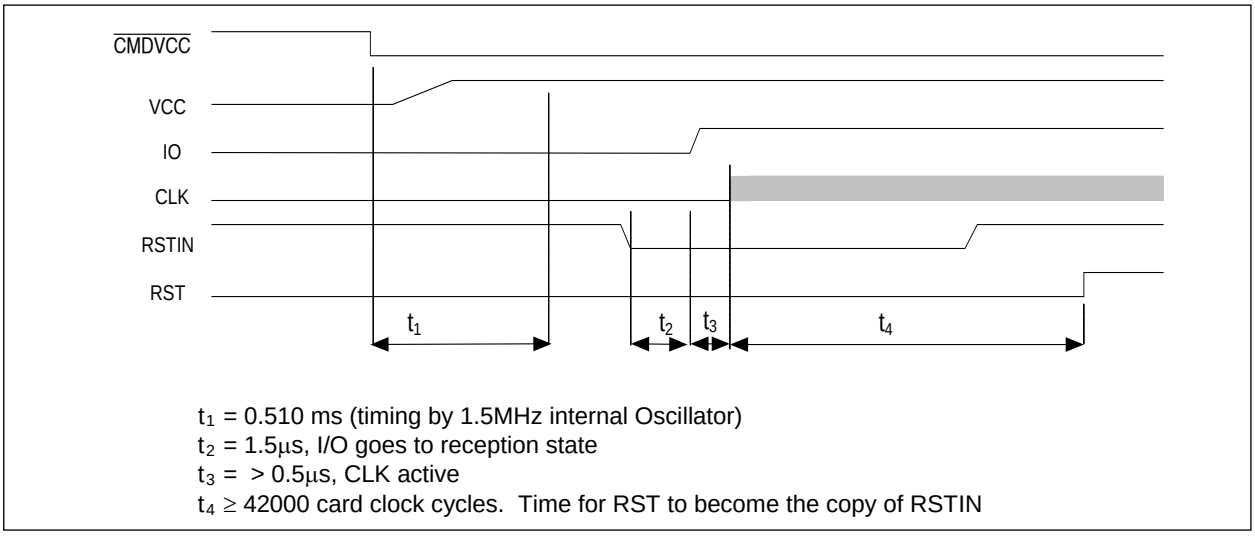


t_1 = 0.510 ms (timing by 1.5 MHz internal Oscillator)
t_2 = 1.5 μs, I/O goes to reception state
$t_3 \geq$ 0.5 μs, CLK starts
$t_4 \geq$ 42000 card clock cycles. Time for RST to become the copy of RSTIN

Figure 5: Asynchronous Activation Sequence – RSTIN Low When $\overline{\text{CMDVCC}}$ Goes Low

The following steps list the activation sequence and the timing of the card control signals when the system controller pulls the $\overline{\text{CMDVCC}}$ low while the RSTIN is high:

1. $\overline{\text{CMDVCC}}$ is set low.
2. Next, the internal V_{CC} control circuit checks the presence of V_{CC} at t_1. In normal operation, the voltage V_{CC} to the card becomes valid during this time. If not, $\overline{\text{OFF}}$ goes low to report a fault to the system controller, and the power V_{CC} to the card is turned off.
3. Due to the fall of RSTIN at t_2, turn I/O (AUX1, AUX2) to reception mode.
4. CLK is applied to the card at the end of t_3 after I/O is in reception mode.
5. RST is to be a copy of RSTIN after t_4. RSTIN may be set high before t_4, however the sequencer won't set RST high until 42000 clock cycles after the start of CLK.



t_1 = 0.510 ms (timing by 1.5MHz internal Oscillator)
t_2 = 1.5μs, I/O goes to reception state
t_3 = > 0.5μs, CLK active
$t_4 \geq$ 42000 card clock cycles. Time for RST to become the copy of RSTIN

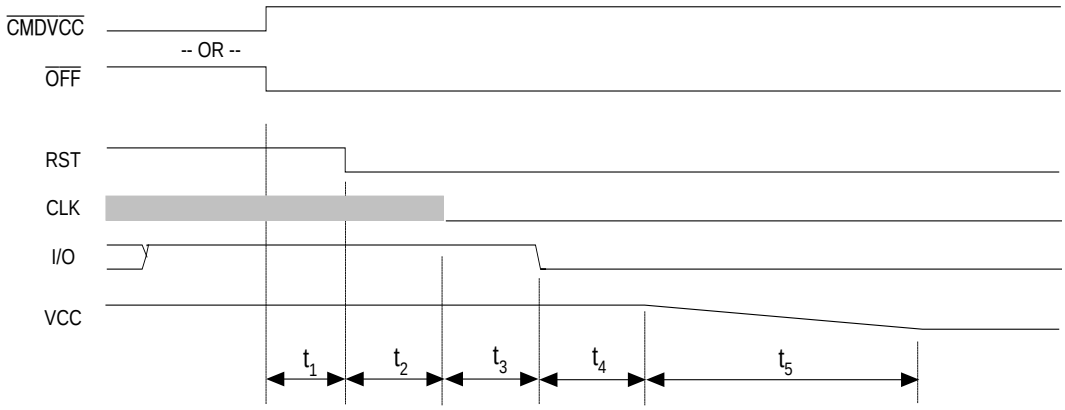
Figure 6: Asynchronous Activation Sequence – Timing Diagram #2

8.4 Deactivation Sequence (Asynchronous Mode)

Deactivation is initiated either by the system controller by setting $\overline{\text{CMDVCC}}$ high, or automatically in the event of hardware faults. Hardware faults are over-current, overheating, V_{DD} fault, V_{CC} fault, and card extraction during the session.

The following steps list the deactivation sequence and the timing of the card control signals when the system controller sets the $\overline{\text{CMDVCC}}$ high or $\overline{\text{OFF}}$ goes low due to a fault or card removal:

1. RST goes low at the end of time t_1.
2. CLK stops low at the end of time t_2.
3. I/O goes low at the end of time t_3. Out of reception mode.
4. V_{CC} is shut down at the end of time t_4. After a delay t_5 (discharge of the V_{CC} capacitor), V_{CC} is low.



$t_1 \geq 0.5\ \mu s$, timing by 1.5 MHz internal Oscillator
$t_2 \geq 7.5\ \mu s$ $t_3 \geq 0.5\ \mu s$ $t_4 \geq 0.5\ \mu s$
t_5 = depends on V_{CC} filter capacitor.
$t_1 + t_2 + t_3 + t_4 + t_5 \sim= 100\ \mu s$

Figure 7: Asynchronous Deactivation Sequence

9 $\overline{\text{OFF}}$ and Fault Detection

There are two cases for which the system controller can monitor the $\overline{\text{OFF}}$ signal: to query regarding the card presence outside card sessions, or for fault detection during card sessions.

Monitoring Outside a Card Session

In this condition, $\overline{\text{CMDVCC}}$ is always high, $\overline{\text{OFF}}$ is low if the card is not present, and high if the card is present. Because it is outside a card session, any fault detection will not act upon the $\overline{\text{OFF}}$ signal. No deactivation is required during this time.

Monitoring During a Card Session

$\overline{\text{CMDVCC}}$ is always low, and $\overline{\text{OFF}}$ falls low if the card is extracted or if any fault is detected. At the same time that $\overline{\text{OFF}}$ is set low, the sequencer starts the deactivation process.

Figure 8 shows the timing diagram for the signals $\overline{\text{CMDVCC}}$, PRES, and $\overline{\text{OFF}}$ during a card session and outside the card session:

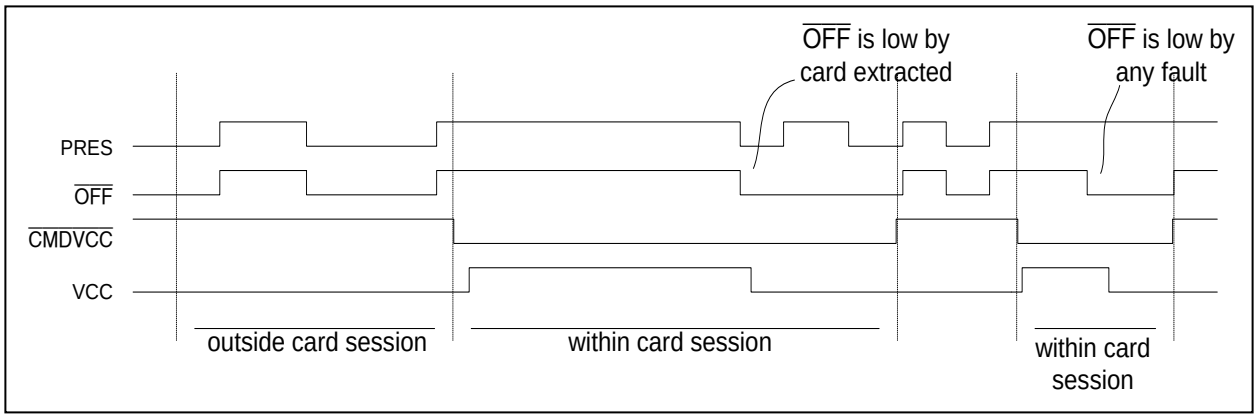


Figure 8: Timing Diagram – Management of the Interrupt Line $\overline{OFF}$

10 I/O Circuitry and Timing

The I/O, AUX1, and AUX2 pins are in the low state after power-on reset and they are in the high state when the activation sequencer turns on the I/O reception state. See Section 8 Activation and Deactivation for more details on when the I/O reception is on.

The state of the I/OUC, AUX1UC, and AUX2UC pins is high after power-on reset. Within a card session and when the I/O reception state is on, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line. When the input I/O line rising edge is detected, both I/O lines return to their neutral state.

Figure 9 shows the state diagram of how the I/O and I/OUC lines are managed to become input or output. The delay between the I/O signals is shown in Figure 10.

In order to be compliant to the NDS specifications, a 27 pF capacitor must be added between pins I/O (C7) and GND (C5) at the smart card connector.

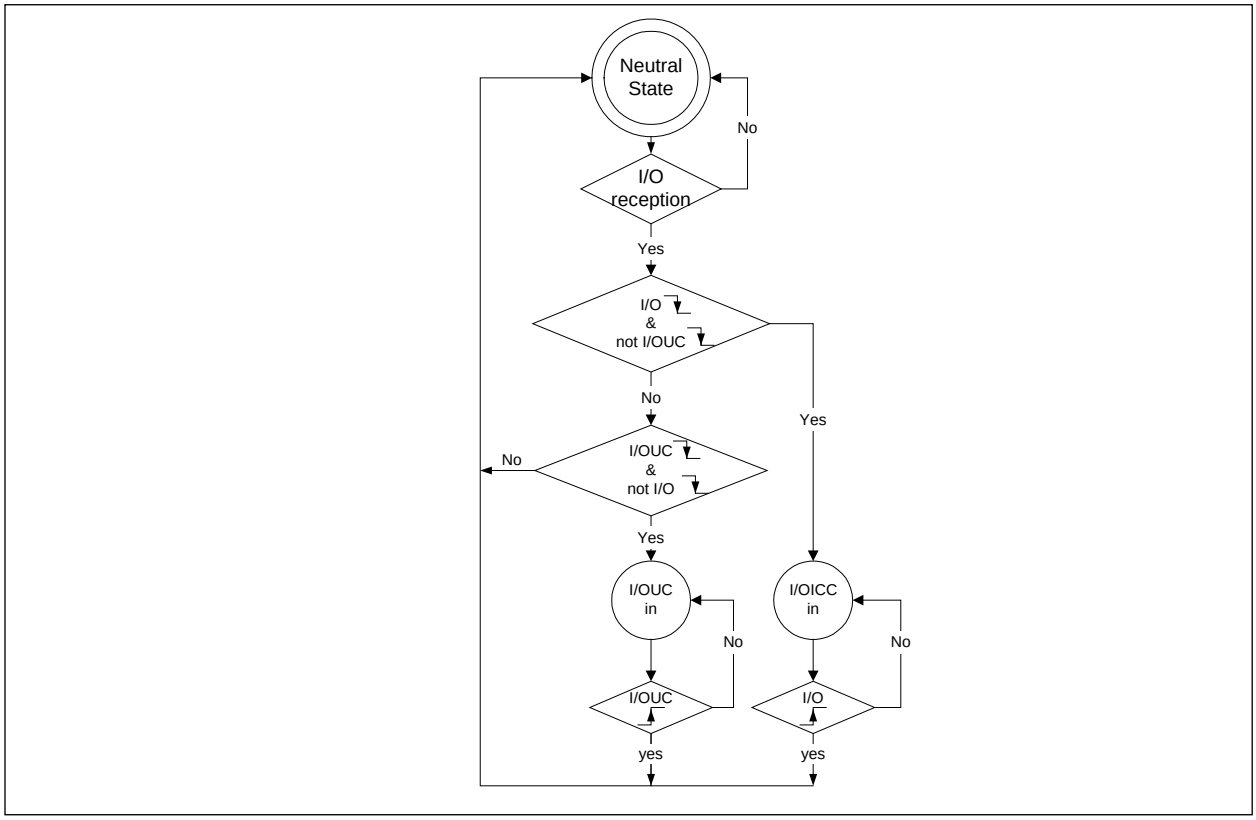


Figure 9: I/O and I/OUC State Diagram

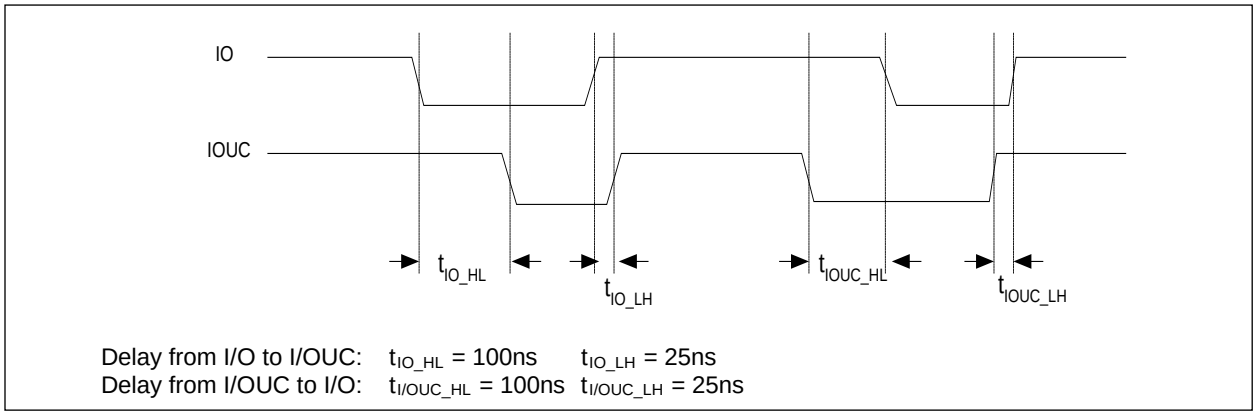


Figure 10: I/O – I/OUC Delays Timing Diagram

11 Typical Application Schematic

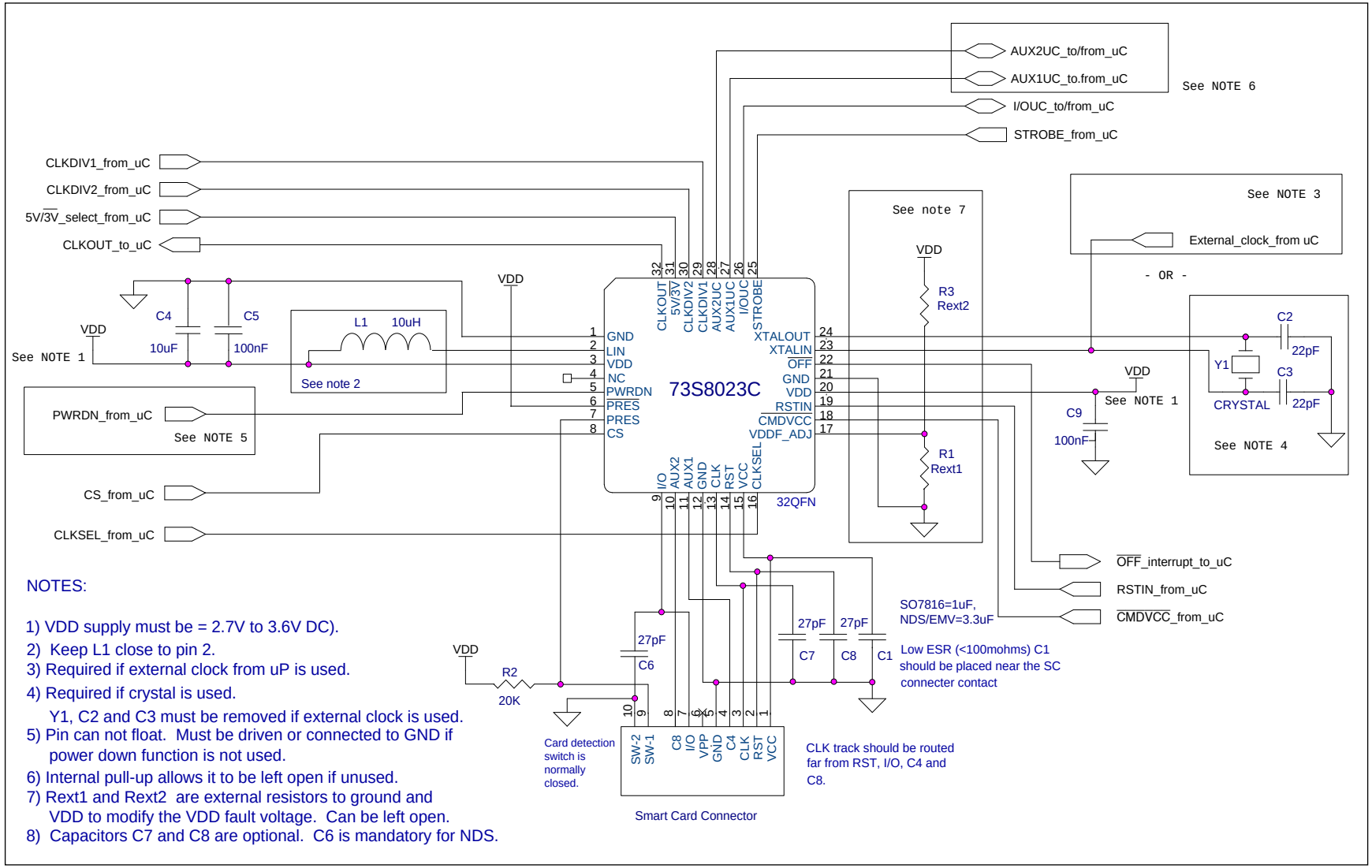


Figure 11: 73S8023C – Typical Application Schematic

12 Electrical Specification

12.1 Absolute Maximum Ratings



Operation outside these rating limits may cause permanent damage to the device.

Parameter	Rating
Supply Voltage V_{DD}	-0.5 to 4.0 VDC
Input Voltage for Digital Inputs	-0.3 to (V_{DD} +0.5) VDC
Storage Temperature	-60 °C to 150 °C
Pin Voltage (except LIN and card interface)	-0.3 to (V_{DD} +0.5) VDC
Pin Voltage (LIN)	-0.3 to 6.0 VDC
Pin Voltage (card interface)	-0.3 to (V_{CC} + 0.5) VDC
ESD Tolerance – Card interface pins	+/- 6 kV
ESD Tolerance – Other pins	+/- 2 kV



ESD testing on Card pins uses the HBM condition, 3 pulses, each polarity referenced to ground. The smart card pins are protected against shorting between any combination of smart card pins.

12.2 Recommended Operating Conditions

Parameter	Rating
Supply Voltage V_{DD}	2.7 to 3.6 VDC
Ambient Operating Temperature	-40 °C to +85 °C
Input Voltage for Digital Inputs	0 V to V_{DD} + 0.3 V

12.3 Package Thermal Parameters

Package	Rating
32QFN	47 °C / W (with bottom pad soldered)
32QFN	78 °C / W (without bottom pad soldered)

12.4 Card Interface Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Card Power Supply (V_{CC}) DC-DC Converter General conditions, -40 °C < T < 85 °C, 2.7 V < V_{DD} < 3.6 V						
V_{CC}	Card supply voltage including ripple and noise	Inactive mode	-0.1		0.1	V
		Inactive mode I_{CC} =1 mA	-0.1		0.4	V
		Active mode I_{CC} < 65 mA; 5 V	4.75		5.25	V
		Active mode I_{CC} < 65 mA; 3 V	2.8		3.2	V
		Active mode single pulse of 100 mA for 2 µs; 5 V, fixed load = 25 mA	4.65		5.25	V
		Active mode single pulse of 100 mA for 2 µs; 3 V, fixed load = 25 mA	2.76		3.2	V
		Active mode current pulses of 40 nAs with peak $\|I_{CC}\|$ < 200 mA, t < 400 ns; 5 V	4.65		5.25	V
		Active mode current pulses of 40 nAs with peak $\|I_{CC}\|$ < 200 mA, t < 400 ns; 3 V	2.76		3.2	V
V_{CCR}	VCC Ripple				350	mV
I_{CCmax}	Maximum supply current to the card	Static load current V_{CC} > 4.6 or 2.7 V as selected, L=10 µH	100			mA
I_{CCF}	I_{CC} fault current		100	125	180	mA
V_{SR}	V_{CC} slew rate – Rise rate on activate	C_F on V_{CC} = 1 uF	0.05	0.15	0.25	V/µs
V_{SF}	V_{CC} slew rate – Fall rate on deactivate	C_F on V_{CC} = 1 uF	0.1	0.3	0.5	V/µs
C_F	External filter capacitor (V_{CC} to GND)		0.47	3.3	4.7	µF
L	Inductor (LIN to V_{DD})			10		µH
Limax	Imax in inductor	V_{CC} = 5 V, I_{CC} = 65 mA, V_{DD} = 2.7 V			400	mA
η	Efficiency	V_{CC} = 5 V, I_{CC} = 65 mA, V_{DD} = 3.3 V		87		%

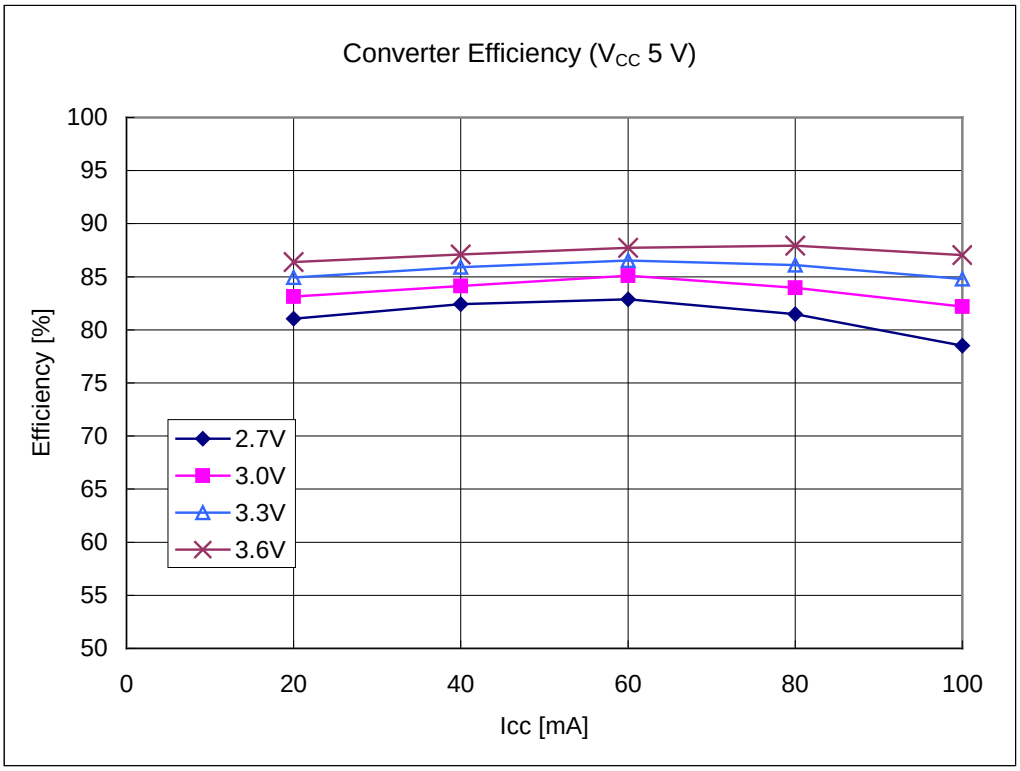


Figure 12: DC – DC Converter efficiency (V_{CC} = 5 V)

Output current on Vcc at 5 V. Input voltage on V_{DD} at 2.7, 3.0, 3.3 and 3.6 volts.

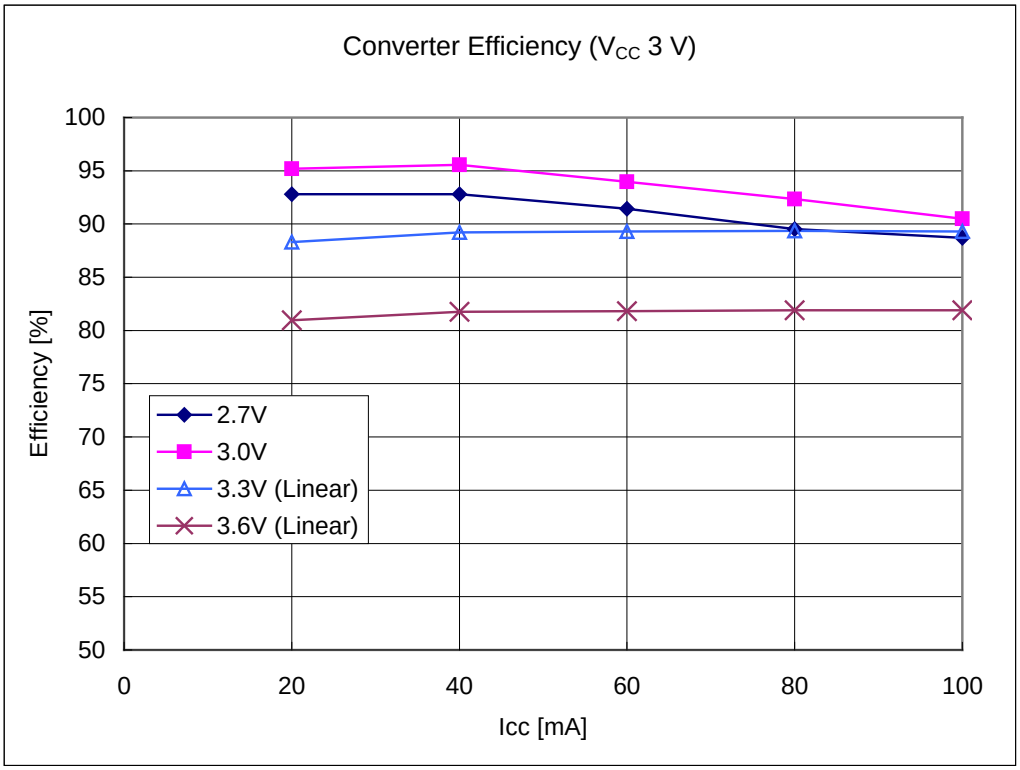


Figure 13: DC – DC Converter Efficiency (V_{CC} = 3 V)

Output current on Vcc at 3 V. Input voltage on V_{DD} at 2.7, 3.0, 3.3 and 3.6 volts.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Interface Requirements – Data Signals: I/O, AUX1, AUX2, and host interfaces: I/OUC, AUX1UC, AUX2UC. I_{SHORTL}, I_{SHORTH}, and V_{INACT} requirements do not pertain to I//OUC, AUX1UC, and AUX2UC.						
V_{OH}	Output level, high (I/O, AUX1, AUX2)	I_{OH} = 0[1]	0.9 V_{CC}		V_{CC}+ 0.1	V
		I_{OH} = -40 µA	0.75 V_{CC}		V_{CC} + 0.1	V
V_{OH}	Output level, high (I/OUC, AUX1UC, AUX2UC)	I_{OH} = 0	0.9 V_{DD}		V_{DD} + 0.1	V
		I_{OH} = -40 µA	0.75 V_{DD}		V_{DD} + 0.1	V
V_{OL}	Output level, low	I_{OL}=1 mA			0.3	V
V_{IH}	Input level, high (I/O, AUX1, AUX2)		1.8		V_{CC} + 0.30	V
V_{IH}	Input level, high (I/OUC, AUX1UC, AUX2UC)		1.8		V_{DD} + 0.30	V
V_{IL}	Input level, low		-0.3		0.8	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1 mA			0.3	V
I_{LEAK}	Input leakage	V_{IH} = V_{CC}			10	µA
I_{IL}	Input current, low (I/OUC, AUX1UC, AUX2UC)	V_{IL} = 0, CS = 1			0.65	mA
		V_{IL} = 0, CS = 0			5	µA
	Input current, low (I/O, AUX1, AUX2)	V_{IL} = 0			2	mA
I_{SHORTL}	Short circuit output current	For output low, shorted to V_{CC} through 33 Ω			15	mA
I_{SHORTH}	Short circuit output current	For output high, shorted to ground through 33 Ω			15	mA
t_R, t_F	Output rise time, fall times	C_L = 80 pF, 10% to 90%. For I/OUC, AUX1UC, AUX2UC, C_L = 50 pF			100	ns
t_{IR}, t_{IF}	Input rise, fall times				1	µs
R_{PU}	Internal pull-up resistor	Output stable for > 200 ns	8	11	14	kΩ
Ipuhiz	Pull-up current, Hi-Z state	For pins IOUC, AUX1UC, AUX2UC when CS = 0			5	µA
FD_{MAX}	Maximum data rate				1	MHz
T_{FDIO}	Delay, I/O to I/OUC, I/OUC to I/O (falling edge to falling edge)			100	Started	ns
	Delay, I/O to I/OUC, I/OUC to I/O (rising edge to rising edge)			10		
C_{IN}	Input capacitance				10	pF

[1] NDS applications require a 27 pF capacitor on I/O placed at the smart card connector.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Reset and Clock for card interface, RST, CLK						
V_{OH}	Output level, high	I_{OH} = -200 µA	0.9 V_{CC}		V_{CC}	V
V_{OL}	Output level, low	I_{OL}= 200 µA	0		0.2	V
V_{INACT}	Output voltage when outside of a session	I_{OL} = 0			0.1	V
		I_{OL} = 1 mA			0.3	V
I_{RST_LIM}	Output current limit, RST				30	mA
I_{CLK_LIM}	Output current limit, CLK				70	mA
t_R, t_F	Output rise time, fall time	C_L = 35 pF for CLK, 10% to 90%			8	ns
		C_L = 200 pF for RST, 10% to 90%			100	ns
Td	Delay time STROBE to CLK, RSTIN to RST	CLKSEL = 1, Cap. load on CLK and RST is minimal, else rise, fall times are a factor			20	ns
δ	Duty cycle for CLK	C_L = 35 pF, 48% < δ_{IN} < 52%	45		55	%

12.5 Digital Signals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Digital I/O Except for OSC I/O						
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		1.8		V_{DD} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -1 mA	V_{DD} - 0.45			V
R_{OUT}	Pull-up resistor, $\overline{OFF}$			20		kΩ
t_{SL}	Time from CS going high to interface active		50			ns
t_{DZ}	Time from CS going low to interface inactive, Hi-Z		50			ns
t_{IS}	Set-up time, control signals to CS rising edge		50			ns
t_{SI}	Hold time, control signals from CS rising edge				50	ns
t_{ID}	Set-up time, control signals to CS fall		50			ns
t_{DI}	Hold time, control signals from CS fall				50	ns
$\|I_{IL1}\|$	Input Leakage Current	GND < V_{IN} < V_{DD}	-5		5	µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Oscillator (XTALIN) I/O Parameters						
V_{ILXTAL}	Input Low Voltage - XTALIN		-0.3		0.3 V_{DD}	V
V_{IHXTAL}	Input High Voltage - XTALIN		0.7 V_{DD}		V_{DD}+0.3	V
I_{ILXTAL}	Input Current - XTALIN	GND < V_{IN} < V_{DD}	-30		30	µA
f_{MAX}	Max freq. Osc or external clock				27	MHz
δin	External input duty cycle limit	$t_{R/F}$ < 10% f_{IN}, 45% < δ_{CLK} < 55%	48		52	%

12.6 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current on V_{DD}	Linear mode, ICC = 0 I/O, AUX1, AUX2 = high		4.9		mA
		Step up mode, ICC = 0 I/O, AUX1, AUX2 = high		4.7		mA
I_{DD_PD}	Supply Current on V_{DD} in Power Down mode	PWRDN = 1, Start/stop bit = 0 All digital inputs driven with a true logical 0 or 1		0.11	2.5	µA

12.7 Voltage / Temperature Fault Detection Circuits

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDF}	V_{DD} fault – V_{DD} Voltage supervisor threshold)	No external resistor on VDDF_ADJ	2.15		2.4	V
V_{CCF}	V_{CC} fault – V_{CC} Voltage supervisor threshold	V_{CC} = 5 V	4.20		4.6	V
		V_{CC}= 3 V	2.5		2.7	V
T_F	Die over temperature fault		115		145	°C
I_{CCF}	Card over current fault		100		150	mA

13 Mechanical Drawing (32-QFN)

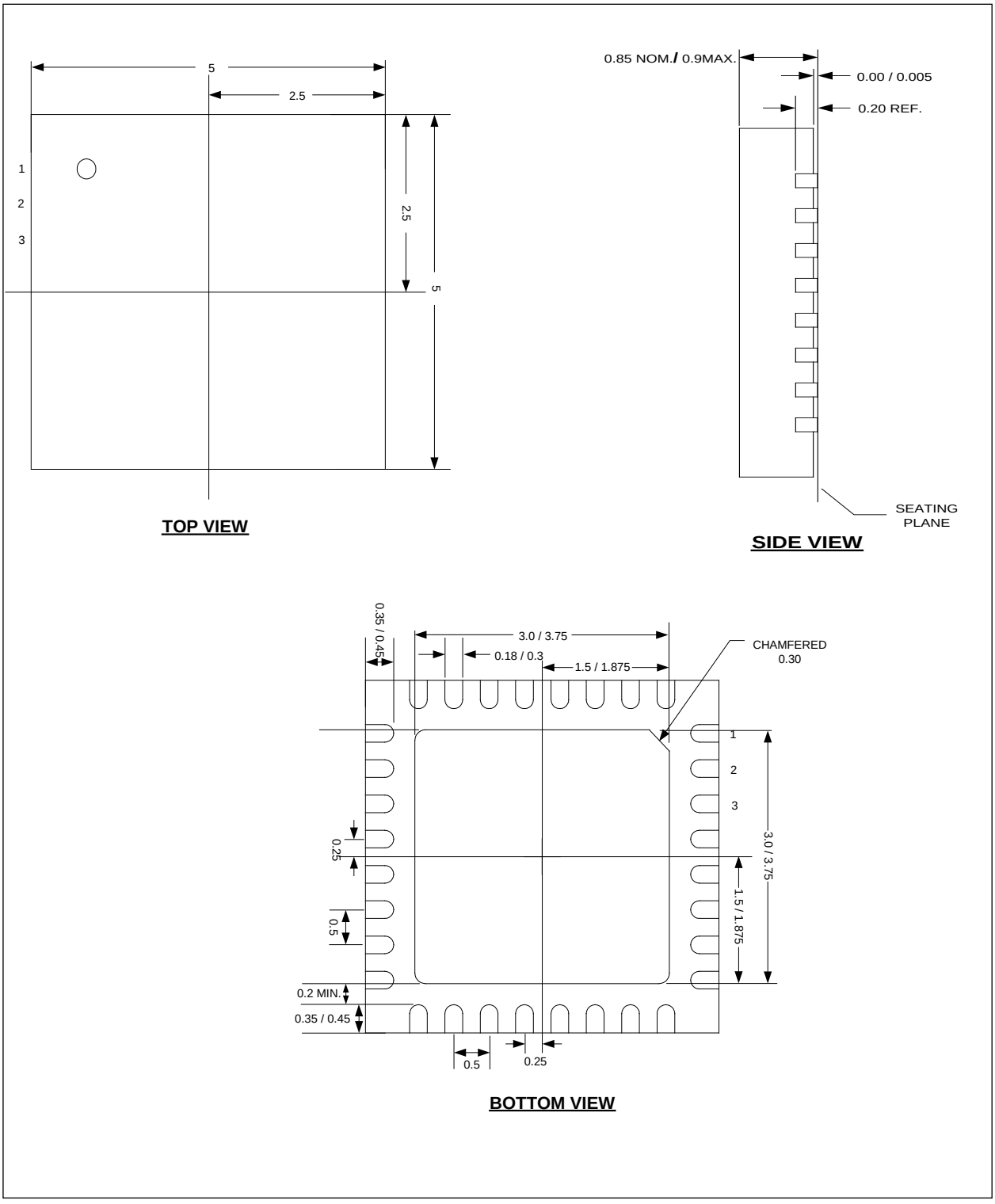
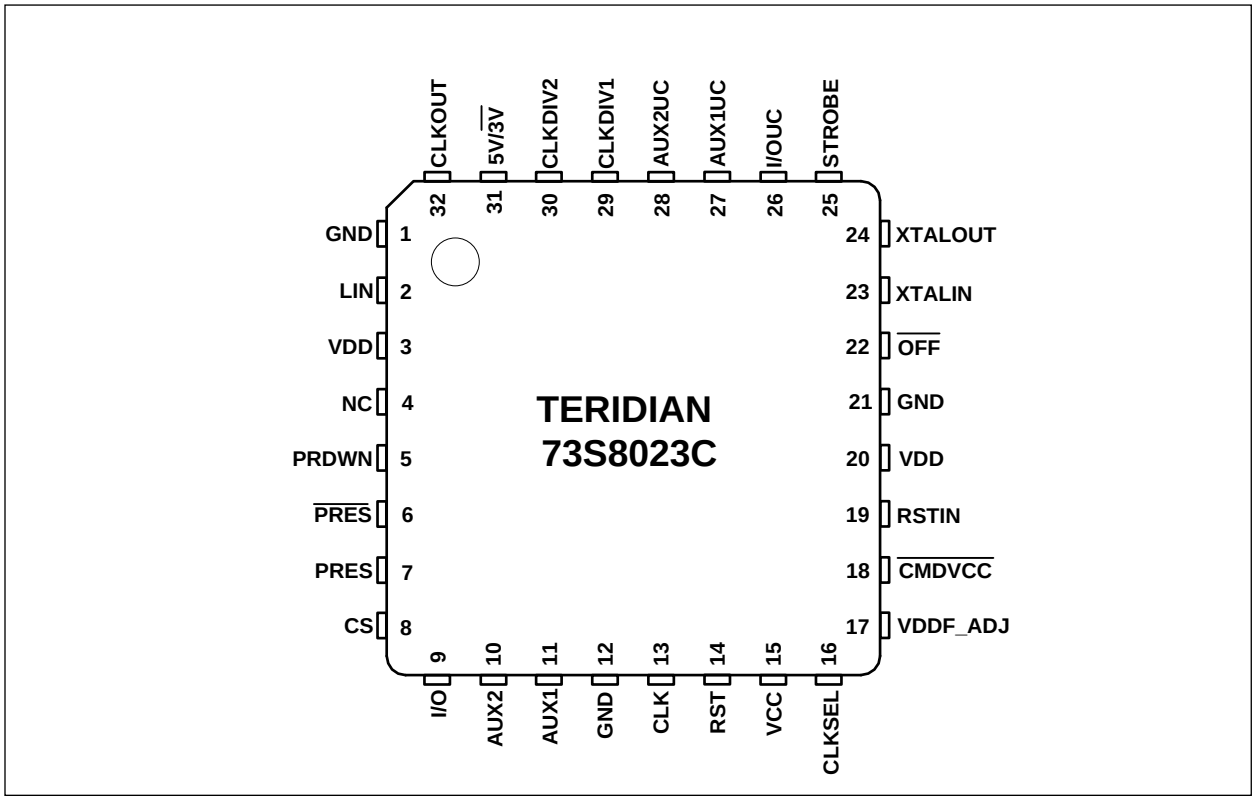


Figure 14: 32-QFN Mechanical Drawing

14 Package Pin Designation (32-QFN)



Use handling procedures necessary for a static sensitive component.



(Top View)

Figure 15: 32-QFN 73S8023C Pin Out

15 Ordering Information

Part Description	Order Number	Packaging Mark
73S8023C-QFN 32-pin Lead-Free QFN	73S8023C-IM/F	73S8023C
73S8023C-QFN 32-pin Lead-Free QFN Tape / Reel	73S8023C-IMR/F	73S8023C

16 Related Documentation

The following 73S8023C documents are available from Teridian Semiconductor Corporation:

73S8023C Data Sheet (this document)
73S8023C QFN Demo Board User's Guide

17 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S8023C, contact us at:

6440 Oak Canyon Road
Suite 100
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: scr.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	6/13/2005	First publication.
1.1	7/15/2005	Converted to Teridian format.
1.2	12/5/2007	Add EMV and ISO logo, remove leaded package option, change 32QFN punched to SAWN package.
1.3	1/17/2008	Changed dimension of bottom exposed pad on 32QFN mechanical package figure.
1.4	1/8/2009	Added NDS logo to page 1 and assigned document number.
1.5	4/3/2009	Removed all references to VPC as VPC must be tied to VDD.

© 2009 Teridian Semiconductor Corporation. All rights reserved.
Teridian Semiconductor Corporation is a registered trademark of Teridian Semiconductor Corporation.
Simplifying System Integration is a trademark of Teridian Semiconductor Corporation.
All other trademarks are the property of their respective owners.

Teridian Semiconductor Corporation makes no warranty for the use of its products, other than expressly contained in the Company's warranty detailed in the Teridian Semiconductor Corporation standard Terms and Conditions. The company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice and does not make any commitment to update the information contained herein. Accordingly, the reader is cautioned to verify that this document is current by comparing it to the latest version on http://www.teridian.com or by checking with your sales representative.

Teridian Semiconductor Corp., 6440 Oak Canyon Rd., Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.Teridian.com