TERIDIAN SEMICONDUCTOR CORP.

Simplifying System Integration™

73S1210F
Evaluation Board User Guide

August 18, 2009
Rev. 1.2
UG_1210F_035

© 2009 Teridian Semiconductor Corporation. All rights reserved.
Teridian Semiconductor Corporation is a registered trademark of Teridian Semiconductor Corporation.
Simplifying System Integration is a trademark of Teridian Semiconductor Corporation.
Microsoft, Windows and Vista are registered trademarks of Microsoft Corporation.
Signum is a trademark of Signum Systems Corporation.
Keil is a trademark of ARM® Ltd.
All other trademarks are the property of their respective owners.

Teridian Semiconductor Corporation makes no warranty for the use of its products, other than expressly contained in the Company's warranty detailed in the Teridian Semiconductor Corporation standard Terms and Conditions. The company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice and does not make any commitment to update the information contained herein. Accordingly, the reader is cautioned to verify that this document is current by comparing it to the latest version on http://www.teridian.com or by checking with your sales representative.

Teridian Semiconductor Corp., 6440 Oak Canyon, Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.teridian.com

Table of Contents

1 Introduction 4
1.1 Evaluation Kit Contents 5
1.2 Evaluation Board Features 5
1.3 Recommended Equipment and Test Tools 5
2 Evaluation Board Setup 6
2.1 Connecting the Evaluation Board with an Emulation Tool 7
2.2 Loading User Code into the Evaluation Board 8
3 Using the PCCID Application 10
3.1 Host Demonstration Software Installation 10
4 Evaluation Board Hardware Description 11
4.1 Jumpers, Switches and Modules 11
4.2 Test Points 16
4.3 Schematic 17
4.4 PCB Layouts 18
4.5 Bill of Materials 24
4.6 Schematic Information 26
4.6.1 Reset Circuit 26
4.6.2 Oscillator 26
4.6.3 LCD 27
4.6.4 Smart Card Interface 28
5 Ordering Information 29
6 Related Documentation 29
7 Contact Information 29
Revision History 30

Figures

Figure 1: 1210F Evaluation Board 4
Figure 2: 73S1210F Evaluation Board Basic Connections 6
Figure 3: 73S1210F Evaluation Board Basic Connections with ADM-51 ICE 7
Figure 4: Emulator Window Showing RESET and ERASE Buttons 9
Figure 5: Emulator Window Showing Erased Flash Memory and File Load Menu 9
Figure 6: 73S1210F Evaluation Board Jumper, Switch and Module Locations 15
Figure 7: 73S1210F Evaluation Board Electrical Schematic 17
Figure 8: 73S1210F Evaluation Board Top View (Silkscreen) 18
Figure 9: 73S1210F Evaluation Board Bottom View (Silkscreen) 19
Figure 10: 73S1210F Evaluation Board Top Signal Layer 20
Figure 11: 73S1210F Evaluation Board Middle Layer 1 – Ground Plane 21
Figure 12: 73S1210F Evaluation Board Middle Layer 2 – Supply Plane 22
Figure 13: 73S1210F Evaluation Board Bottom Signal Layer 23
Figure 14: External Components for RESET 26
Figure 15: Oscillator Circuit 26
Figure 16: LCD Connections 27
Figure 17: Smart Card Connections 28

Tables

Table 1: Flash Programming Interface Signals 8
Table 2: Evaluation Board Jumper, Switch and Module Description 11
Table 3: Evaluation Board Test Point Description 16
Table 4: 73S1210F Evaluation Board Bill of Materials 24

1 Introduction

The Teridian Semiconductor Corporation (TSC) 73S1210F Evaluation Board is used to demonstrate the capabilities of the 73S1210F Smart Card Controller devices. It has been designed to operate either as a standalone or as a development platform.

The 73S1210F Evaluation Board can be programmed to run any of the Teridian turnkey applications or a user-developed custom application. Teridian provides its USB CCID application preloaded on the board and an EMV testing application on the CD.

Applications can be downloaded through the In-Circuit-Emulator (ICE) or through the TSC Flash Programmer Model TFP2. As a development tool, the evaluation board can operate in conjunction with an ICE to develop and debug 73S1210F based embedded applications.



The 73S1210F Evaluation Board uses the same PWB as the 73S1217F. The 73S1217F has some features that the73S1210F does not contain. These include the 32 kHz oscillator and USB interface. These features are depopulated on the 73S1210F Evaluation Board.

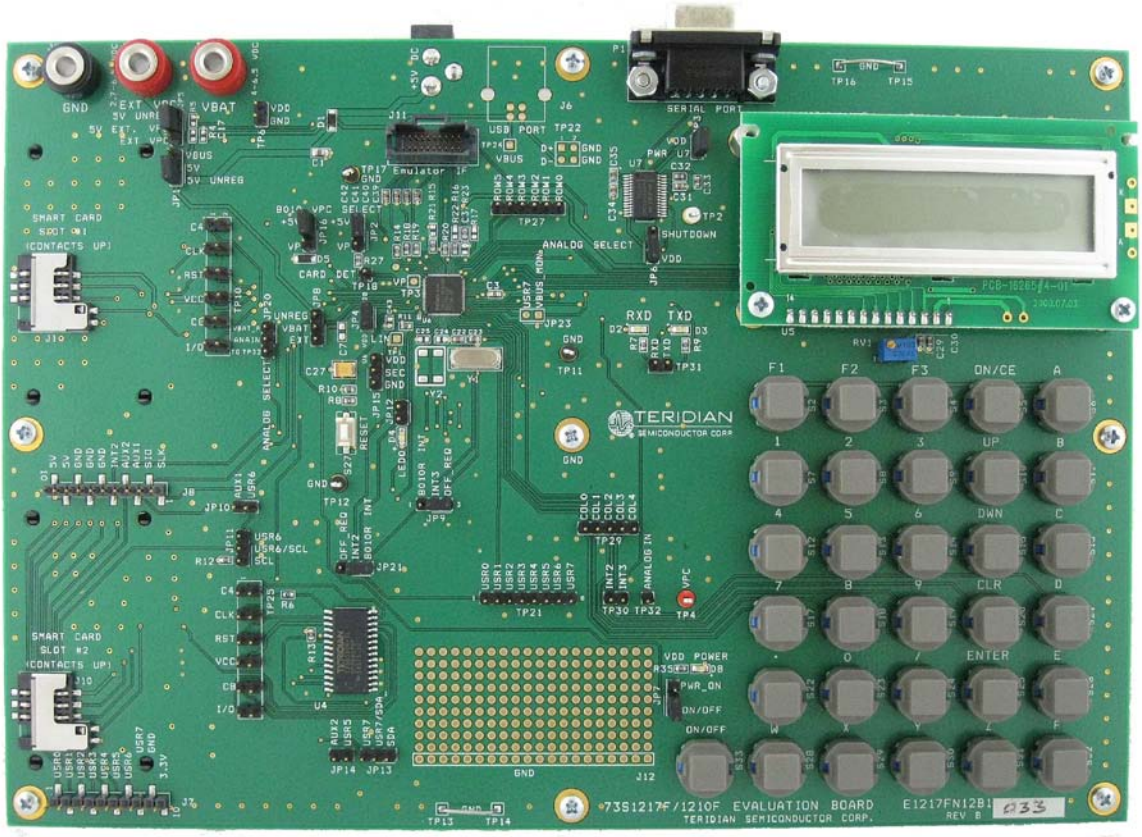


Figure 1: 1210F Evaluation Board

1.1 Evaluation Kit Contents

The 73S1210F Evaluation Kit contains the following:

- 73S1210F Evaluation Board: 4-layer, rectangular PCB as shown in Figure 1 (identification number E1217FN12B1 Rev B), containing the 73S1210F with the preloaded Pseudo-CCID (PCCID) program.
- 5 VDC/1,000 mA universal wall transformer with 1.0 mm plug ID (CUI Inc. – EPAS-101W-05).
- Serial cable: DB9, male/female, 2 meter length (Digi-Key AE1379-ND).
- CD containing documentation (data sheet, and user guides), Software API libraries, evaluation code, and utilities.
- The 73S1210F Evaluation Board Lite Quick Start Guide document.

1.2 Evaluation Board Features

The 73S1210F Evaluation Board (see Figure 1) includes the following:

- RS-232 interface
- Dual smart card interface
- ICE/Programmer interface
- 2 line x 16 character LCD module
- 6 x 5 Keypad
- 1 LED

1.3 Recommended Equipment and Test Tools

The following equipment and tools (not provided) are recommended for use with the 73S1210F Evaluation Kit:

- For functional evaluation: PC with Microsoft® Windows® XP or Vista® equipped with an RS232 (COM) port with DB9 connector.
- For software development (MPU code)
  - Signum™ ICE (In Circuit Emulator): ADM-51. Refer to http://signum.temp.veriohosting.com/Signum.htm.
  - Keil™ 8051 C Compiler Kit: CA51. Refer to http://www.keil.com/c51/ca51kit.htm, and http://www.keil.com/product/sales.htm

2 Evaluation Board Setup

Figure 2 shows the basic connections of the evaluation board with the external equipment.

The power supply can come from two sources:

- A regulated lab power supply connected to the banana plugs J2, J3 and J5.
- Any AC-DC converter block, able to generate a DC power supply of 2.7 V min / 6.5 V max / 400 mA.

The communication with an external host is accommodated via a standard RS-232 serial interface (TX/RX only).

The board is loaded by default with the PCCID application. It requires a PC to be connected through its serial port. When powered-up, the board is able to run with the PC Exerciser host application. Refer to the *73S1210F Evaluation Board Quick Start Guide* to setup and run the PCCID application.

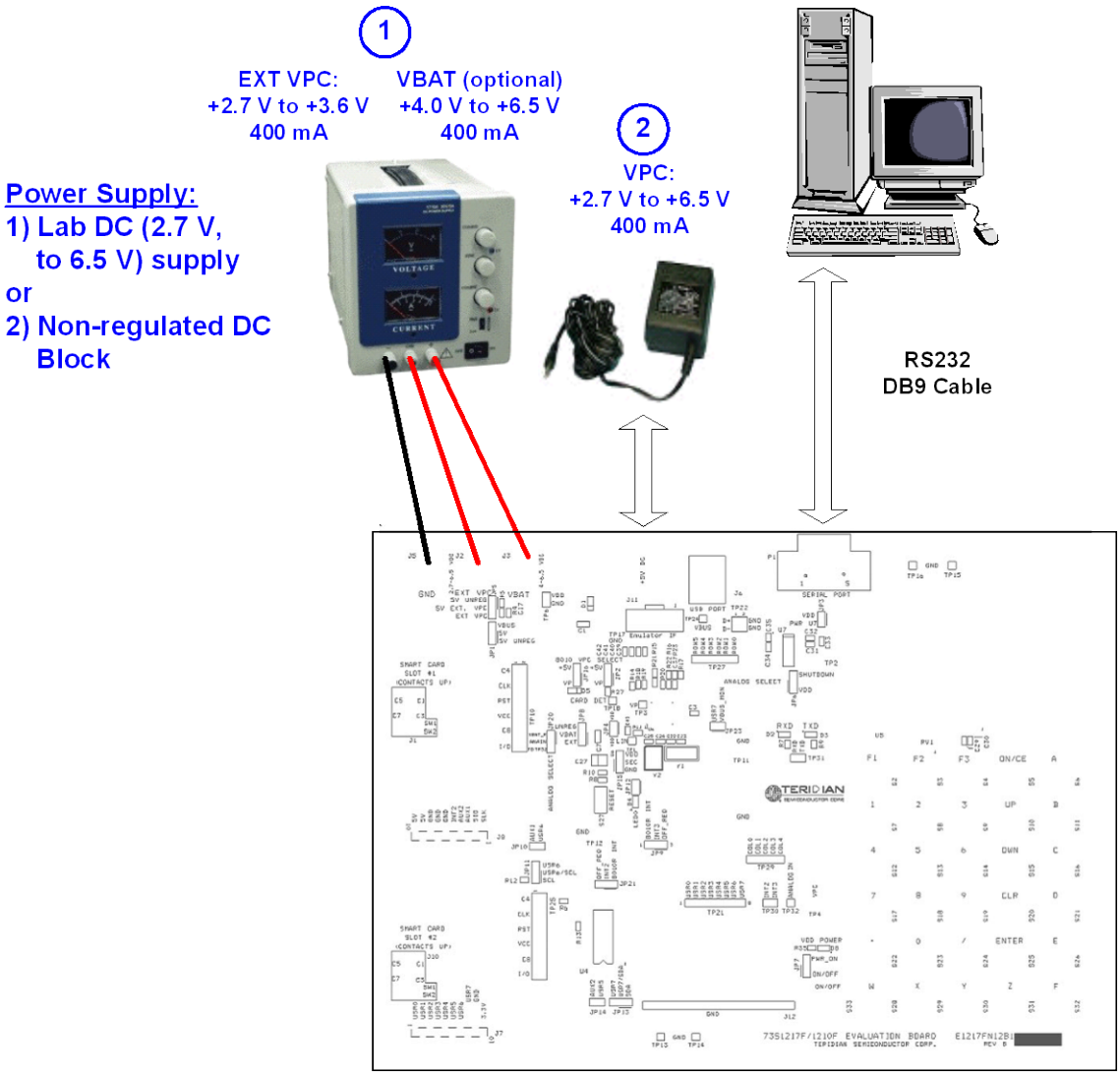


Figure 2: 73S1210F Evaluation Board Basic Connections

2.1 Connecting the Evaluation Board with an Emulation Tool

The 73S1210F Evaluation Board has been designed to operate with an In-Circuit-Emulator (ICE) from Signum Systems (model ADM-51). Figure 3 shows the connections between the ICE and the evaluation board. The Signum System POD has a ribbon cable that must be directly attached to connector J11.

Signum Systems offers different POD options depending on user needs. The standard pod allows users to perform typical emulator functions such as symbolic debugging, in-line breakpoints, memory examination/modification, etc. Other pod options enable code trace capability and/or complex breakpoints at an additional cost.

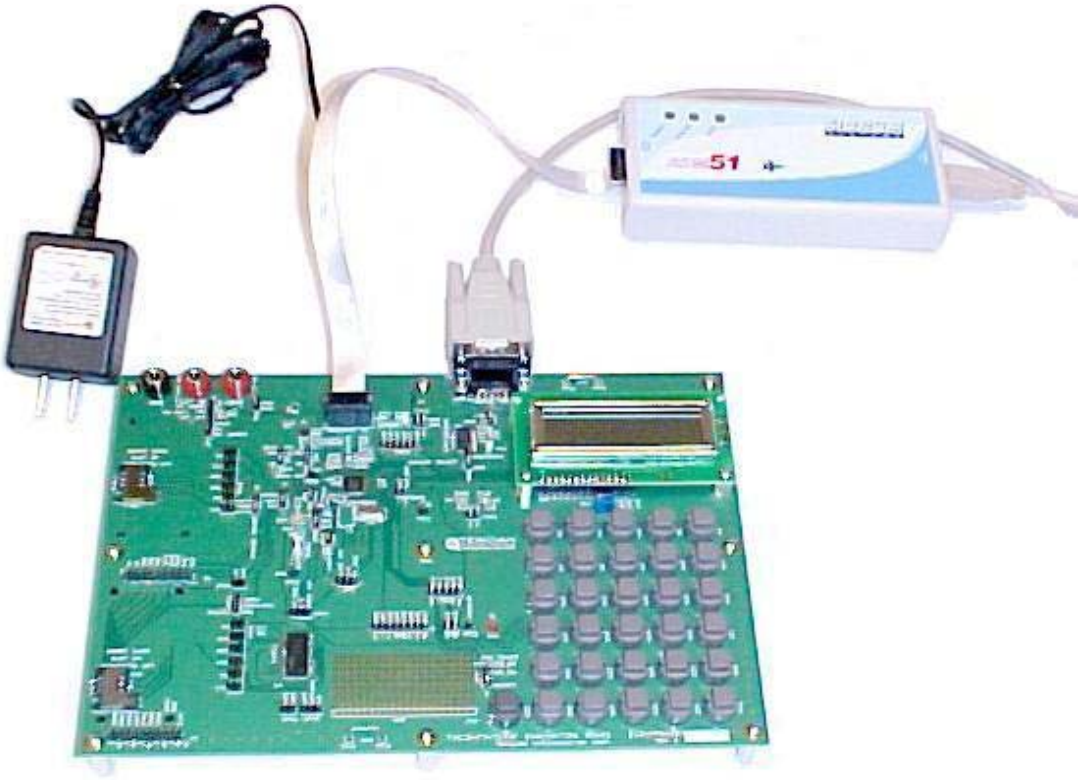


Figure 3: 73S1210F Evaluation Board Basic Connections with ADM-51 ICE

2.2 Loading User Code into the Evaluation Board

Hardware Interface for Programming

The signals listed in Table 1 are necessary for communication between the TFP2 or ICE and the 73S1210F.

Table 1: Flash Programming Interface Signals

Signal	Direction	Function
E_TCLK	Output from 73S1217F	Data clock
E_RXTX	Bi-directional	Data input/output
E_RST[1]	Bi-directional	Flash Downloader Reset (active low)
[1] The E_RST signal should only be driven by the TFP2 when enabling these interface signals. The TFP2 must release E_RST at all other times.		

These signals, along with 3.3 V and GND are available on the emulator header J11. Production modules may be equipped with much simpler programming connectors, e.g. a 5x1 header.

Programming of the flash memory requires either the Signum Systems ADM51 in-circuit emulator or the Flash Download Board Module (FDBM) provided by Teridian.

Loading Code with the In-Circuit Emulator

If firmware exists in the 73S1210F flash memory, the memory must be erased before loading a new file into memory. In order to erase the flash memory, the RESET button in the emulator software must be clicked followed by the ERASE button (see Figure 4).

Once the flash memory is erased, the new file can be loaded using the Load command in the File menu. The dialog box shown in Figure 5 makes it possible to select the file to be loaded by clicking the Browse button. Once the file is selected, pressing the OK button loads the file into the flash memory of the IC.

At this point, the emulator probe (cable) can be removed. Once the 73S1210F device is reset using the reset button on the evaluation board, the new code starts executing.

Loading Code with the TSC Flash Programmer Model TFP2

Follow the instructions given in the *TSC Flash Programmer Model TFP2 User's Manual*.

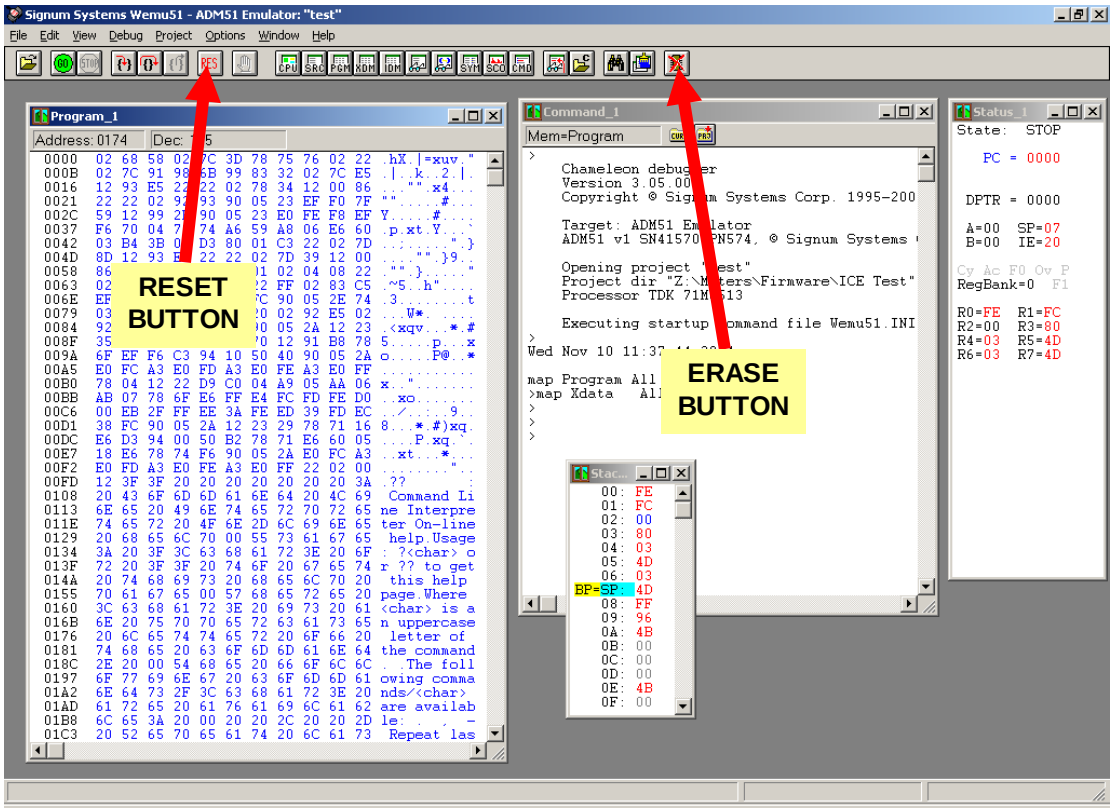


Figure 4: Emulator Window Showing RESET and ERASE Buttons

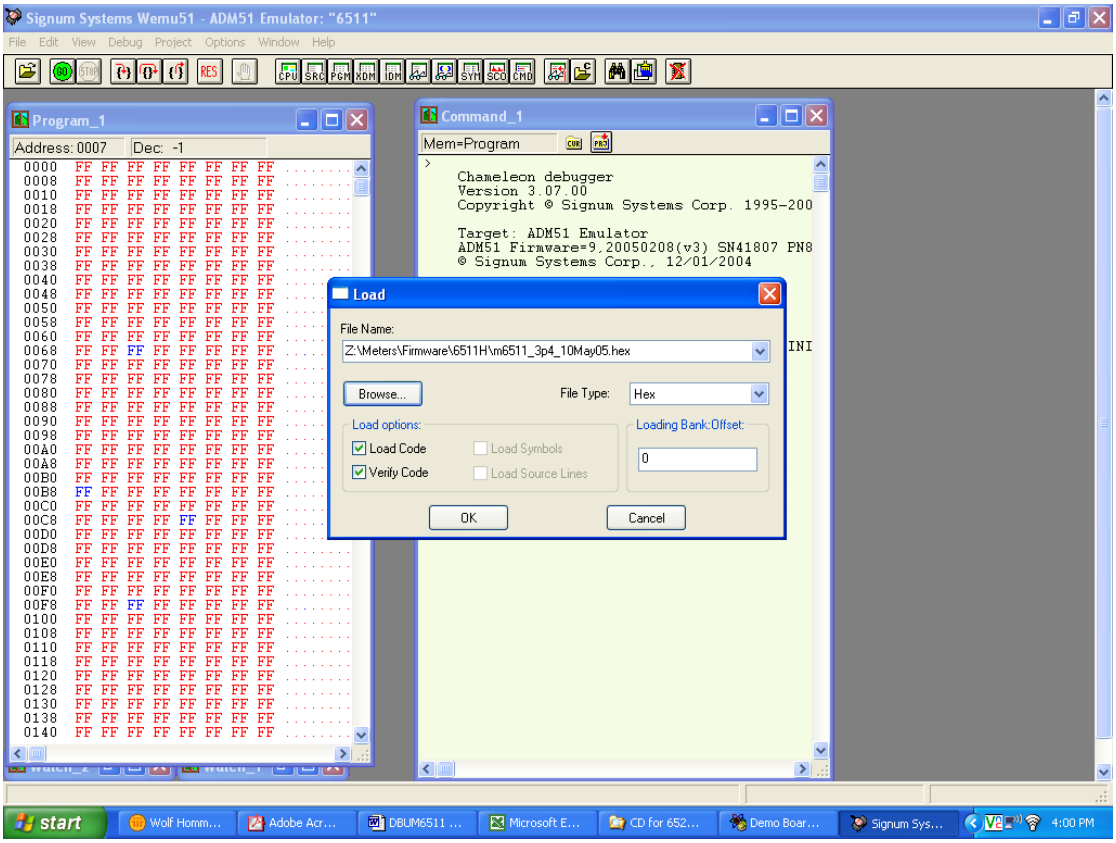


Figure 5: Emulator Window Showing Erased Flash Memory and File Load Menu

3 Using the PCCID Application

The PCCID firmware is pre-installed on the 73S1210F Evaluation Board. It requires a PC with the serial RS-232 port. When powered-up, the board is able to run the PCCID demonstration host application which allows:

- Smart card activation and deactivation, in ISO or EMV mode.
- Smart card APDU commands to be exchanged with the smart card inserted in the board.
- Starting a test sequence in order to test and evaluate the board performance against an EMV test environment.

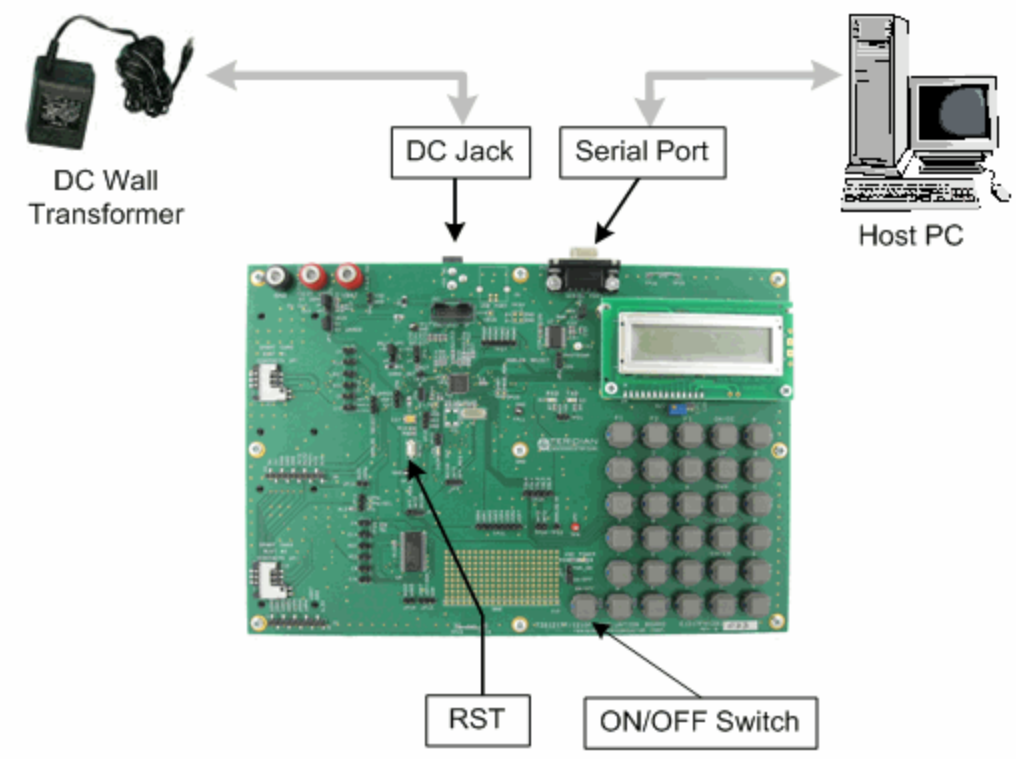
3.1 Host Demonstration Software Installation

Installation on Windows XP

Follow these steps to install the software on a PC running Windows XP:

- Extract "PCCID V***z.zz*** Release.zip" (where ***z.zz*** is the latest version of the firmware release).
  - Create an install directory. For example: "C:\TSC\".
  - Unzip "PCCID V***z.zz*** Release.zip" to the just created folder. All applications and documentation needed to run the board with a Windows PC will be loaded to this folder.
- Plug the supplied adapter into the 5V DC jack and a wall outlet.
- Connect the serial cable between the host system and the 73S1210F Evaluation Board.
- Press the ON/OFF switch to turn the board on.
- Run "TSCP-CCID.exe" (located in the path - ***x***:***yyy***\ PCCID V***z.zz*** Release\Host Applications\Windows App\App\Bin\Release) on the host system to execute the host demonstration application (where ***x*** refers to the drive, ***yyy*** refers to the directory the installation .zip file was expanded to and ***z.zz*** is the latest version of the firmware release).

At this point the application window should appear. For additional information regarding the use of the Teridian Host application, refer to the *Pseudo-CCID Host GUI Users Guide* (UG_12xxF_037).



4 Evaluation Board Hardware Description

4.1 Jumpers, Switches and Modules

Table 2 describes the 73S1210F Evaluation Board jumpers, switches and modules. The Item # in Table 2 references Figure 6.

Table 2: Evaluation Board Jumper, Switch and Module Description

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
1	J2, J3, J5	No Connect	Banana plugs for external regulated power supply	Must be used to connect an external power supply. These inputs are intended to allow control of the input supply voltage of the board. JP5 must be in position "EXT VPC" when using VPC and JP8 must be in position "EXT" when using the VBAT power supply inputs.
				CAUTION The evaluation board is sensitive to the polarity: One red plug is +2.7/6.5 V for external VPC and the other red plug is +4.0/6.5 V for VBAT. The black plug is ground.
2	JP2	+5V	73S8010R VPC select	Selects VPC power supply source for the 73S8010R device between VP on the 73S1210F and +5 V from JP1 pin 2.
3	J11	Not Inserted	In-Circuit Emulator connector	This connector must be used when using an external In-Circuit Emulator (SIGNUM 8052 ADM51 ICE). Refer to the Electrical Schematic for pin assignment.
4	PJ1	Connect	DC jack	Plug to connect an external DC block. Must be used in conjunction with appropriate settings of S1, JP1 and JP6 (see details above). Power supply features are: Voltage: 2.7 V to 6.5 V Current: 400 mA
5	JP6	VDD	RS-232 Xcvr enable jumper	Selects between VDD (always enabled) and a test point (with pull down) to allow the RS232 transceiver chip to be shut down.
6	P1	Connect	DB9 RS232 female socket	This socket allows connection of an RS232 cable to a computer. Use crossed wired (RX/TX) cable. The evaluation board has an on-board level shifter (U7) to allow direct connection to a computer. Connection to an RS232 link is required when using the pre-downloaded PCCID application.
7	JP3	Inserted	RS-232 Xcvr power	Power supply jumper for the RS232 transceiver chip. Can be removed to obtain accurate power measurements.
8	D2, D3		LEDs:	These LEDs (D2, D3) reflect the activity on the

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
			Serial link activity	serial link (RS232 or serial). • D2 reflects the activity on the RX line (Data going TO the 73S1210F) • D3 reflects the activity on the TX line (Data going FROM the 73S1210F)
9	U5		LCD Module	On-board LCD module: • 2 lines of 16 characters, each character dot matrix is 5x7. • Includes an embedded Hitachi HD44780 LCD driver, controlled from the on-board 73S1210F USR interface.
10	RV1		Adjustable resistor to adjust LCD brightness	Can be used to adjust the brightness of the on-board LCD module.
11	S2 to S26, S27 to S32		On-board keypad	5x6 keyboard directly connected to the on-board 73S1210F IC (68-pin only). The assignment of the keys, as silk-printed on the PCB, is the one supported by the TSC Application Programming Interface.
12	–		Board reference and serial number	Should be mentioned in any communication with TSC Application Engineers when requesting support.
13	D8		VDD power indicator	Indicates when the 73S1210F is turned on (VDD = 3.3 V).
14	S33		ON/OFF switch	Switch used to turn on and off the 73S1210F. The switch is overridden when VBUS is applied (VDD is always on). When VDD is on and the switch is pressed, the 73S1210F will activate the OFF_REQ signal and the 73S1210F must set the SCPWRDN or PWRDN bits to shutoff VDD.
15	JP7	ON/OFF	Power ON/OFF select jumper	This jumper will select between the ON/OFF switch and ground. When the switch is selected, the VDD power will toggle between on and off (see item #16). When ground is selected, the VDD will turn on automatically upon application of VPC to the 73S1210F.
16	–		Breadboard area	This breadboard area allows engineers to add their own circuitry / connection of peripherals when prototyping and developing a 73S1210F based application. User I/Os, GPIOs, interrupt pins and power supply pins are located close to this area to allow easy connection.
17	JP9	OFF_REQ	INT3 select	Selects the source for INT3 between the 73S8010R and the OFF_REQ pin on the 73S1210F. Should be set opposite of JP21.
18	JP21	8010R INT	INT2 select	Selects the source for INT2 between the 73S8010R and the OFF_REQ pin on the 73S1210F. Should be set opposite of JP9.

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
19	JP13	Not Inserted	Jumper: USR7/SDA select	This jumper selects which signal is connected to the daughter board connector pin USR7: • In position “USR7”, the 73S1210F USR7 signal is connected to the daughter card pin USR7. • In position “SDA”, the I2C SDA signal is connected to the daughter card pin USR7. This allows the SDA line to connect to an SDA pin on a 73S8010R daughter card.
20	JP14	Not Inserted	Jumper: USR7/SDA select	This jumper allows the on board 73S8010R AUX2 pin to be connected to USR5 if needed. If not needed, the jumper should be removed.
21	U4		On board 73S8010R	The board contains a built-in 73S8010R that is connected to the external smart card interface of the 73S1210F. This device can be disconnected from the 73S1210F if not used, by removing jumpers JP12 and JP21.
22	J7,J8		Optional 73S80xxX Daughter Board interface	When developing applications that require more than 2 smart card interfaces, an optional daughter board can be populated to use the 73S1210F external smart card interface (lines SCIO and SCK), in conjunction with the USR(0:7) port and the INT2 interrupt input of the 73S1210F). Refer to the Electrical Schematic for pin assignment.
23	J9, J10		SIM / SAM and Smart Card connectors – external interface (#2)	Allows the evaluation board to communicate with a smart card using either the standard (credit card size) or SIM/SAM format. This slot is connected to the 73S1210F external card interface # 2. Note that J10 is wired is parallel to the smart card connector J9 (underneath the PCB). Both connectors cannot be populated at the same time.
24	JP11	Not Inserted	Jumper: USR6/SCL select	This jumper selects which signal is connected to the daughter board connector pin USR6: • In position “USR6”, the 73S1210F USR6 signal is connected to the daughter card pin USR6. • In position “SCL”, the I2C SCL signal is connected to the daughter card pin USR6. This allows the SCL line to connect to an SCL pin on a 73S8010R daughter card.
25	JP10	Not Inserted	Jumper: USR6/AUX1 select	This jumper allows the on board 73S8010R AUX1 pin to be connected to USR6 if needed. If not needed the jumper should be removed.
26	S27		Reset button	Evaluation board main reset: Asserts a hardware reset to the on-board 73S1210F IC.

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
27	JP12	Inserted	LED0 jumper	In normal use, a jumper must be inserted in this header to connect the LEDs to the LED pins of the 73S1210F. This jumper can be replaced by a µA / mA-meter to measure the actual current drawn by the LED output of the 73S1210F.
28	JP15	GND	Jumper: security fuse control	This jumper should be removed at all times. Connecting the jumper will allow the security fuses to be blown under firmware control. Refer to the *73S1210F Data Sheet* for further information about the security fuse.
29	JP20	Not Inserted	Analog select	Selects the analog input between TP32 and the VBAT input voltage (via resistor divider).
30	JP8	Not Inserted	VBAT select	Selects the VBAT input between an external supply on J3 or the unregulated 5 V on PJ1.
31	J1, J4		SIM / SAM and Smart Card connectors – internal interface (#1)	Allows the evaluation board to communicate with a smart card using either the standard (credit card size) or SIM/SAM format: This slot is connected to the 73S1210F built-in card interface # 1. J1 is wired in parallel to the smart card connector J4 (underneath the PCB). Both connectors cannot be used at the same time.
32	JP4	Inserted	VDD jumper	The VDD supply jumper can be replaced with an current meter to measure the power consumption on VDD.
33	JP1	5V Unreg	Jumper: 5V power supply selection	This jumper selects the 5.0 V power supply. It selects either the unregulated 5 V supply from PJ1 or the 5.0 V from the USB VBUS: • In position “5V UNREG”, the evaluation board 5.0 V is powered from the PJ1 connector. • In position “VBUS”, the evaluation board is powered from USB VBUS.
34	JP5	5V Unreg	Jumper: VPC power supply selection	This jumper selects the VPC power supply. It selects either the power supply connected to plug J2 or the 5 V unregulated supply on the PJ1 connector. • In position “5V UNREG”, the evaluation board VPC is connected to 5 V coming in on PJ1. • In position “EXT VPC”, the evaluation board VPC is powered from the voltage applied on the plug J2.

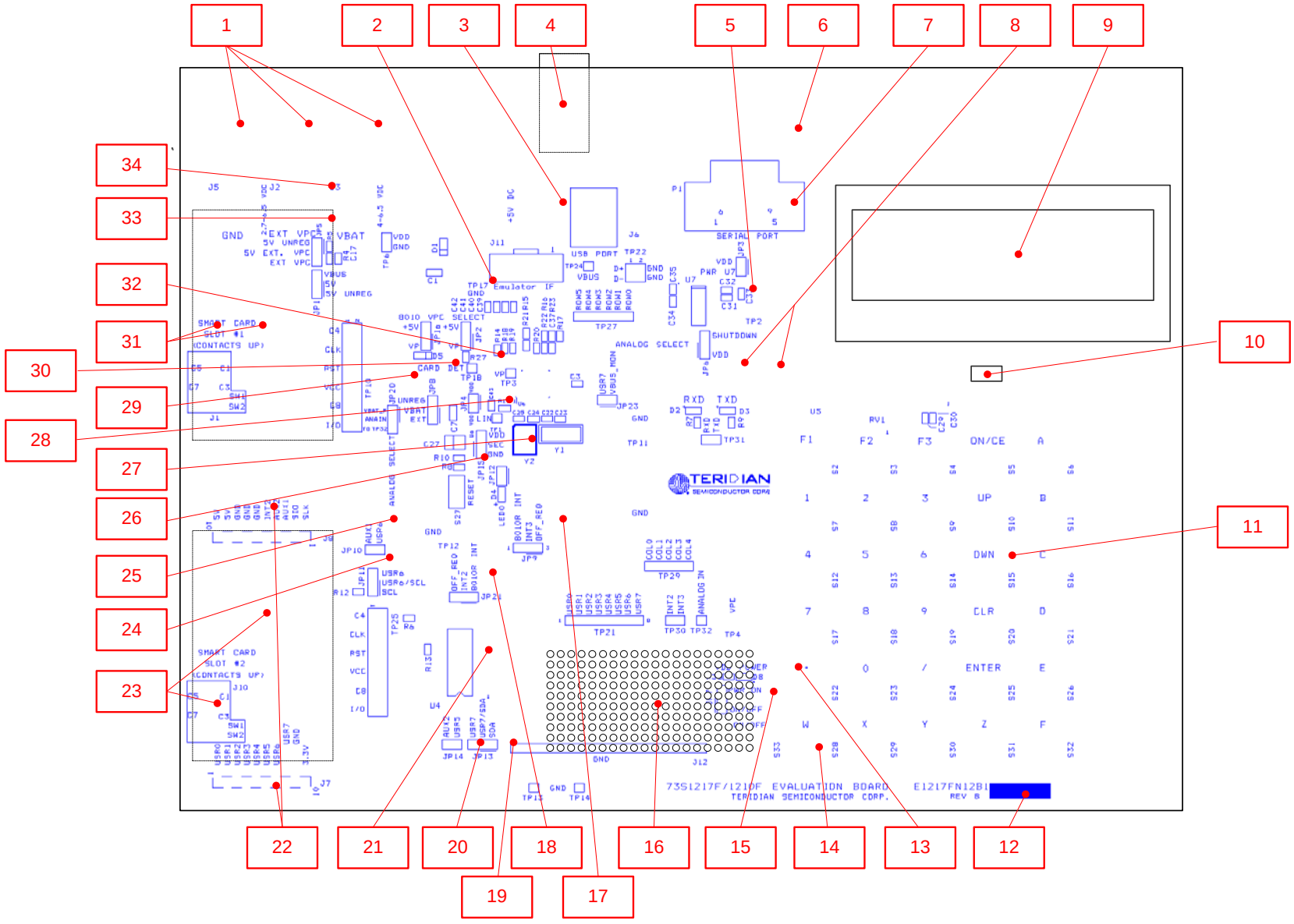


Figure 6: 73S1210F Evaluation Board Jumper, Switch and Module Locations

4.2 Test Points

The test point numbers listed in Table 3 refer to the test point numbers shown in the electrical schematic and in the silkscreen of the PCB.

Table 3: Evaluation Board Test Point Description

Test Point #	Name	Use
TP1	LIN	Test point to monitor Inductor operation.
TP2	Shutdown	Test point to control the enable input on the RX-232 transceiver chip.
TP4	VPC	Single-pin test point. VPC signal directly connected to the 73S1210F and its decoupling capacitors. Can be used to measure integrity of the power supply of the DC-DC converters of the 73S1210F.
TP6	VDD	2-pin test point, with one ground and one VDD signal directly connected to the 73S1210F and its decoupling capacitors. Can be used to measure the integrity of the digital power supply of the 73S1210F, or to add a decoupling capacitor.
TP10	Smart Card Contacts – Interface #1	Header for measurement of the card signals, close to the card connectors. Contains the card signals VCC1, RST1, CLK1, C81 and C41. Each contact has its own ground pin on the header.
TP11 to TP17	GND	Ground test points. Can be used for grounding of lab equipment probes.
TP18	Card Detect – Interface #1	Card detect signal coming directly from the card connectors.
TP21	USR(7:0)	Standard 9/8-bit user I/O port of the 73S1210F.  Some of the user I/Os are shared by the extension 73S80xx daughter board when using an external smart card interface, and the LCD interface. Only one should be used at a time.
TP22	USB – N/A	USB is not available and TP22 is not populated with the 73S1210F.
TP24	VBUS – N/A	USB is not available and TP24 is not populated with the 73S1210F.
TP25	Smart Card Contacts – Interface #2	Header for measurement of the card signals, close to the card connectors. Contains the card signals VCC2, RST2, CLK2, C42 and C82. Each contact has its own ground pin on the header.
TP27	ROW[0:5]	The row pins used for the keypad interface.
TP29	COL[0:4]	The column pins used for the keypad interface.
TP30	INT2 INT3	Interrupt input #2 and #3 of the 73S1210F. This header is close to the breadboard area for easy wiring.
TP31	RX, TX	The TX and RX serial UART I/O signals (3.3 V digital logic level).

4.3 Schematic

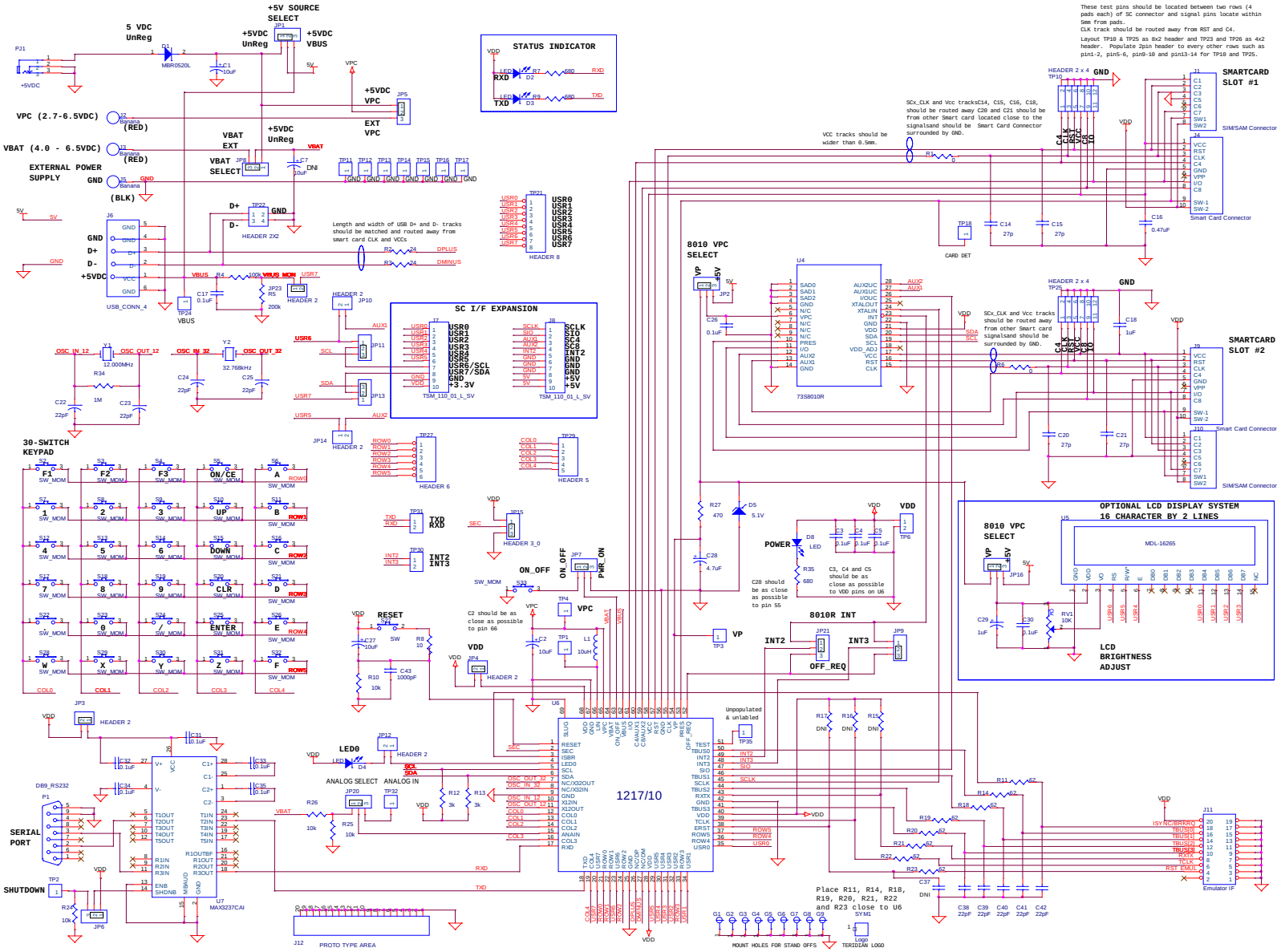


Figure 7: 73S1210F Evaluation Board Electrical Schematic

4.4 PCB Layouts

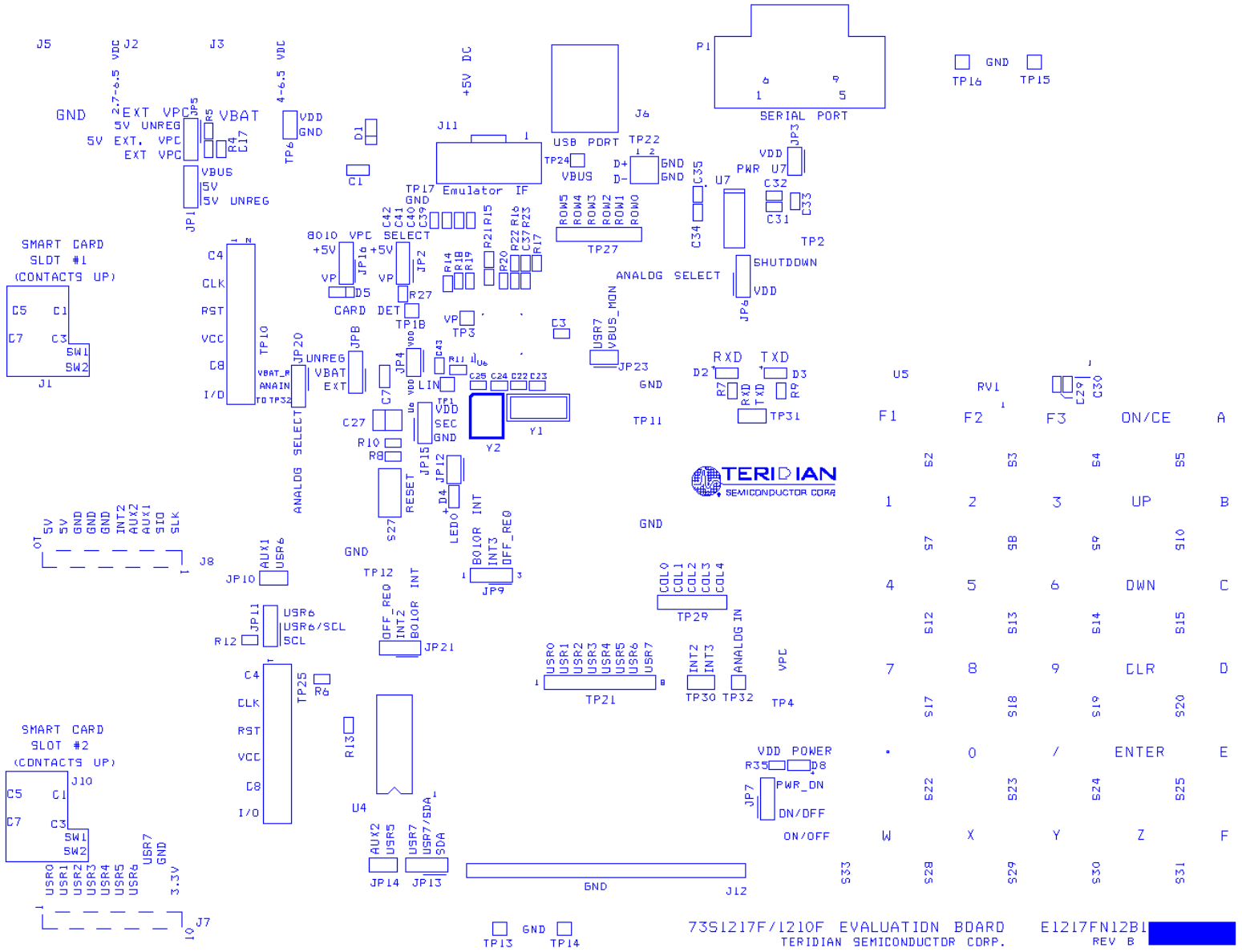


Figure 8: 73S1210F Evaluation Board Top View (Silkscreen)

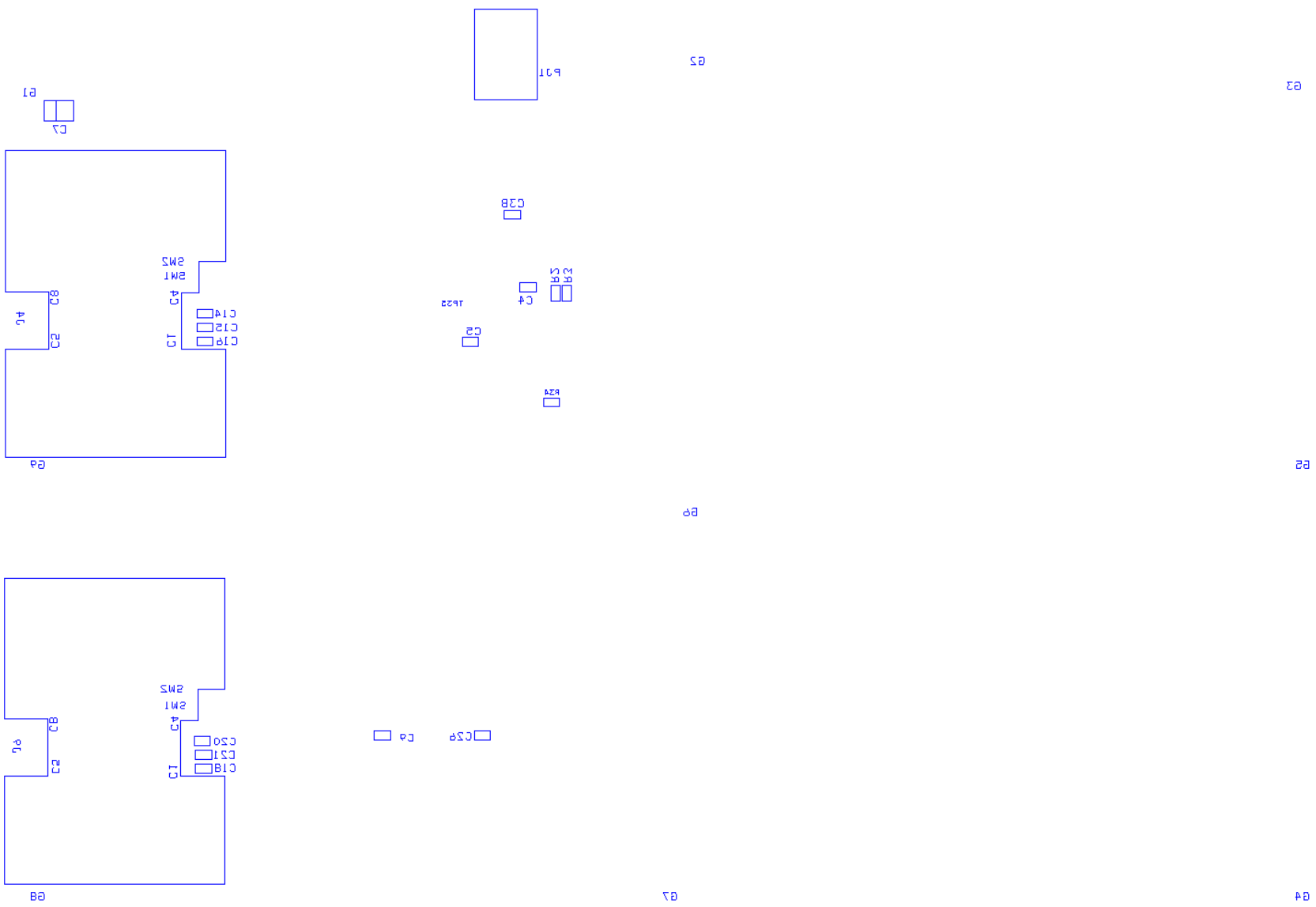


Figure 9: 73S1210F Evaluation Board Bottom View (Silkscreen)

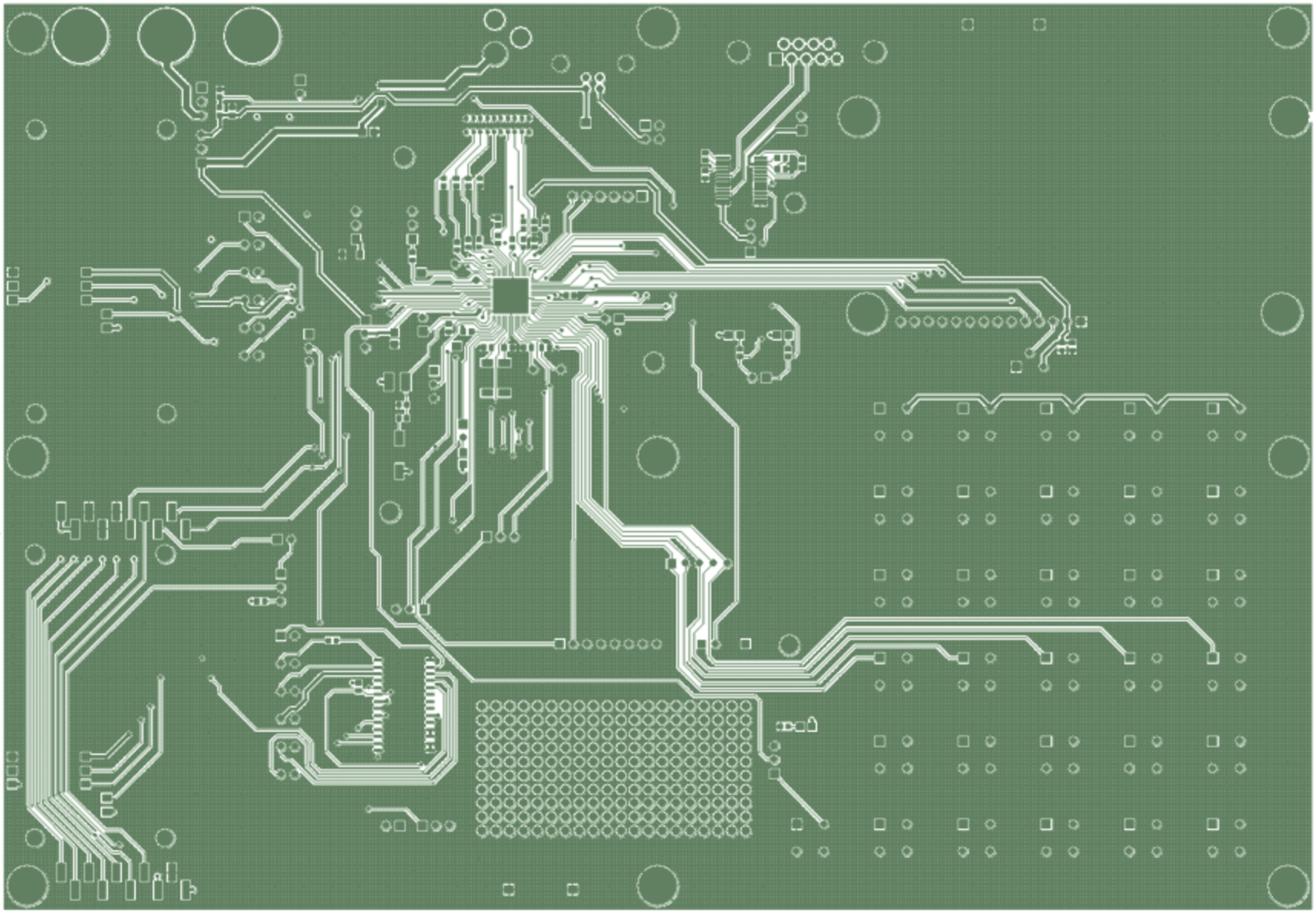


Figure 10: 73S1210F Evaluation Board Top Signal Layer

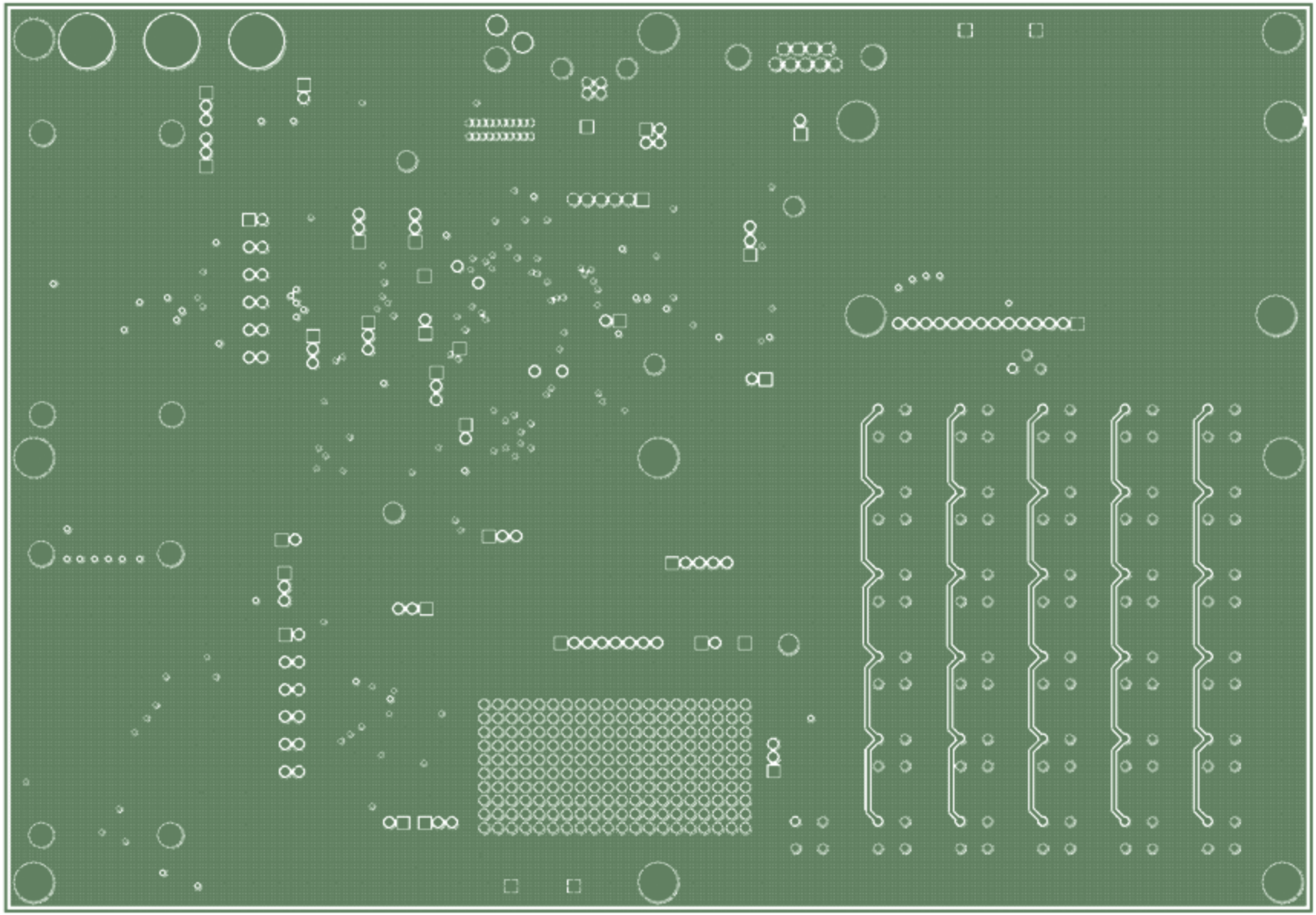


Figure 11: 73S1210F Evaluation Board Middle Layer 1 – Ground Plane

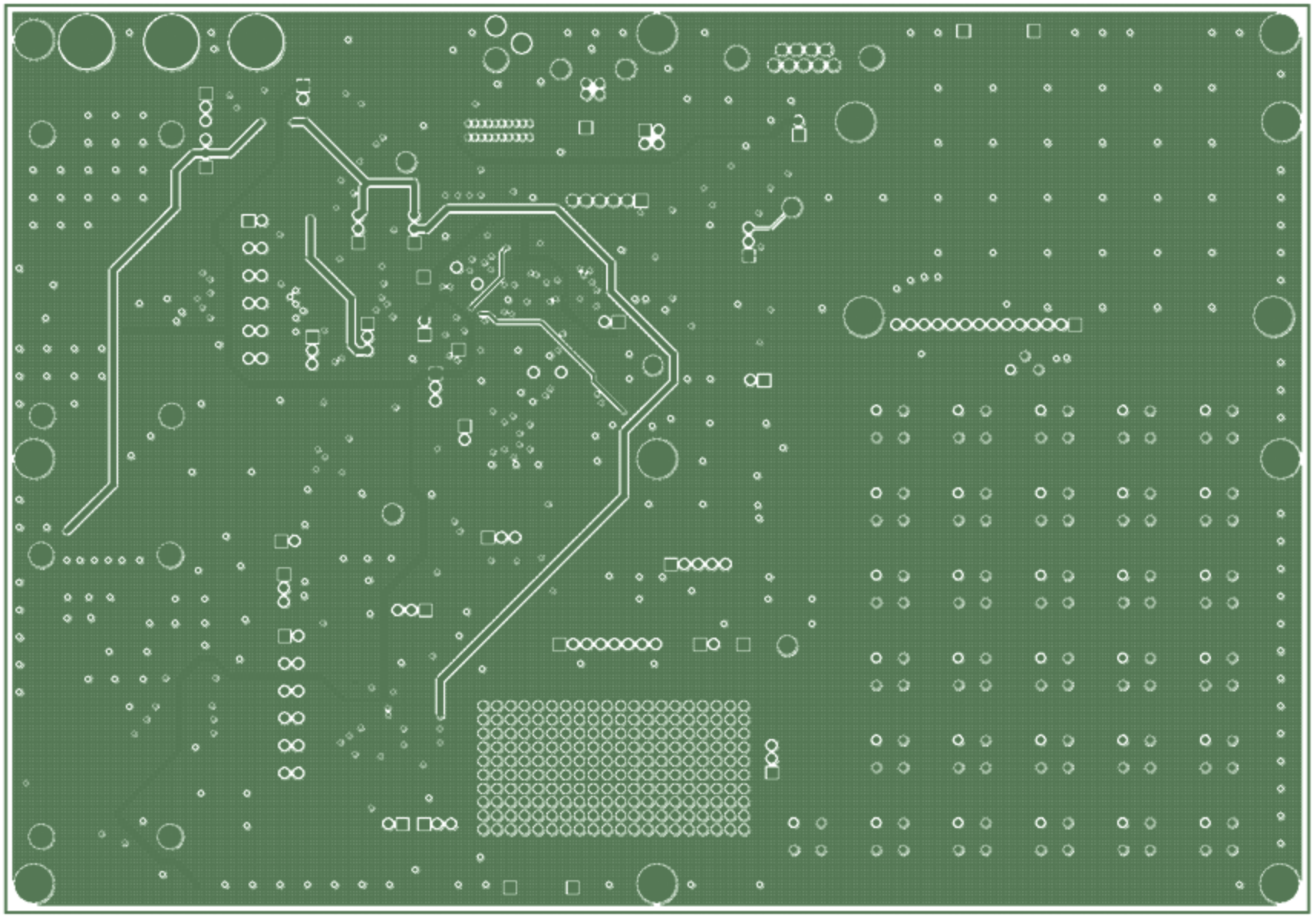


Figure 12: 73S1210F Evaluation Board Middle Layer 2 – Supply Plane

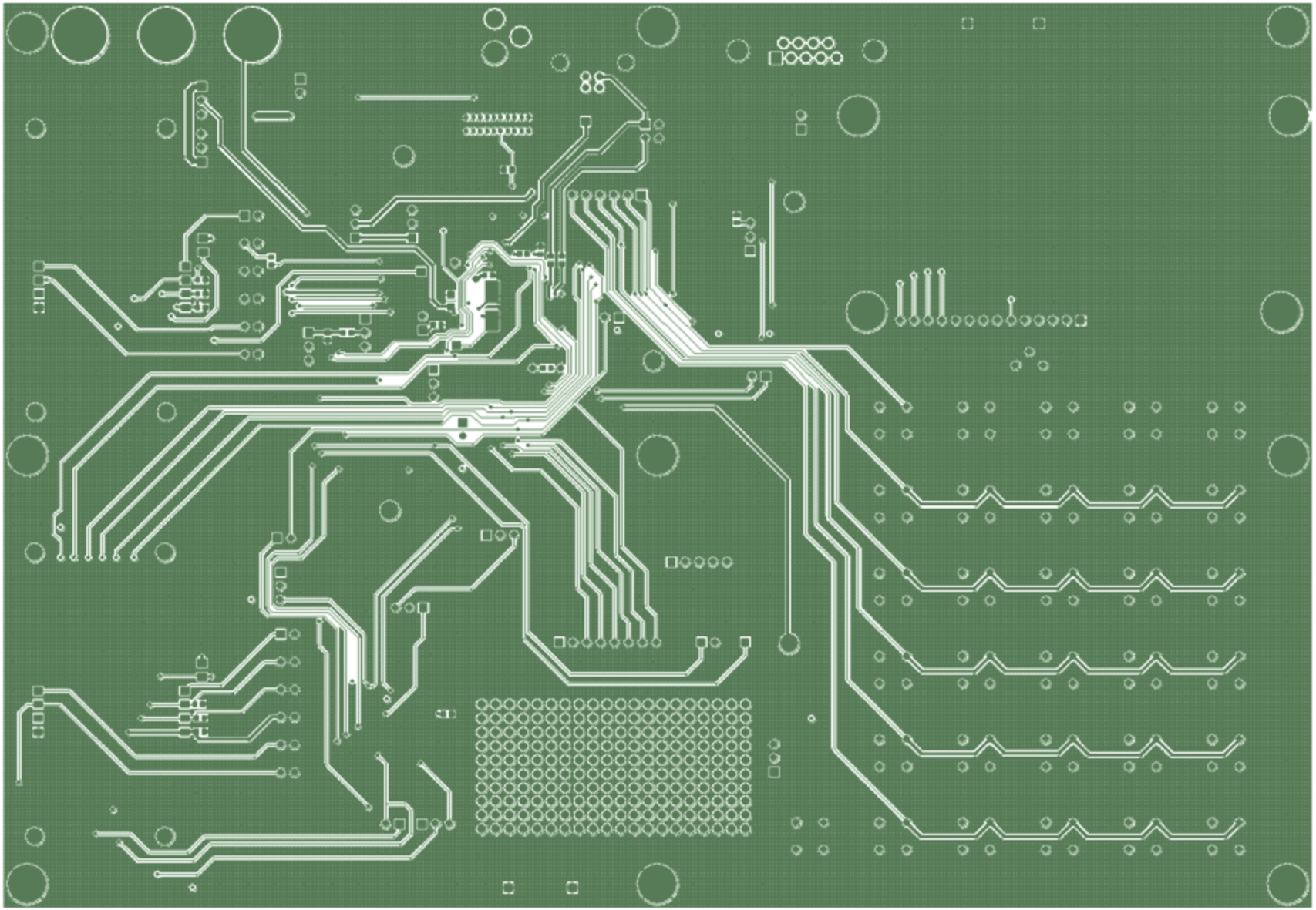


Figure 13: 73S1210F Evaluation Board Bottom Signal Layer

4.5 Bill of Materials

Table 4 provides the bill of materials for the 73S1210F Evaluation Board schematic provided in Figure 7.

Table 4: 73S1210F Evaluation Board Bill of Materials

Item	Qty.	Reference	Part	PCB Footprint	Digi-key Part Number	Part Number	Manufacturer
1	1	C27	10 µF	3528-21 (EIA)	478-1672-1-ND	TAJB106K010R	AVX Corporation
2	2	C1,C2	10 µF	0805	PCC2225CT-ND	ECJ-2FB0J106M	Panasonic
3	10	C3,C4,C5,C26,C30,C31, C32,C33, C34,C35	0.1 µF	603	445-1314-1-ND	C1608X7R1H104K	TDK Corporation
4	1	C28	4.7 µF	0603	PCC2396CT-ND	ECJ-1VB0J475K	Panasonic
5	1	C16	0.47 µF	0603	PCC2275CT-ND	ECJ-1VB1A474K	Panasonic
6	4	C14,C15,C20,C21	27 pF	603	PCC270ACVCT-ND	ECJ-1VC1H270J	Panasonic
7	2	C18,C29	1 µF	603	PCC2174CT-ND	C1608X5R1A105K	TDK Corporation
8	7	C22,C23, C38-C42	22 pF	603	PCC220ACVCT-ND	ECJ-1VC1H220J	Panasonic
9	1	C43	1000 pF	603	PCC2151CT-ND	ECJ-1VC1H102J	Panasonic
10	1	D1	MBR0520L	SOD-123	MBR0520LCT-ND	MBR0520L	Fairchild
11	1	D5	MMSZ4689T1G	SOD-123	MMSZ4689T1GOSCT-ND	MMSZ4689T1G -7	ON Semiconductor
12	4	D2,D3,D4,D8	LED	805	160-1414-1-ND	LTST-C170FKT	LITE-ON INC
13	13	JP1,JP2,JP5,JP6,JP7, JP8,JP9,JP11,JP13, JP15,JP16, JP20, JP21	HEADER 3	1 x 3 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
14	5	JP3,JP4,JP10,JP12,JP14	HEADER 2	1 x 2 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
15	2	J1,J10	SIM/SAM Connector	ITT_CCM03-3013	401-1691-1-ND	CCM03-3754	ITT Industries
16	2	J2,J3	Banana (red)	Banana		16BJ381	Mouser
17	1	J5	Banana (black)	Banana		16BJ382	Mouser
18	2	J4,J9	Smart Card Connector	CCM02-2504	401-1715-ND	CCM02-2504LFT	ITT Industries
19	2	J8,J7	TSM_110_01_L_SV	TSM_110_01_L_SV		TSM_110_01_L_SV	Samtec
20	1	J11	Emulator IF	10 X 2 pin	A3210-ND	104068-1	AMP/Tyco Electronics
21	1	L1	10 µH	1210	490-4059-1-ND	LQH32CN100K53L	Murata
22	1	PJ1	+5 VDC	RAPC712	SC1152-ND	RAPC712	Switchcraft
23	1	P1	DB9_RS232	AMP_745781	A2100-ND	745781-4	AMP/Tyco Electronics

Item	Qty.	Reference	Part	PCB Footprint	Digi-key Part Number	Part Number	Manufacturer
24	1	RV1	10 KΩ	3266W	3266W-103-ND	3266W-1-103	Bourns
25	2	R1,R6	0	603	P0.0GCT-ND	ERJ-3GEY0R00V	Panasonic
26	3	R7,R9,R35	680 Ω	603	P680GCT-ND	ERJ-3GEYJ681V	Panasonic
27	1	R8	10 Ω	603	P10GCT-ND	ERJ-3GEYJ100V	Panasonic
28	4	R10, R24, R25, R26	10 kΩ	603	P10KGCT-ND	ERJ-3GEYJ103V	Panasonic
29	8	R11,R14,R18,R19,R20, R21, R22,R23	62 Ω	603	P62GCT-ND	ERJ-3GEYJ620V	Panasonic
30	2	R12,R13	3 kΩ	603	P3.0KGCT-ND	ERJ-3GEYJ302V	Panasonic
31	1	R27	470 Ω	603	P470GCT-ND	ERJ-3GEYJ471V	Panasonic
32	1	R34	1 MΩ	603	P1.0MGCT-ND	ERJ-3GEYJ106V	Panasonic
33	31	S2-S26, S28-S33	SW_MOM	Pushbutton SW	401-1885-ND	D6 C 10LFS	ITT Industries
34	1	S27	SW	Panasonic EVQ	P8051SCT	EVQ-PJX05M	Panasonic
35	2	TP18,TP32	TP	1 pin	S1011-36-ND	PZC36SAAN	Sullins Electronics
36	2	TP2, TP18	TP	1 Pin White	5012K-ND	5012	Keystone Electronics
37	1	TP4	TP	1 pin Red	5010K-ND	5010	Keystone Electronics
38	3	TP11,TP12,TP17	TP	1 pin Black	5011K-ND	5011	Keystone Electronics
39	3	TP6,TP30,TP31	TP2	1 x 2 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
40	2	TP10,TP25	HEADER 2 x 6	6 x 2 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
41	1	TP21	HEADER 8	1 x 8 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
42	1	TP27	HEADER 6	6 x 1 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
43	1	TP29	HEADER 5	5 x 1 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
44	1	U4	73S8010R		73S8010R		Teridian Semiconductor
45	1	U5	MDL-16265		153-1078-ND	MDL-16265-SS-LV	Varitronix
46	1	U6	73S1210F	68 QFN		73S1210F	Teridian Semiconductor
47	1	U7	MAX3237CAI		MAX3237CAI-ND	MAX3237CAI	Maxim
48	1	Y1	12.000 MHz		X1116-ND	ECS-120-20-4XDN	ECS

4.6 Schematic Information

This section provides recommendations on proper schematic design that will help in designing circuits that are functional and compatible with the PCCID software library APIs.

4.6.1 Reset Circuit

The 73S1210F Evaluation Board provides a reset pushbutton that can be used when prototyping and debugging software. The RESET pin should be supported by the external components shown in Figure 14. R8 should be around 10 Ω. The capacitor C27 should be 10 µF. R8 and C27 should be mounted as close as possible to the IC.

C43 (1000 pF) is shown for EFT protection and is optional.

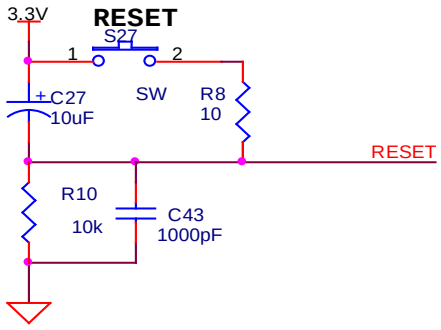


Figure 14: External Components for RESET

4.6.2 Oscillator

The 73S1210F contains a single oscillator for the primary system clock. The system clock should use a 12 MHz crystal to provide the proper system clock rates for the serial and smart card interfaces. The system oscillator requires a 1 MΩ parallel resistor to insure proper oscillator startup (Figure 15).

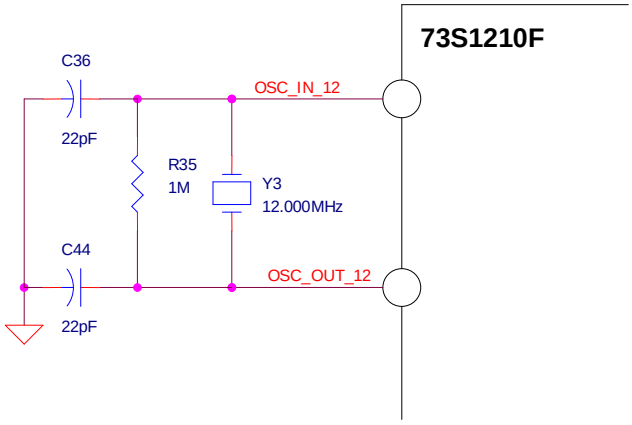


Figure 15: Oscillator Circuit

4.6.3 LCD

The 73S1210F does not contain an on-chip LCD controller. However, an LCD module (with built-in controller) can be used with the 73S1210F via use of specific USR (GPIO) pins. The LCD API libraries support up to a 2 line/16 character display. Figure 16 shows the basic connection for this type of LCD. The LCD module must connect to the USR pins as shown and it requires an external brightness adjust circuit.

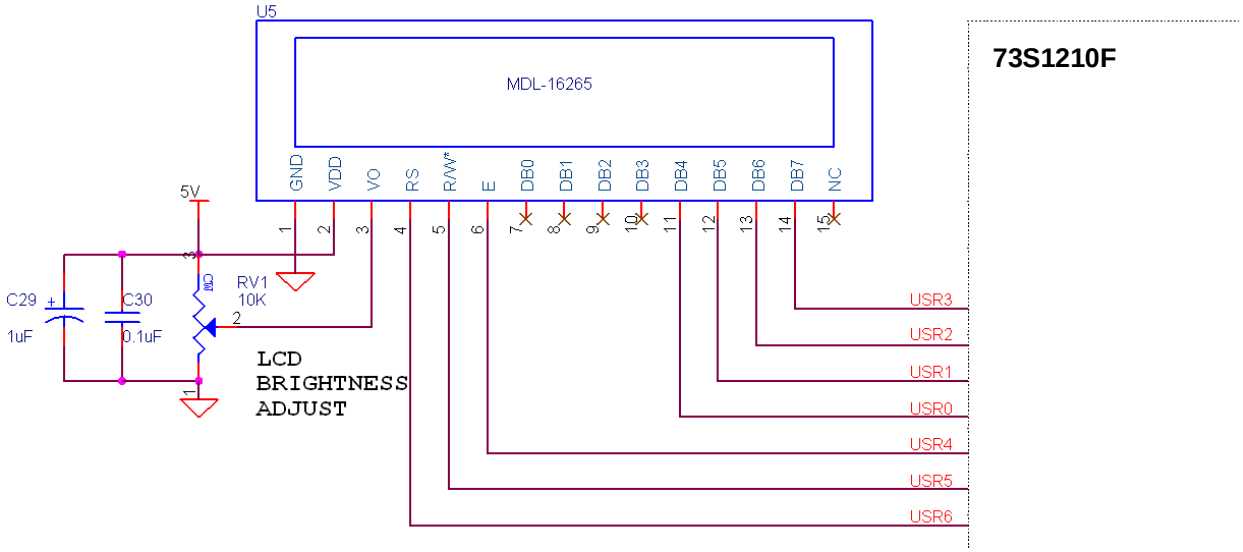


Figure 16: LCD Connections

4.6.4 Smart Card Interface

The smart card interface on the 73S1210F requires few external components for proper operation. Figure 17 shows the recommended smart card interface connections.

- The RST and CLK signals should have 27 pF capacitors at the smart card connector.
- It is recommended that a 0 Ω resistor be added in series with the CLK signal. If necessary, in noisy environments, this resistor can be replaced with a small resistor to create a RC filter on the CLK signal to reduce CLK noise. This filter is used to soften the clock edges and provide a cleaner clock for those environments where this could be problematic.
- The VCC output must have a 1.0 μF capacitor at the smart card connector for proper operation.
- The VPC input is the power supply input for the smart card power. It is recommended that both a 10 μF and a 0.1 μF capacitor are connected to provide proper decoupling for this input.
- The PRES input on the 73S1210F contains a very weak pull down resistor. As a result, an additional external pull down resistor is recommended to prevent any system noise from triggering a false card event. The same holds true for the $\overline{\text{PRES}}$ input, except a pull up resistor is utilized as the logic is inverted from the PRES input.

The smart card interface layout is important. The following guidelines should be followed to provide the optimum smart card interface operation:

- Route auxiliary signals away from card interface signals
- Keep CLK signal as short as possible and with few bends in the trace. Keep route of the CLK trace to one layer (avoid vias to other plane). Keep CLK trace away from other traces especially RST and VCC. Filtering of the CLK trace is allowed for noise purpose. Up to 30 pF to ground is allowed at the CLK pin of the smart card connector. Also, the zero Ω series resistor, R7, can be replaced for additional filtering (no more than 100 Ω).
- Keep VCC trace as short as possible. Make trace a minimum of 0.5 mm thick. Also, keep VCC away from other traces especially RST and CLK.
- Keep CLK trace away from VCC and RST traces. Up to 30 pF to ground is allowed for filtering
- Keep 0.1 μF close to VDD pin of the device and directly take other end to ground
- Keep 10 μF and 0.1 μF capacitors close to VPC pin of the device and directly take other end to ground
- Keep 1.0 μF close to VCC pin of the smart card connector and directly take other end to ground

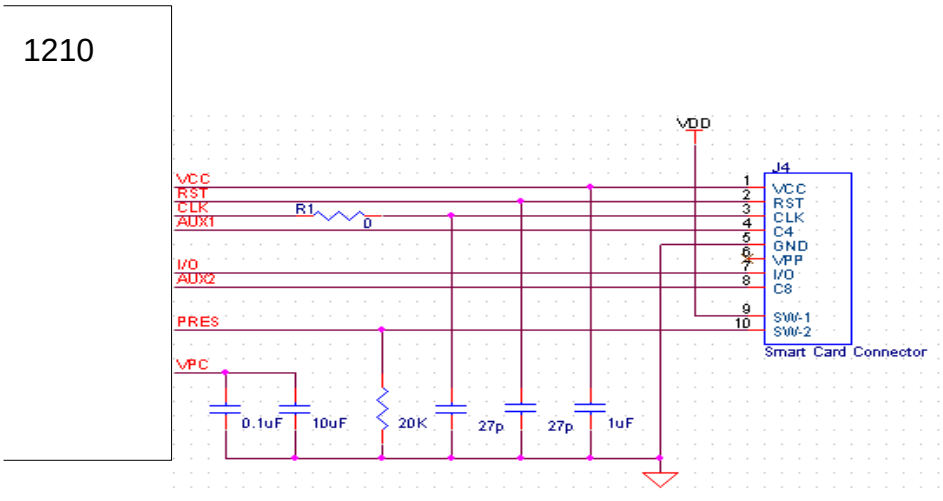


Figure 17: Smart Card Connections

5 Ordering Information

Part Description	Order Number
73S1210F 68-Pin QFN Evaluation Board	73S1210F-EB

6 Related Documentation

The following 73S1210F documents are available from Teridian Semiconductor Corporation:

73S1210F Data Sheet
73S1210F Evaluation Board Quick Start Guide
TSC Flash Programmer Model TFP2 User's Manual

7 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S1210F contact us at:

6440 Oak Canyon Road
Suite 100
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: scr.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	January 3, 2007	Document Creation.
1.1	February 12, 2007	Changed 5.1 V zener diode part number and value of limiting resistor R27.
1.2	August 18, 2009	Updated BOM parts to remove bad or obsolete part numbers. Removed Zener and current limiting resistor. Removed LAPIE references. Miscellaneous editorial modifications.