TERIDIAN SEMICONDUCTOR CORP.

Simplifying System Integration™

73S1209F
Evaluation Board User Guide

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Teridian Semiconductor Corp., 6440 Oak Canyon, Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.teridian.com

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1 Introduction

The Teridian Semiconductor Corporation (TSC) 73S1209F Evaluation Board is used to demonstrate the capabilities of the 73S1209F Smart Card Controller device. It has been designed to operate either as a standalone or as a development platform.

The 73S1209F Evaluation Board can be programmed to run any of the Teridian turnkey applications or a user-developed custom application. Teridian provides its USB CCID application preloaded on the board and an EMV testing application on the CD.

Applications can be downloaded through the In-Circuit-Emulator (ICE) or through the TSC Flash Programmer Model TFP2. As a development tool, the evaluation board can operate in conjunction with an ICE to develop and debug 73S1209F based embedded applications.



The 73S1209F Evaluation Board uses the same PWB as the 73S1215F. The 73S1215F has some features that the 73S1209F does not contain. These include the 32 kHz oscillator, USB interface, LED2 and LED3. These features are depopulated on the 73S1209F.

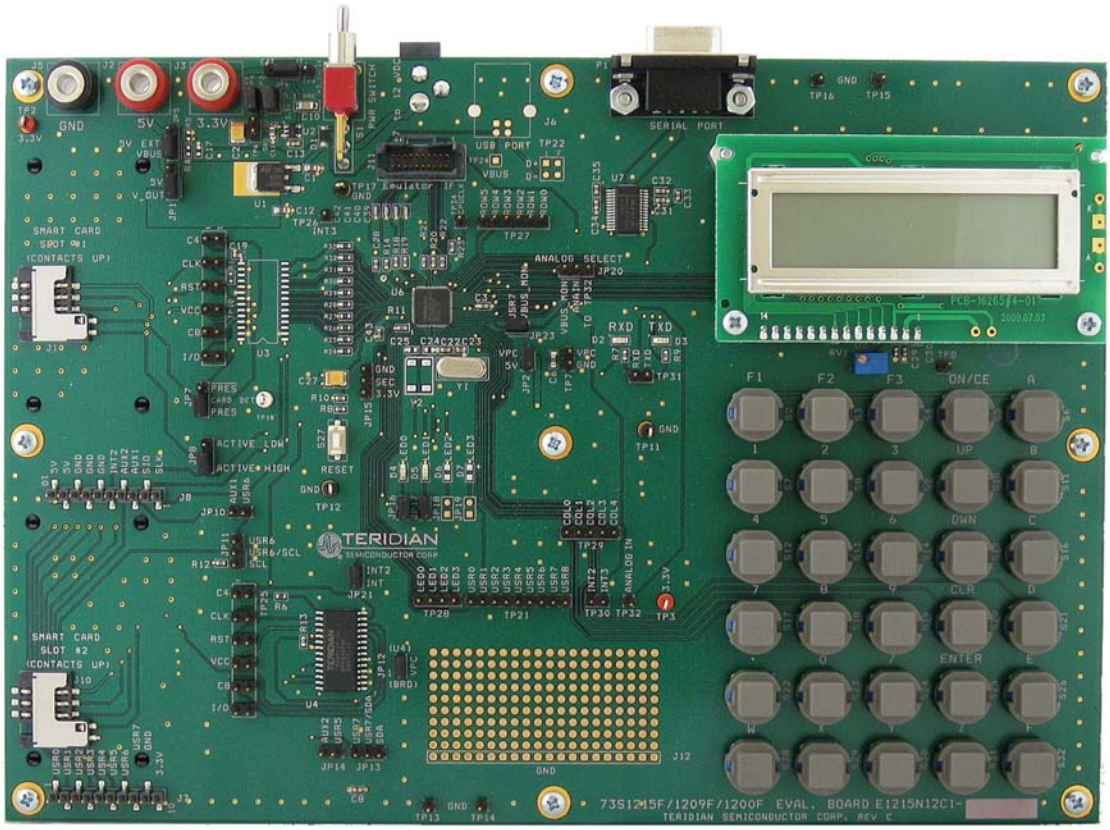


Figure 1: 73S1209F Evaluation Board

1.1 Evaluation Kit Contents

The 73S1209F Evaluation Kit contains the following:

- 73S1209F Evaluation Board: 4-layer, rectangular PWB as shown in Figure 1 (identification number E1215N12C1 Rev C), containing the 73S1209F with the preloaded turnkey program PCCID.
- 12 VDC/1,000 mA universal wall transformer with 2.1 mm plug ID (CUI Inc. – EPAS-101W-12).
- Serial cable: DB9, male/female, 2 meter length (Digi-Key AE1379-ND).
- CD containing documentation (data sheet, and user guides), Software API libraries, evaluation code, and utilities.

1.2 Evaluation Board Features

The 73S1209F Evaluation Board (see Figure 1) includes the following:

- RS-232 interface
- Dual smart card interface
- ICE/Programmer interface
- 2 line x 16 character LCD module
- 6 x 5 Keypad
- 2 LEDs

1.3 Recommended Equipment and Test Tools

The following equipment and tools (not provided) are recommended for use with the 73S1209F Evaluation Kit:

- For functional evaluation: PC with Microsoft® Windows® XP or Vista®.
- For software development (MPU code)
  - Signum™ ICE (In Circuit Emulator): ADM-51. Refer to http://signum.temp.veriohosting.com/Signum.htm.
  - Keil™ 8051 C Compiler Kit: CA51. Refer to http://www.keil.com/c51/ca51kit.htm and http://www.keil.com/product/sales.htm

2 Evaluation Board Setup

Figure 2 shows the basic connections of the evaluation board with the external equipment.

The power supply can come from two sources:

- A regulated lab power supply connected to the banana plugs J2, J3 and J5. In this case, the board main switch S1 has no effect.
- Any AC-DC converter block (default), able to generate a DC power supply of 7 V min / 12 V max / 400 mA. In this case, the board main switch S1 connects or disconnects the supply to the board.

The communication with an external host is accommodated via a standard RS-232 serial interface (TX/RX only).

The board is loaded by default with the PCCID application. It requires a PC to be connected through its serial port. When powered-up, the board is able to run with the PC Exerciser host application. Refer to the *73S1209F Evaluation Board Quick Start Guide* to setup and run the PCCID application.

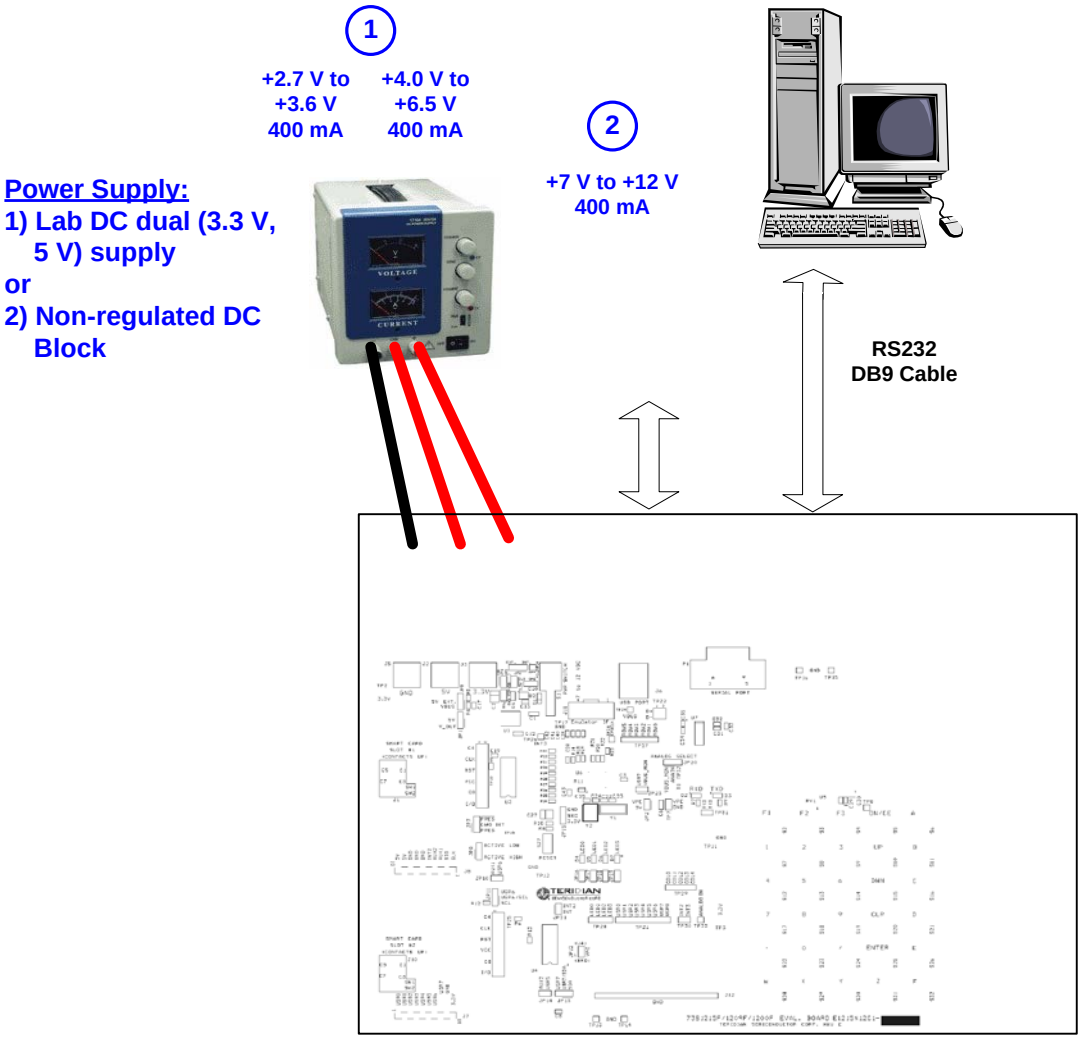


Figure 2: 73S1209F Evaluation Board Basic Connections

2.1 Connecting the Evaluation Board with an Emulation Tool

The 73S1209F Evaluation Board has been designed to operate with an In-Circuit-Emulator (ICE) from Signum Systems (model ADM-51). Figure 3 shows the connections between the ICE and the evaluation board. The Signum System POD has a ribbon cable that must be directly attached to connector J11.

Signum Systems offers different POD options depending on user needs. The standard pod allows users to perform typical emulator functions such as symbolic debugging, in-line breakpoints, memory examination/modification, etc. Other pod options enable code trace capability and/or complex breakpoints at an additional cost.

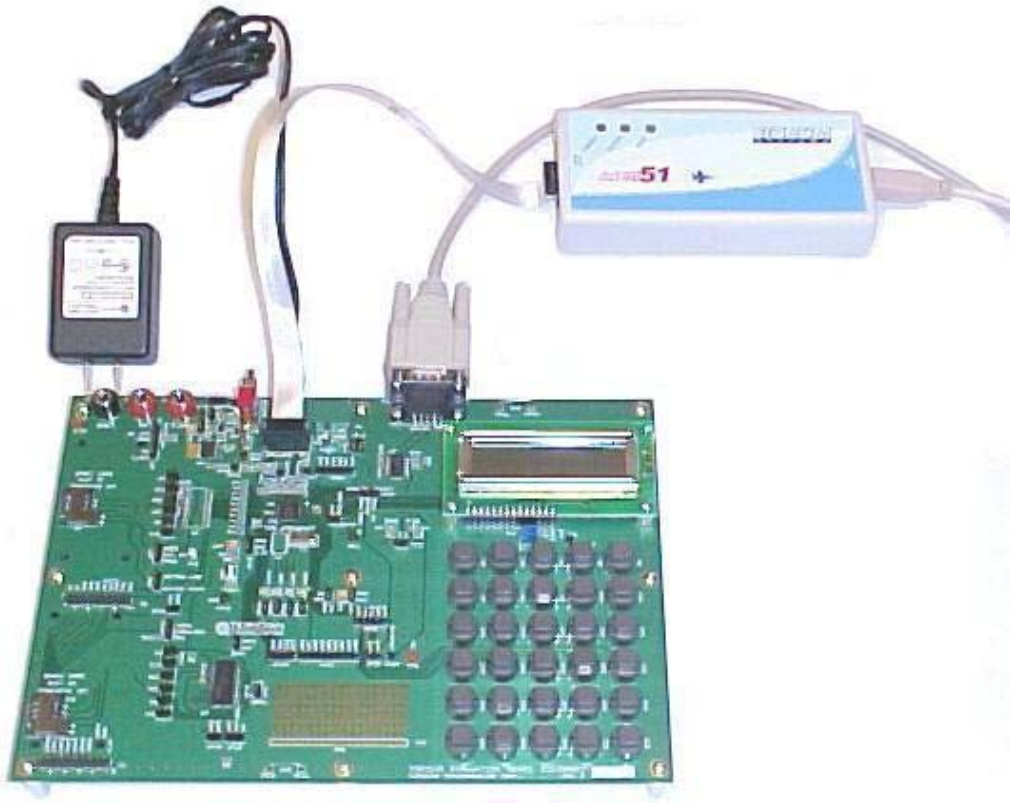


Figure 3: 73S1209F Evaluation Board Basic Connections with ADM-51 ICE

2.2 Loading User Code into the Evaluation Board

Hardware Interface for Programming

The signals listed in Table 1 are necessary for communication between the TFP2 or ICE and the 73S1209F.

Table 1: Flash Programming Interface Signals

Signal	Direction	Function
E_TCLK	Output from 73S1209F	Data clock
E_RXTX	Bi-directional	Data input/output
E_RST[1]	Bi-directional	Flash Downloader Reset (active low)
[1] The E_RST signal should only be driven by the TFP2 when enabling these interface signals. The TFP2 must release E_RST at all other times.		

These signals, along with 3.3 V and GND are available on the emulator header J11. Production modules may be equipped with much simpler programming connectors, e.g. a 5x1 header.

Programming of the flash memory requires either the Signum Systems ADM51 in-circuit emulator or the TSC Flash Programmer Model TFP2 provided by Teridian.

Loading Code with the In-Circuit Emulator

If firmware exists in the 73S1209F flash memory, the memory must be erased before loading a new file into memory. In order to erase the flash memory, the RESET button in the emulator software must be clicked followed by the ERASE button (see Figure 4).

Once the flash memory is erased, the new file can be loaded using the Load command in the File menu. The dialog box shown in Figure 5 makes it possible to select the file to be loaded by clicking the Browse button. Once the file is selected, pressing the OK button loads the file into the flash memory of the IC.

At this point, the emulator probe (cable) can be removed. Once the 73S1209F device is reset using the reset button on the evaluation board, the new code starts executing.

Loading Code with the TSC Flash Programmer Model TFP2

Follow the instructions given in the *TSC Flash Programmer Model TFP2 User's Manual*.

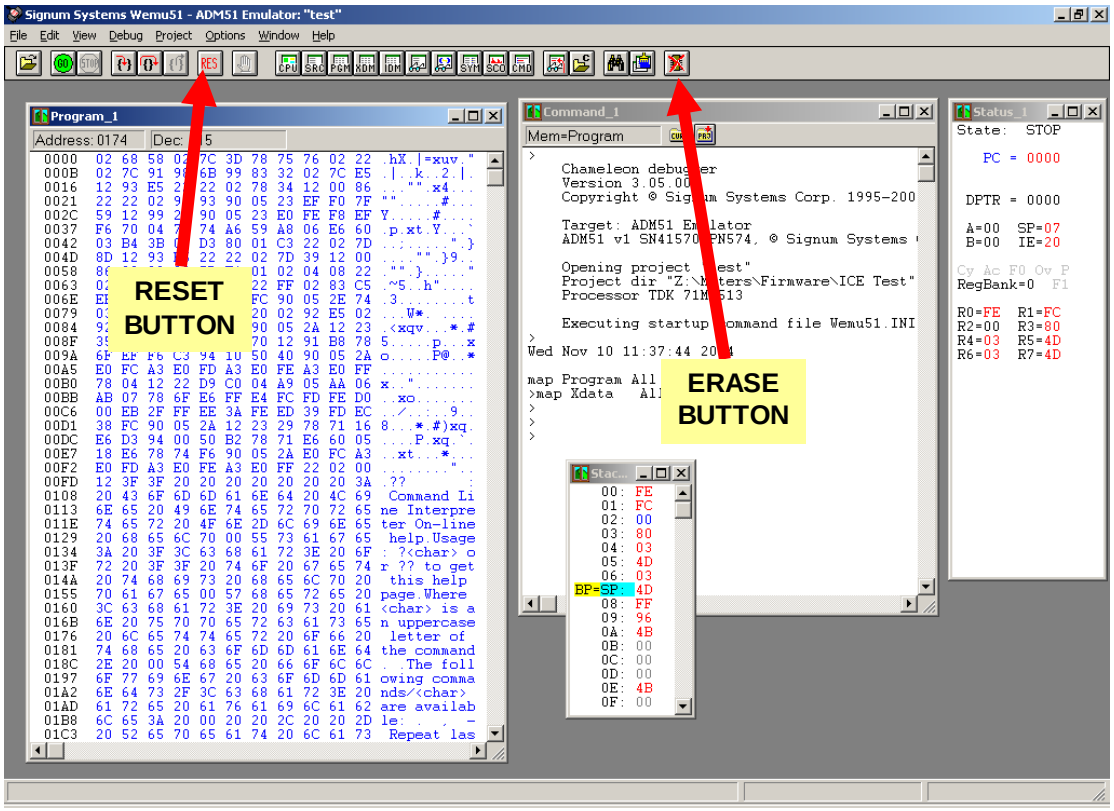


Figure 4: Emulator Window Showing RESET and ERASE Buttons

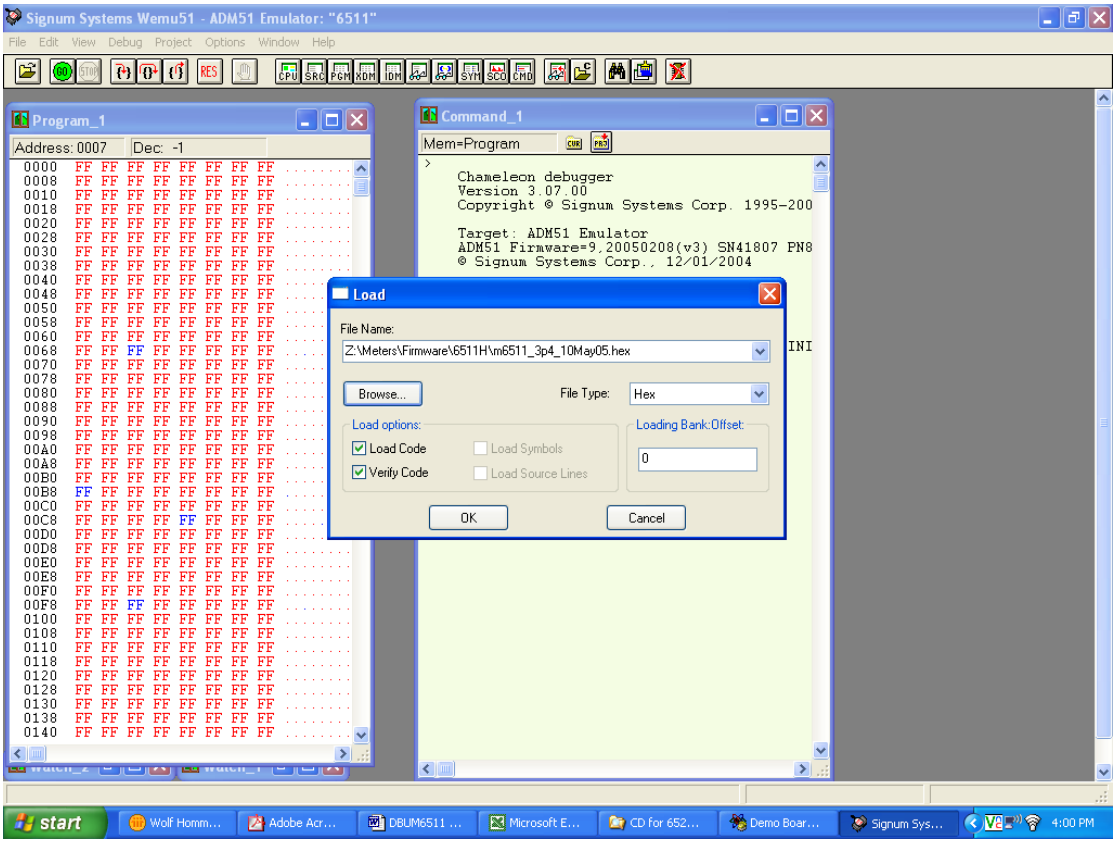


Figure 5: Emulator Window Showing Erased Flash Memory and File Load Menu

3 Using the PCCID Application

The PCCID firmware is pre-installed on the 73S1209F Evaluation Board. It requires a PC with the serial RS-232 port. When powered-up, the board is able to run the PCCID demonstration host application which allows:

- Smart card activation and deactivation, in ISO or EMV mode.
- Smart card APDU commands to be exchanged with the smart card inserted in the board.
- Starting a test sequence in order to test and evaluate the board performance against an EMV test environment.

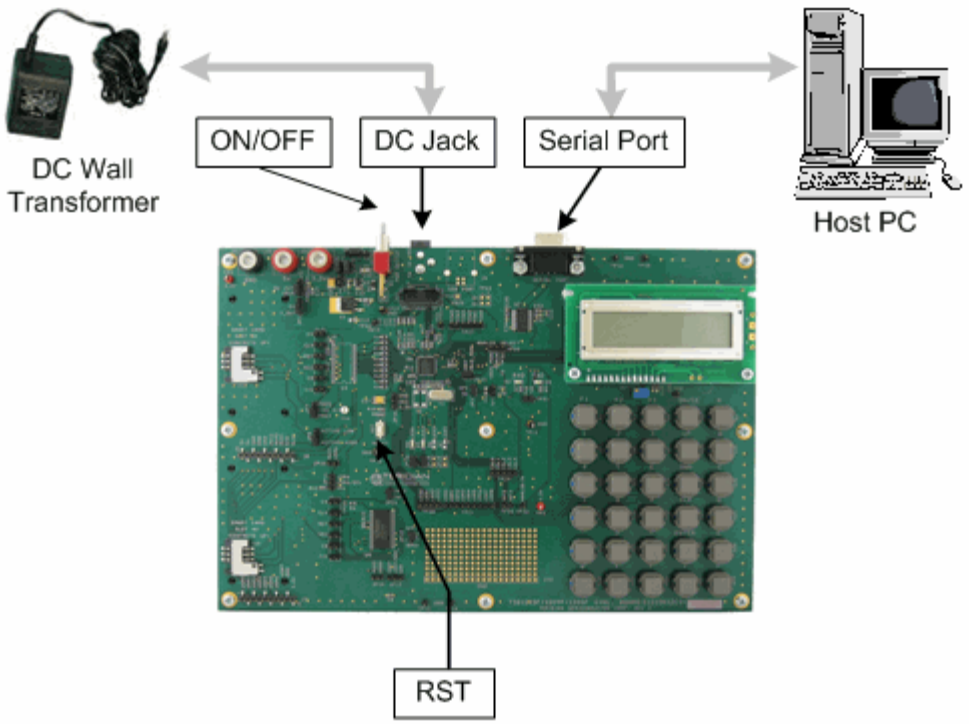
3.1 Host Demonstration Software Installation

Installation on Windows XP

Follow these steps to install the software on a PC running Windows XP:

- Extract "PCCID V***z.zz*** Release.zip" (where ***z.zz*** is the latest version of the firmware release).
  - Create an install directory. For example: "C:\TSC\".
  - Unzip "PCCID V***z.zz*** Release.zip" to the just created folder. All applications and documentation needed to run the board with a Windows PC will be loaded to this folder.
- Plug the supplied adapter into the 5V DC jack and a wall outlet.
- Connect the serial cable between the host system and the 73S1209F Evaluation Board.
- Press the ON/OFF switch to turn the board on.
- Run "TSCP-CCID.exe" (located in the path - ***x***:***yyy***\ PCCID V***z.zz*** Release\Host Applications\Windows App\App\Bin\Release) on the host system to execute the host demonstration application (where ***x*** refers to the drive, ***yyy*** refers to the directory the installation .zip file was expanded to and ***z.zz*** is the latest version of the firmware release).

At this point the application window should appear. For additional information regarding the use of the Teridian Host application, refer to the *Pseudo-CCID Host GUI Users Guide* (UG_12xxF_037).



4 Evaluation Board Hardware Description

4.1 Jumpers, Switches and Modules

Table 2 describes the 73S1209F Evaluation Board jumpers, switches and modules. The Item # in Table 2 references Figure 6. The default setting refers to setup for running USB-CCID application.

Table 2: Evaluation Board Jumper, Switch and Module Description

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
1	J2, J3, J5	No Connect	Banana plugs for external regulated power supply	Must be used to connect an external regulated power supply. These inputs are intended to allow control of the input supply voltage of the board (e.g. different than 5.0 V and 3.3 V on-board regulators). JP5 must be in position "5V EXT" and JP1 must be in position "5V "when using this 5 V power supply input. JP6 must be in position "EXT" "when using this 3.3 V power supply input.
 The evaluation board is sensitive to the polarity: One red plug is +3.3 V nominal and the other red plug is +5.0 V. The black plug is ground. The voltage supply input should be in the range +2.7 V to +3.6 V and 4.75 V to 5.5 V respectively.				
2	JP4	Inserted	VDD jumper	In normal use, a jumper must be inserted in this header, to connect the +3.3 V power supply of the board to the VDD pins of the 73S1209F. This jumper can be replaced by a μA / mA-meter to measure the actual current drawn by the 73S1209F.
3	JP3	Inserted	3.3 V jumper	In normal use, a jumper must be inserted in this header, to connect the +3.3 V power supply of the RS-232 transceiver and the 73S8010R. This jumper can be removed to minimize power consumption if these devices are not used.
4	JP6	'INT'	Jumper: power supply selection (#1)	A jumper must be inserted to select one of the following settings: • In position "EXT", the evaluation board 3.3 V is supplied from the external power supply inputs (banana plug J3). In this case, the voltage must be externally regulated. The power supply line is directly applied to the board power supply. This external power supply must not exceed 3.6 V. • In position "INT", the evaluation board is powered from the 3.3 V voltage regulator U1. The regulator can be powered either from the USB bus power supply (USB-powered application), or from an external non-regulated power supply (connector PJ1).
5	S1		Main switch	This switch turns the power On / Off to the evaluation board, when the jumper JP1 is in position "VOUT". When using a lab regulated power supply connected to the banana plugs J2 and J3, this switch has no effect.

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
6	PJ1	Connect	DC jack	Plug to connect an external DC block. Must be used in conjunction with appropriate settings of S1, JP1 and JP6 (see details above). Power supply features are: Voltage: 7 V min; 12 V max Current: 400 mA
7	J11	No Connect	In-Circuit Emulator connector	This connector must be used when using an external In-Circuit Emulator (SIGNUM 8052 ADM51 ICE). Refer to the Electrical Schematic for pin assignment.
8	JP20	Not Inserted	Jumper: analog in	Jumper will select between the VBUS or analog in test point for the analog input. Using VBUS on the analog input will free up the USR7 interrupt for other uses. The analog input can be set up to use the compare to detect when the USB cable is inserted/removed.
9	P1	No Connect	DB9 RS232 female socket	This socket allows connection of an RS232 cable to a computer. Use a crossed wires (RX/TX) cable. The evaluation board has an on-board level shifter (U7) to allow direct connection to a computer. Connection of a RS232 link is required when using the pre-downloaded application.
10	D2, D3, D4, D5		LEDs: Serial link activity and four dedicated LED pins.	These LEDs (D2, D3) reflect the activity on the serial link (RS232 or serial), and the others are used for general purpose indicators without the need for current limiting resistors. • D2 reflects the activity on the RX line (Data going TO the 73S1209F) • D3 reflects the activity on the TX line (Data coming FROM the 73S1209F) • D4 to D5 are the LED0-LED1 output pins .
11	U5		LCD Module	On-board LCD module: • 2 lines of 16 characters, each character dot matrix is 5x7. • Includes an embedded Hitachi HD44780 LCD driver, controlled from the on-board 73S1209F USR interface.
12	RV1		Adjustable resistor to adjust LCD brightness	Can be used to adjust the brightness of the on-board LCD module.
13	S2 to S31		On-board keypad	5x6 keyboard directly connected to the on-board 73S1209F IC. The assignment of the keys, as silk-printed on the PCB is the one supported by the TSC Application Programming Interface.
14	–		Board reference and serial number	Should be mentioned in any communication with TSC Application Engineers when requesting support.

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
15	JP2	Inserted	Jumper VPC	In normal use, a jumper must be inserted in this header to connect the +5.0 V power supply of the board to the VPC pins of the 73S1209F. This jumper can be replaced by a μA / mA-meter to measure the actual current drawn by the 73S1209F.
16	–		Breadboard area	This breadboard area allows engineers to add their own circuitry / connection of peripherals, when prototyping and developing a 73S1209F based application. User I/Os, GPIOs, interrupt pins and power supply pins are located close to this area to allow easy connection.
17	JP16, JP17	Inserted	Jumper: LED pins	In normal use, a jumper must be inserted in this header, to connect the LEDs to the LED pins of the 73S1209F. This jumper can be replaced by a μA / mA-meter to measure the actual current drawn by the LED outputs of the 73S1209F.
18	JP12	Inserted	Jumper: 73S8010R VPC connect	Insertion of the jumper will provide 5.0 V to the 73S8010R VPC pin. If the 73S8010R is not used, the jumper can be removed.
19	JP13	Not Inserted	Jumper: USR7/SDA select	This jumper selects which signal is connected to the daughter board connector pin USR7: • In position “USR7”, the 73S1209F USR7 signal is connected to the daughter card pin USR7. • In position “SDA”, the I2C SDA signal is connected to the daughter card pin USR7. This allows the SDA line to connect to an SDA pin on a 73S8010R daughter card.
20	JP14	Not Inserted	Jumper: USR5/AUX2 select	This jumper allows the on board 73S8010 AUX2 pin to be connected to USR5 if needed. If not needed the jumper should be removed.
21	U4		On board 73S8010R	The board contains a built-in 73S8010R that is connected to the external smart card interface of the 73S1209F. If not used, this device can be disconnected from the 73S1209F by removing jumpers JP12 and JP21.
22	JP21	Inserted	Jumper: 73S8010R interrupt	This jumper will allow the on-board 73S8010 interrupt output to connect to INT2 on the 73S1209F. Remove this jumper if the on-board 73S8010 is not used.
23	J7,J8	Not Inserted	Optional 73S80xxX Daughter Board interface	When developing applications that require more than 2 smart card interfaces, an optional daughter board can be populated to use the 73S1209F external smart card interface (lines SCIO and SCK), in conjunction with the USR(0:7) port and the INT2 interrupt input of the 73S1209F). Refer to the Electrical Schematic for pin assignment.

Item #	Schematic and Silkscreen Reference	Default setting	Name	Use
24	J9, J10		SIM / SAM and Smart Card connectors – external interface (#2)	Allows the evaluation board to communicate with a smart card using either the standard (credit card size) or SIM/SAM format. This slot is connected to the 73S1209F external card interface # 2. Note that J10 is wired is parallel to the smart card connector J9 (underneath the PCB). Both connectors cannot be populated at the same time.
25	JP11	Not Inserted	Jumper: USR6/SCL select	This jumper selects which signal is connected to the daughter board connector pin USR6: • In position “USR6”, the 73S1209F USR6 signal is connected to the daughter card pin USR6. • In position “SCL”, the I2C SCL signal is connected to the daughter card pin USR6. This allows the SCL line to connect to an SCL pin on a 73S8010R daughter card.
26	JP10	Not Inserted	Jumper: USR6/AUX1 select	This jumper allows the on board 73S8010 AUX1 pin to be connected to USR6 if needed. If not needed the jumper should be removed.
27	JP8	‘Active High’	Jumper: Selection of the polarity of the card detection switches of internal smart card connector	On-board smart card connectors and SIM/SAM connectors are equipped with card presence switches, normally open when no card is inserted. When the switches are closed (card inserted), the polarity must be selected by a jumper on JP8: • In position “ACTIVE HIGH”, the card detection switches connect +3.3 V to the card detection inputs of the 73S1209F. • In position “ACTIVE LOW”, the card detection switches connect ground to the card detection inputs of the 73S1209F. The 73S1209F firmware can handle both polarities for card detection. Therefore, this setting is firmware dependent. The default firmware settings are JP8 = ACTIVE HIGH and JP7 = PRES.
28	S27		Reset button	Evaluation board main reset: Asserts a hardware reset to the on-board 73S1209F IC.
29	JP7	‘PRES’	Jumper: Selection of the PRES and PRESB inputs	Selects the card detect input PRES or PRESB. PRES is the active high input and PRESB is the active low input. See item 29 for more detail.
30	JP15	‘GND’	Jumper: security fuse control	This jumper should be removed at all times. Connecting the jumper will allow the security fuses to be blown under firmware control. Refer to the *73S1209F Data Sheet* for further information about the security fuse.

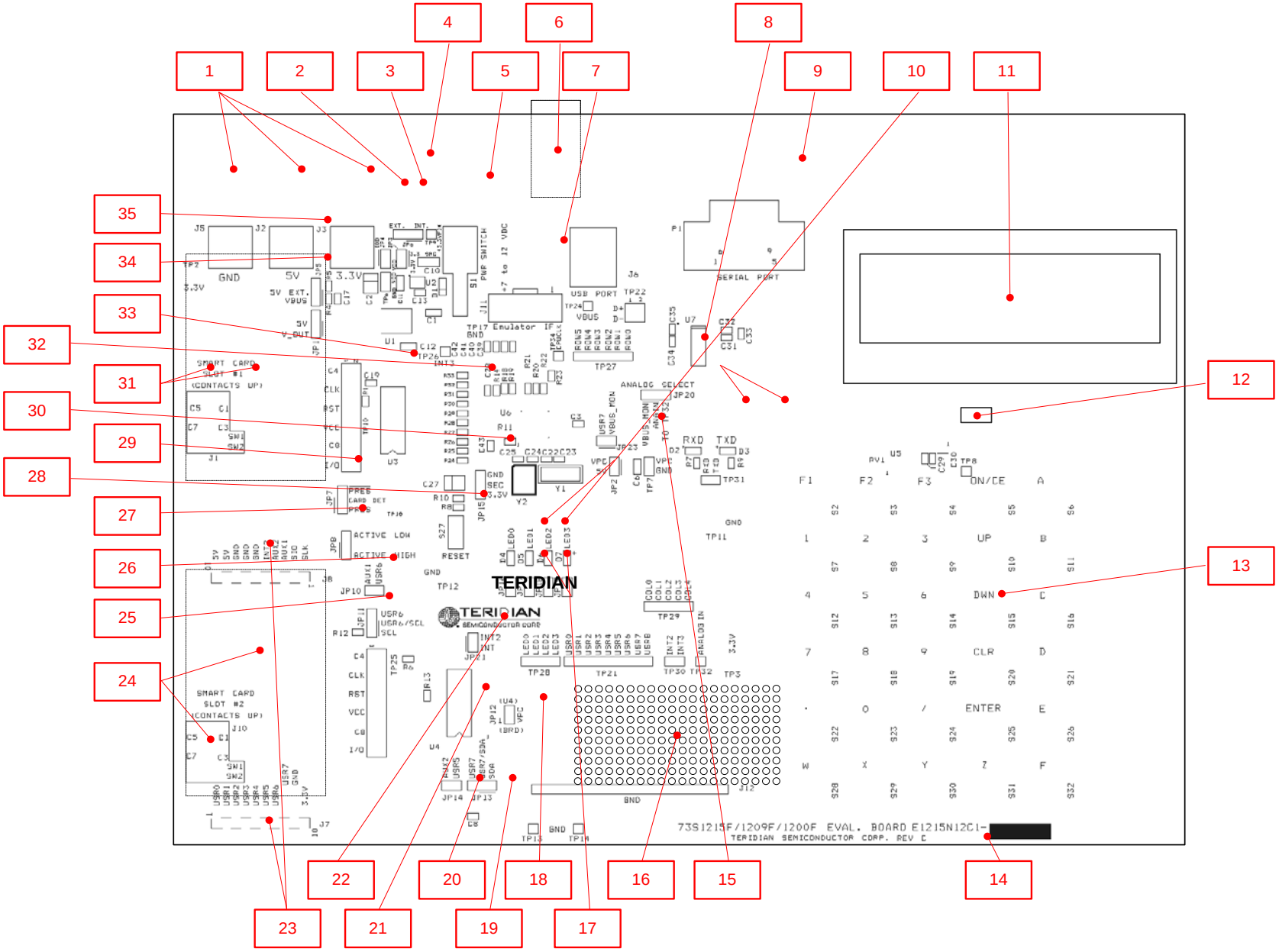


Figure 6: 73S1209F Evaluation Board Jumper, Switch and Module Locations

4.2 Test Points

The test point numbers listed in Table 3 refer to the test point numbers shown in the electrical schematic and in the silkscreen of the PCB.

Table 3: Evaluation Board Test Point Description

Test Point #	Name	Use
TP2, TP3	+3.3V	+3.3 V main board power supply, coming from the internal or external source, as defined from the jumpers JP3 and JP6. TP3 and TP4 are close to the breadboard area for easy wiring of the power supply.
TP6 TP7	VDD VPC	2-pin test point, with one ground and one VDD signal directly connected to the 73S1209F and its decoupling capacitors. Can be used to measure the integrity of the digital power supply of the 73S1209F, or to add a decoupling capacitor.
TP8	+5V	+5 V coming from the external DC block (connected to JP5), as selected with jumper on JP1. Can be used to test voltage presence.
TP9	+3.3VFIX	+3.3 V coming from the on-board regulator (powered up from the external DC block). Can be used to test voltage presence.
TP10	Smart Card Contacts – Interface #1	Header for measurement of the card signals, close to the card connectors. Contains the card signals VCC1, RST1, CLK1, C81 and C41. Each contact has its own ground pin on the header.
TP11 to TP17	GND	Ground test points. Can be used for grounding of lab equipment probes.
TP18	Card Detect – Interface #1	Card detect signal coming directly from the card connectors.
TP21	USR(7:0)	Standard 8-bit user I/O port of the 73S1209F.  Some of the user I/Os are shared by the extension 73S80xx daughter board and the LCD interface. Only one should be used at a time.
TP22	USB – N/A	TP22 is not populated with the 73S1209F.
TP24	VBUS – N/A	TP24 is not populated with the 73S1209F.
TP25	Smart Card Contacts – Interface #2	Header for measurement of the card signals, close to the card connectors. Contains the card signals VCC2, RST2, CLK2, C42 and C82. Each contact has its own ground pin on the header.
TP26	INT3	Interrupt input #3 secondary test points.
TP27	ROW[0:5]	The row pins used for the keypad interface.
TP28	LED0-1	The LED outputs from the 73S1209F. (LED2 and LED3 are N/C on the 73S1209F)
TP29	COL[0:4]	The column pins used for the keypad interface.
TP30	INT2-3	Interrupt input #2 and #3 of the 73S1209F. This header is close to the breadboard area for easy wiring.
TP31	RX, TX	The TX and RX serial UART I/O signals (3.3 V digital logic level).
TP32	ANALOG IN	Analog input test point. Analog voltage can be connected to this test point for voltage comparison.
TP34	CPUCLK	This pin outputs the oscillator clock of the 73S1209F device. Can be used as a clock source for any purpose.

4.3 Schematic

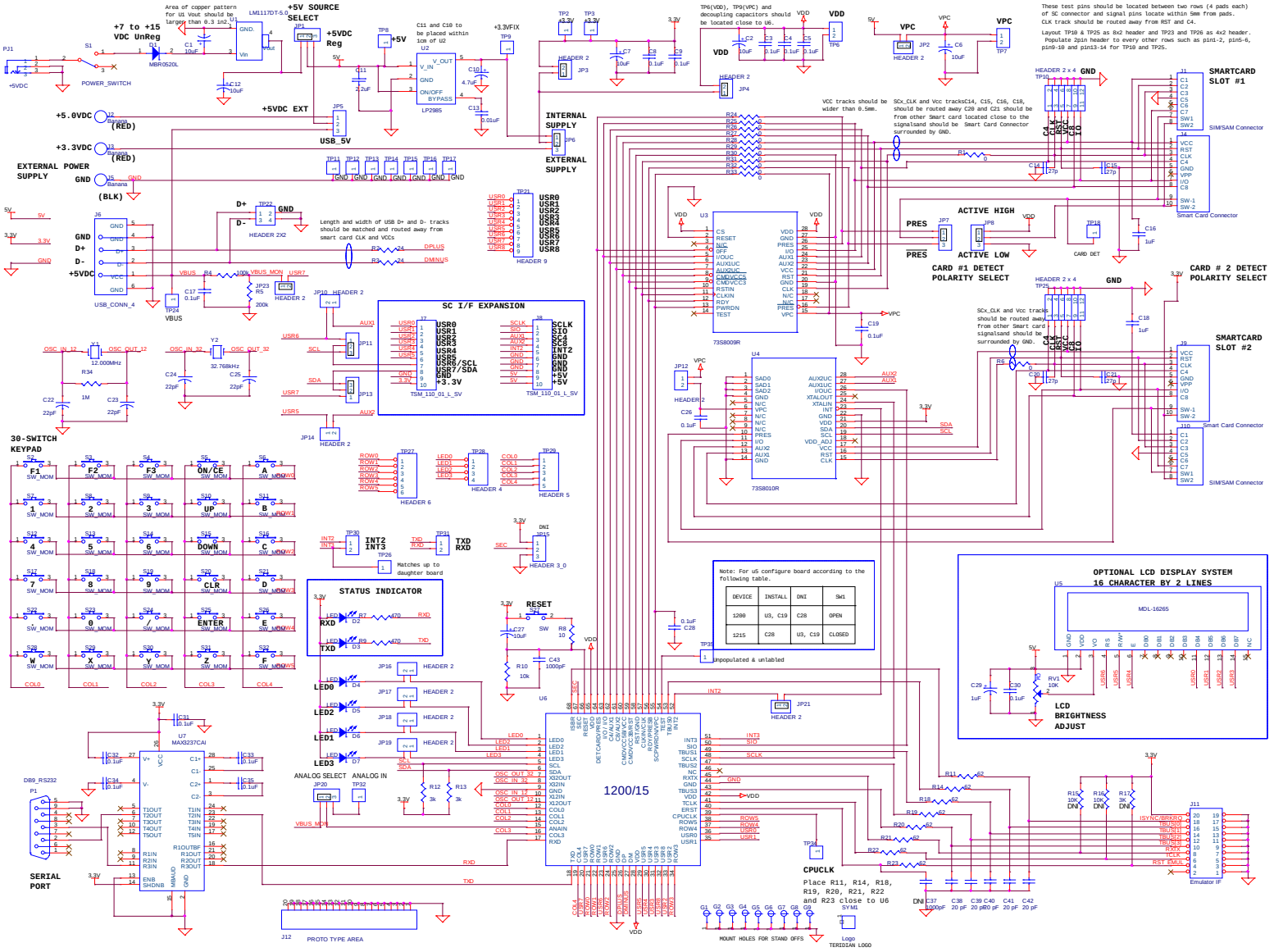


Figure 7: 73S1209F Evaluation Board Electrical Schematic

4.4 PCB Layouts

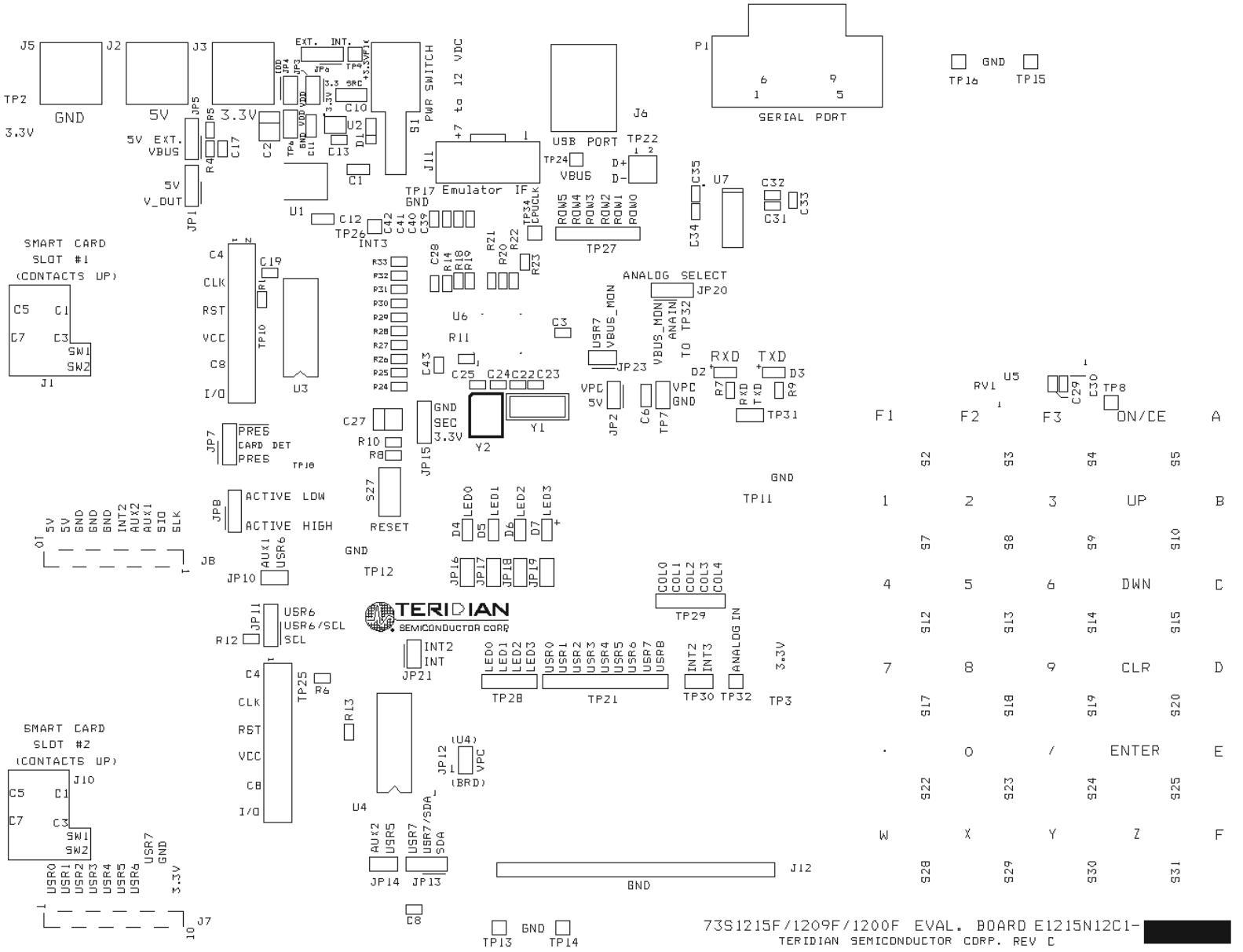


Figure 8: 73S1209F Evaluation Board Top View (Silkscreen)

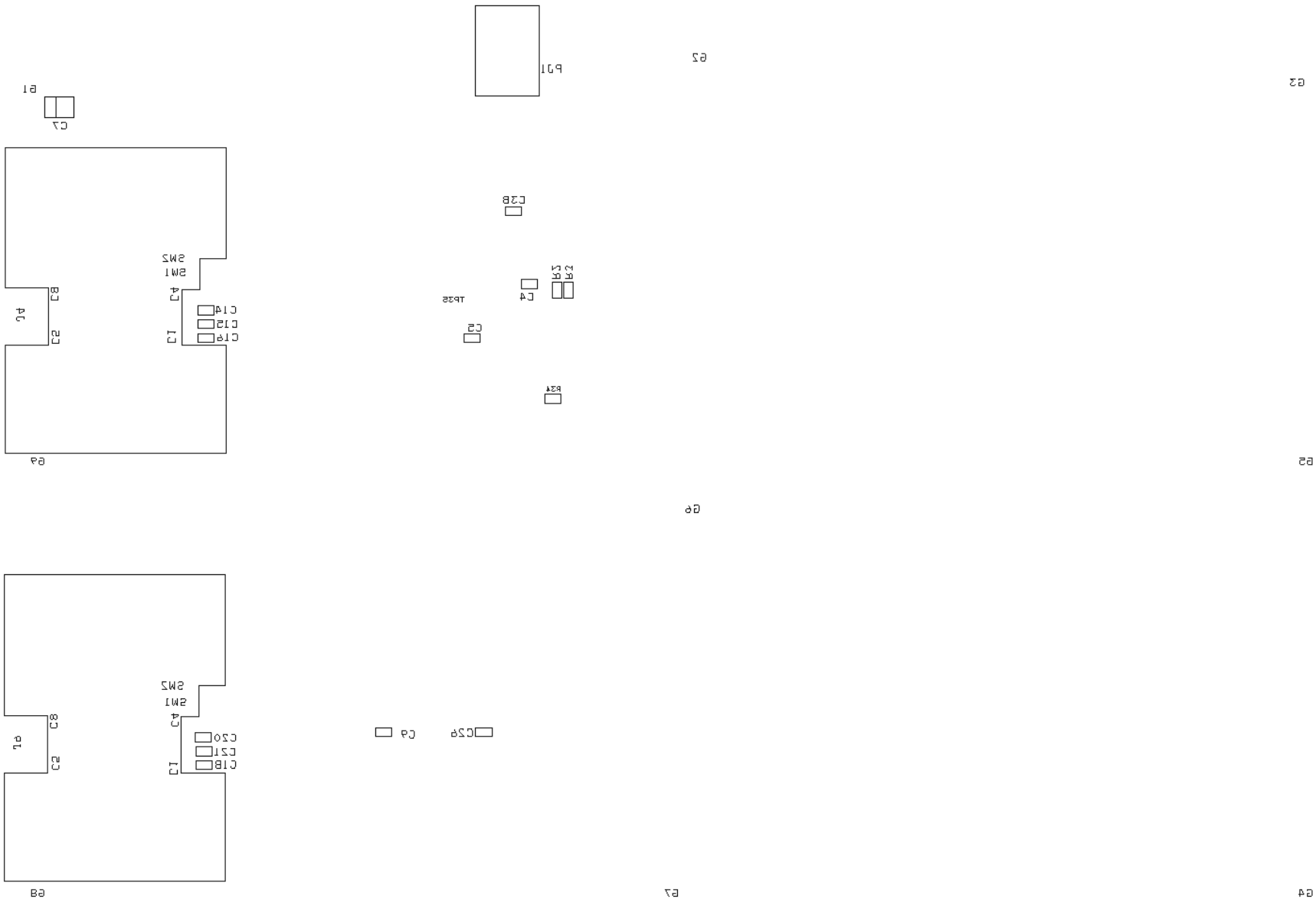


Figure 9: 73S1209F Evaluation Board Bottom View (Silkscreen)

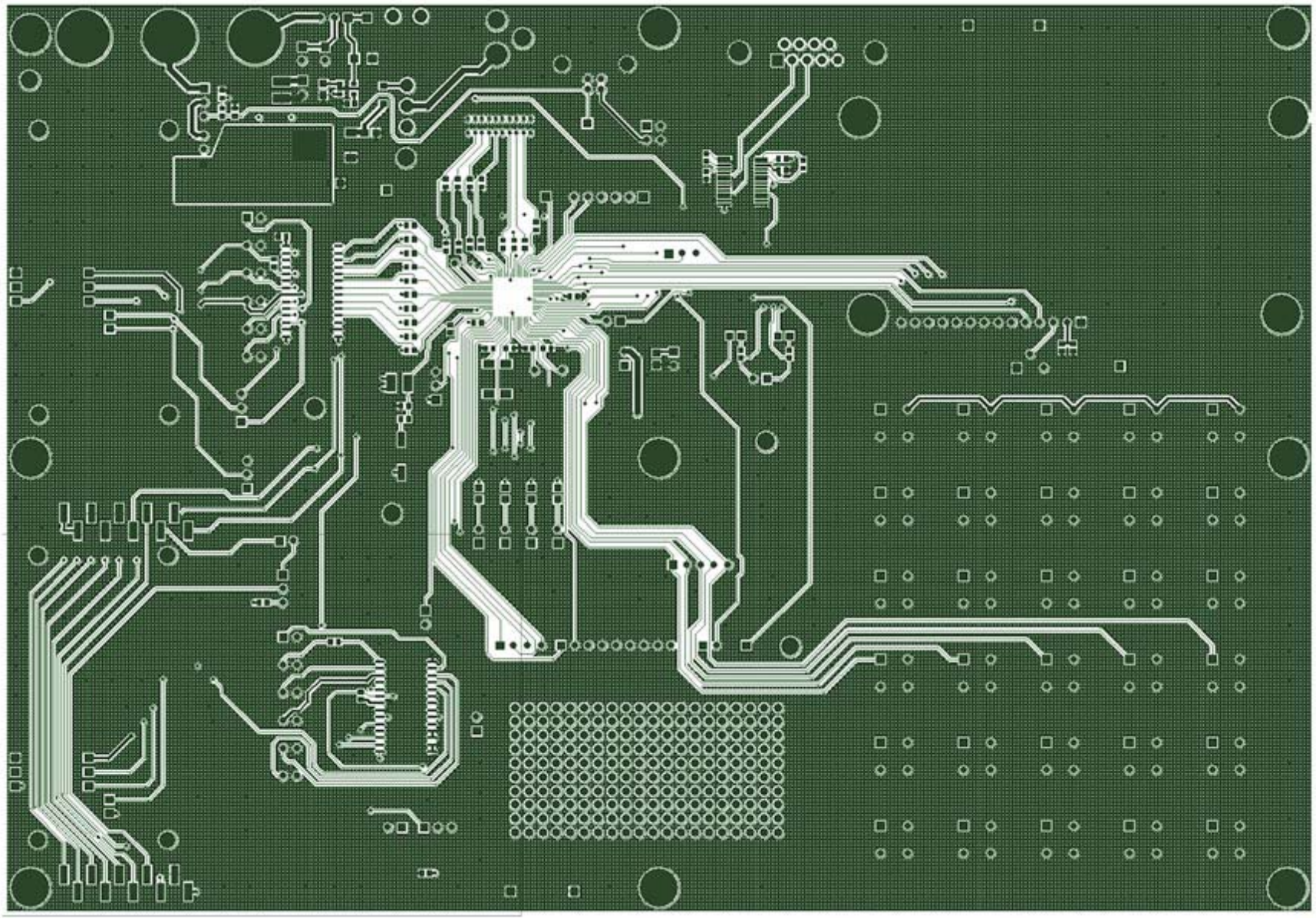


Figure 10: 73S1209F Evaluation Board Top Signal Layer

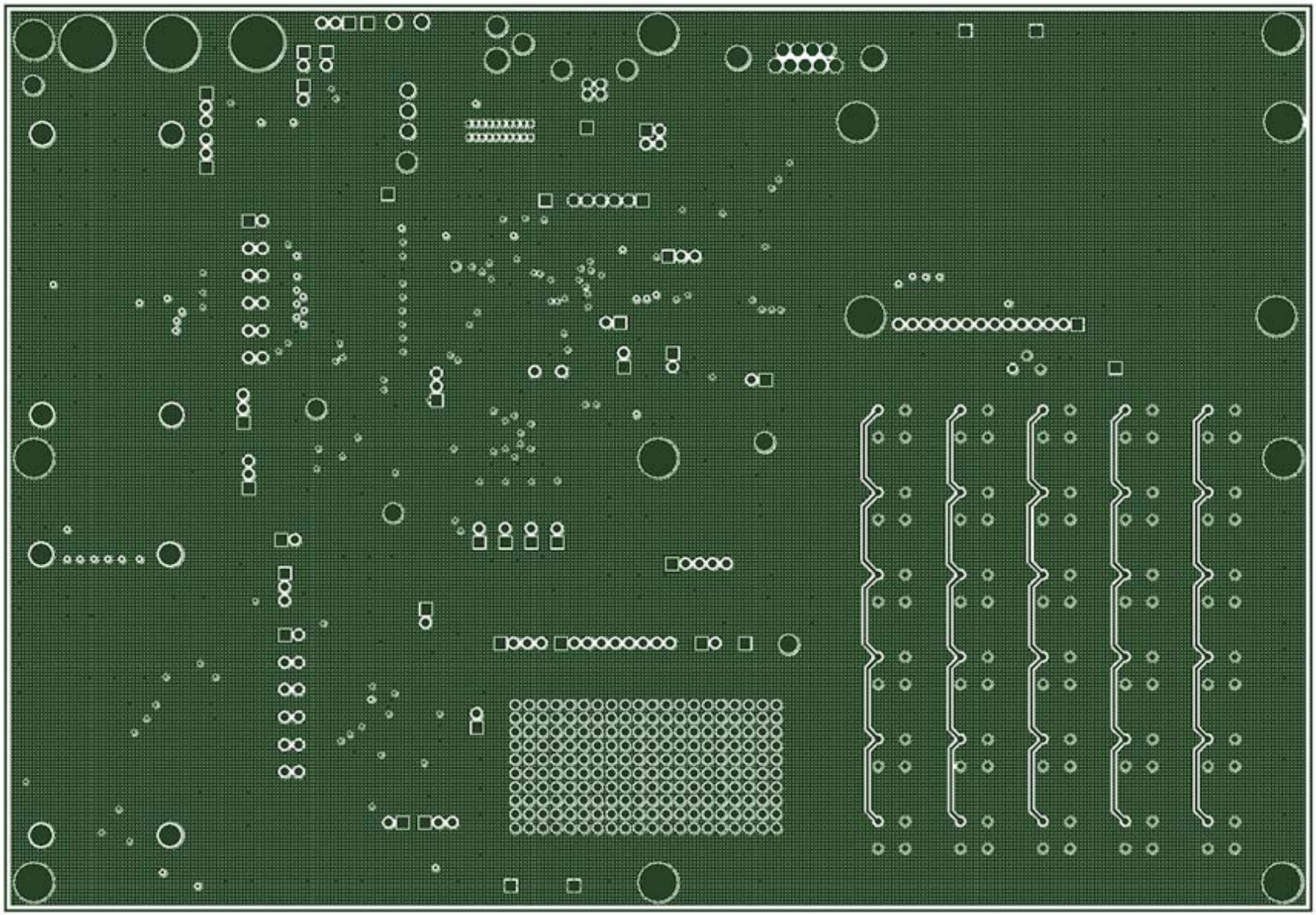


Figure 11: 73S1209F Evaluation Board Middle Layer 1 – Ground Plane

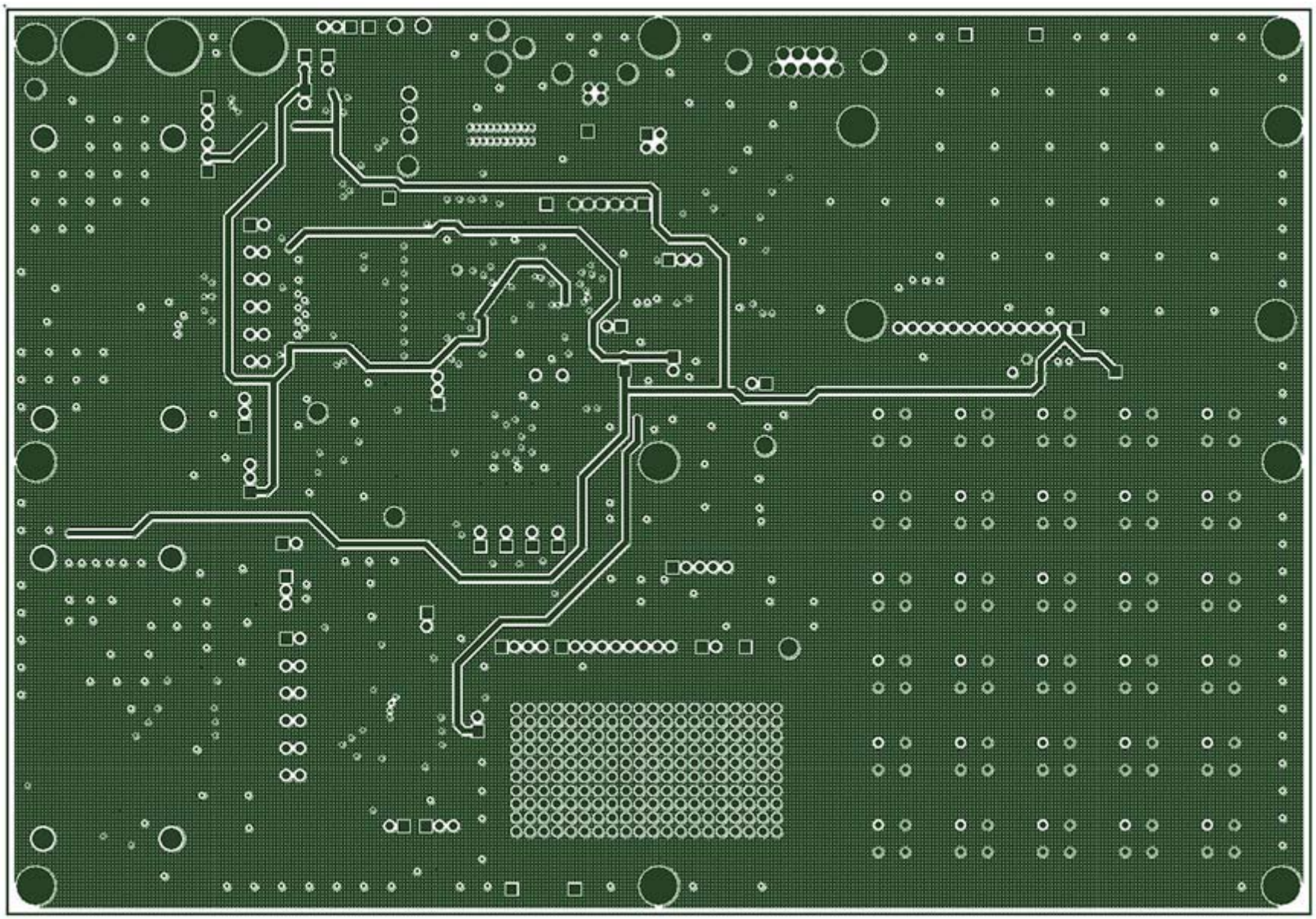


Figure 12: 73S1209F Evaluation Board Middle Layer 2 – Supply Plane

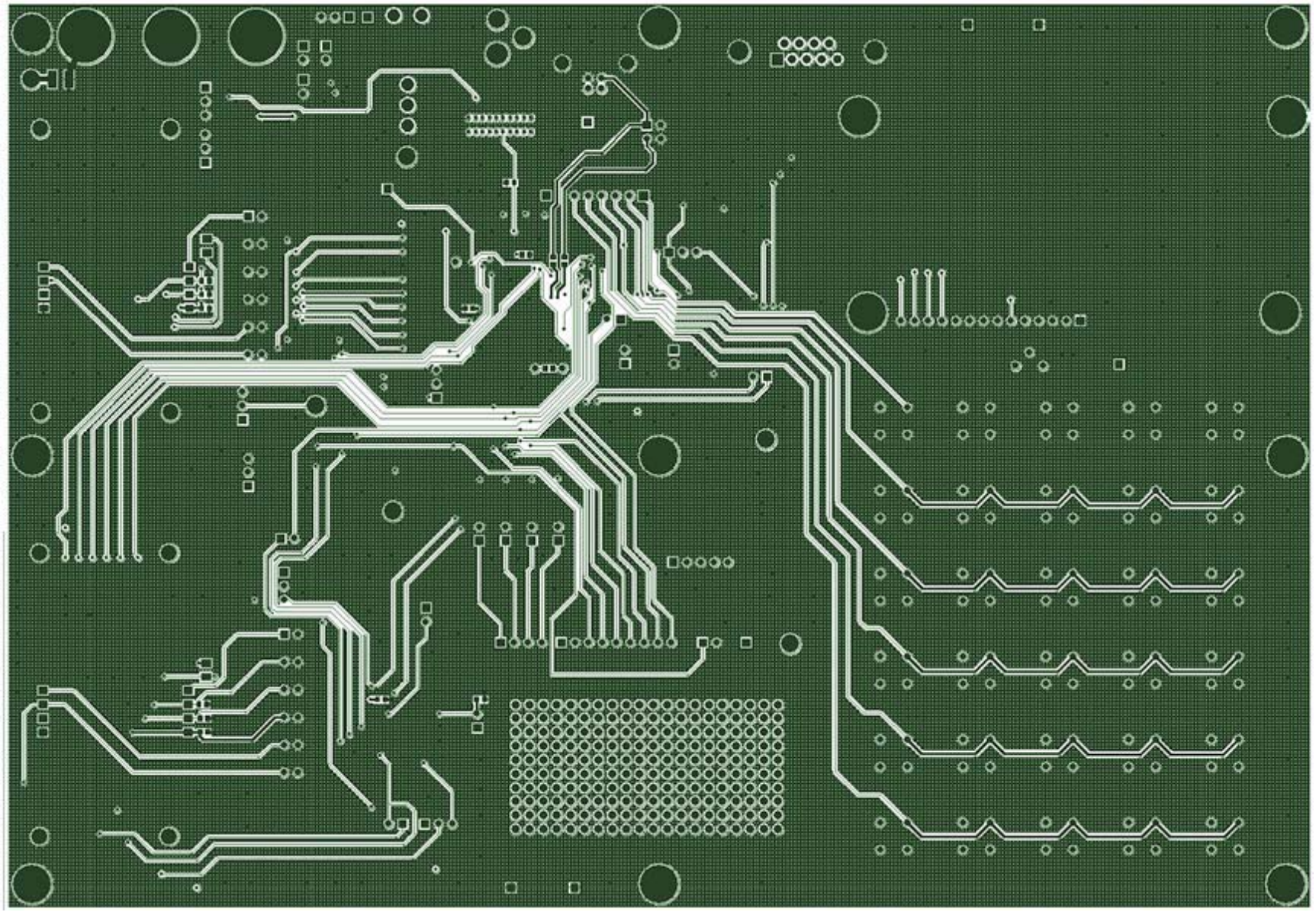


Figure 13: 73S1209F Evaluation Board Bottom Signal Layer

4.5 Bill of Materials

Table 4 provides the bill of materials for the 73S1209F Evaluation Board schematic provided in Figure 7.

Table 4: 73S1209F Evaluation Board Bill of Materials

Item	Qty.	Reference	Part	PCB Footprint	Digi-key Part Number	Part Number	Manufacturer
1	3	C2,C7,C27	10 µF	3528-21 (EIA)	478-1672-1-ND	TAJB106K010R	AVX Corporation
2	3	C1, C6,C12	10 µF	805	PCC2225CT-ND	ECJ-2FB0J106M	Panasonic
3	14	C3,C4,C5,C8,C9,C19, C26,C28,C30,C31,C32, C33, C34,C35	0.1 µF	603	PCC1762CT-ND	ECJ-1VB1C104K	Panasonic
4	1	C10	4.7 µF	603	PCC2396CT-ND	ECJ-1VB0J475K	Panasonic
5	1	C11	2.2 µF	805	PCC1923CT-ND	ECJ-2YB0J225K	Panasonic
6	1	C13	0.01 µF	603	445-1311-1-ND	C1608X7R1H103K	TDK Corporation
7	4	C14,C15,C20,C21	27 pF	603	PCC270ACVCT-ND	ECJ-1VC1H270J	Panasonic
8	3	C16,C18,C29	1 µF	603	PCC2174CT-ND	C1608X5R1A105K	TDK Corporation
9	2	C22,C23	22 pF	603	PCC220ACVCT-ND	ECJ-1VC1H220J	Panasonic
10	5	C38, C39, C40, C41, C42	20 pF	603	PCC200ACVCT-ND	ECJ-1VC1H200J	Panasonic
11	1	C43	1000 pF	603	PCC2151CT-ND	ECJ-1VC1H102J	Panasonic
12	1	D1	MBR0520L	SOD-123	MBR0520LCT-ND	MBR0520L	Fairchild
13	4	D2,D3,D4,D5	LED	805	160-1414-1-ND	LTST-C170FKT	LITE-ON INC
14	9	JP1,JP5,JP6,JP7,JP8, JP11, JP13,JP15, JP20	HEADER 3	1 x 3 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
15	9	JP2,JP3,JP4,JP10,JP12, JP14, JP16,JP17,JP21	HEADER 2	1 x 2 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
16	2	J1,J10	SIM/SAM Connector	ITT_CCM003_3754	CCM03-3754CT-ND	CCM03-3754CT-ND	C&K
17	2	J2,J3	Banana (red)	Banana		16BJ381	Mouser
18	1	J5	Banana (black)	Banana		16BJ382	Mouser
19	2	J9,J4	Smart Card Connector	ITT_CCM002-2504	CCM02-2504-ND	CCM02-2504-ND	C&K
20	2	J8,J7	TSM_110_01_L_SV	TSM_110_01_L_SV		TSM_110_01_L_SV	Samtec
21	1	J11	Emulator IF	10 X 2 pin	A3210-ND	104068-1	AMP/Tyco Electronics

Item	Qty.	Reference	Part	PCB Footprint	Digi-key Part Number	Part Number	Manufacturer
22	1	PJ1	+12VDC	RAPC722	SC1153-ND	RAPC722	Switchcraft
23	1	P1	DB9_RS232	AMP_745781	A2100-ND	745781-4	AMP/Tyco Electronics
24	1	RV1	10 kΩ	3266W	3266W-103-ND	3266W-1-103	Bourns
25	12	R1,R6,R24-33	0 Ω	603	P0.0GCT-ND	ERJ-3GEY0R00V	Panasonic
26	2	R7,R9	470 Ω	603	P470GCT-ND	ERJ-3GEYJ471V	Panasonic
27	1	R8	10 Ω	603	P10GCT-ND	ERJ-3GEYJ100V	Panasonic
28	1	R10	10 kΩ	603	P10KGCT-ND	ERJ-3GEYJ103V	Panasonic
29	8	R11,R14,R18,R19,R20, R21, R22,R23	62 Ω	603	P62GCT-ND	ERJ-3GEYJ620V	Panasonic
30	2	R12,R13	3 Ωk	603	P3.0KGCT-ND	ERJ-3GEYJ302V	Panasonic
31	1	R34	1 MΩ	603	P1.0MGCT-ND	ERJ-3GEYJ106V	Panasonic
32	1	S1	POWER_SWITCH	POW_SW	EG2364-ND	100SP1T2B4M7RE	E-Switch
33	30	S2,S3,S4,S5,S6,S7,S8, S9,S10,S11,S12,S13, S14S15,S16,S17,S18, S19,S20,S21,S22,S23, S24,S25,S26,S28,S29, S30,S31,S32	SW_MOM	Pushbutton SW	401-1885-ND	D6 C 10 LFS	ITT Industries
34	1	S27	SW	Panasonic EVQ	P8051SCT	EVQ-PJX05M	Panasonic
35	11	TP8,TP9,TP13,TP14, TP15,TP16,TP17,TP26, TP32, TP34, TP35	TP	1 Pin	S1011E-36-ND	PZC36SAAN	Sullins Electronics
36	1	TP18	TP	1 pin White	5012K-ND	5012	Keystone Electronics
37	2	TP2,TP3	TP	1 pin Red	5010K-ND	5010	Keystone Electronics
38	2	TP11,TP12	TP	1 pin Black	5011K-ND	5011	Keystone Electronics
39	4	TP6,TP7,TP30,TP31	TP2	1 x 2 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
40	2	TP10,TP25	HEADER 2 x 4	6 x 2 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
41	1	TP21	HEADER 9	1 x 9 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
42	1	TP27	HEADER 6	6 x 1 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
43	1	TP28	HEADER 4	4 x 1 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics
44	1	TP29	HEADER 5	5 x 1 pin	S1011E-36-ND	PBC36SAAN	Sullins Electronics

Item	Qty.	Reference	Part	PCB Footprint	Digi-key Part Number	Part Number	Manufacturer
45	1	U1	LM1117DT-5.0	TO-252-3	LM1117DT-5.0-ND	LM1117DT-5.0	National Semiconductor
46	1	U2	LP2985		LP2985IM5-3.3CT-ND	LP2985IM5-3.3	National Semiconductor
47	1	U4	73S8010R		73S8010R		Teridian Semiconductor
48	1	U5	MDL-16265		153-1078-ND	MDL-16265-SS-LV	Varitronix
49	1	U6	73S1209F	68 QFN		73S1209F	Teridian Semiconductor
50	1	U7	MAX3237CAI		MAX3237CAI-ND	MAX3237CAI	Maxim
51	1	Y1	12.000 MHz		X1116-ND	ECS-120-20-4XDN	ECS

4.6 Schematic Information

This section provides recommendations on proper schematic design that will help in designing circuits that are functional and compatible with the PCCID software library APIs.

4.6.1 Reset Circuit

The 73S1209F Evaluation Board provides a reset pushbutton that can be used when prototyping and debugging software. The RESET pin should be supported by the external components shown in Figure 14. R8 should be around 10 Ω. The capacitor C27 should be 10 µF. R8 and C27 should be mounted as close as possible to the IC.

C43 (1000 pF) is shown for EFT protection and is optional.

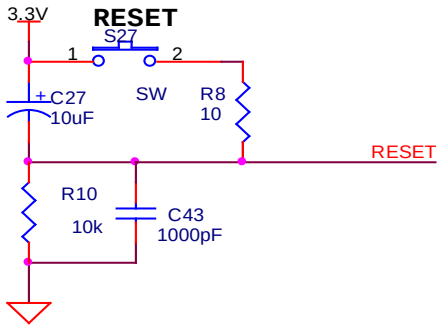


Figure 14: External Components for RESET

4.6.2 Oscillators

The 73S1209F contains an oscillator for the primary system clock. The system clock should use a 12 MHz crystal to provide the proper system clock rates for the serial and smart card interfaces. The system oscillator requires a 1 MΩ parallel resistor to insure proper oscillator startup (Figure 15).

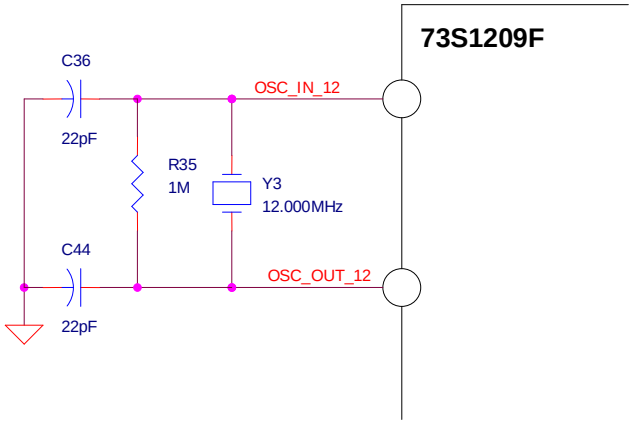


Figure 15: Oscillator Circuit

4.6.3 LCD

The 73S1209F does not contain an on-chip LCD controller. However, an LCD module (with built-in controller) can be used with the 73S1209F via use of specific USR (GPIO) pins. The LCD API libraries support up to a 2 line/16 character display. Figure 16 shows the basic connection for this type of LCD. The LCD module must connect to the USR pins as shown and it requires an external brightness adjust circuit.

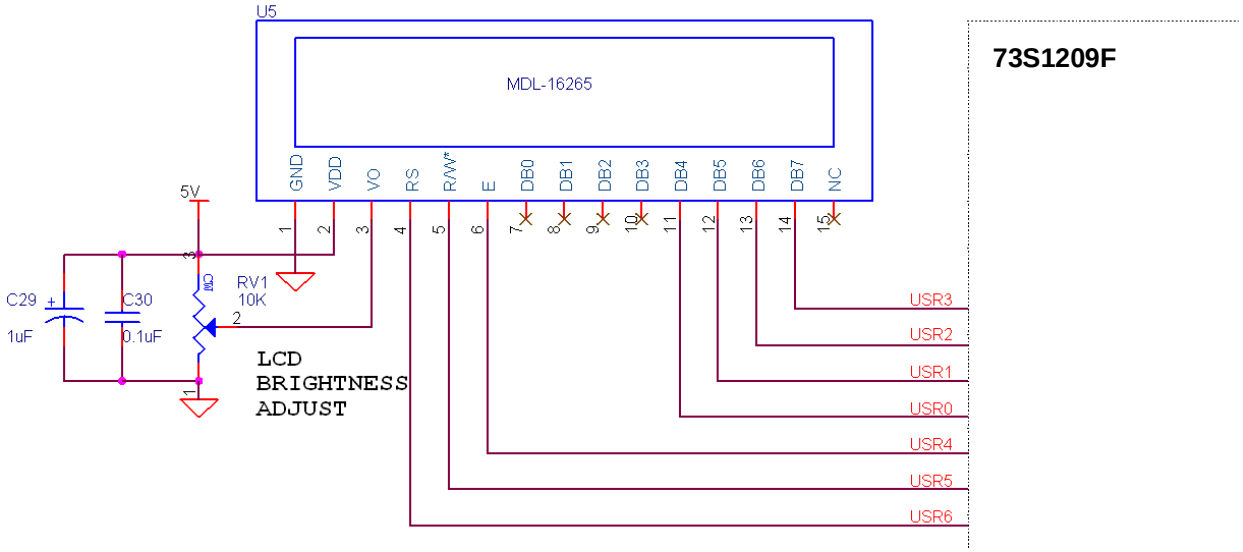


Figure 16: LCD Connections

4.6.4 Smart Card Interface

The smart card interface on the 73S1209F requires few external components for proper operation. Figure 17 shows the recommended smart card interface connections.

- The RST and CLK signals should have 27 pF capacitors at the smart card connector.
- It is recommended that a 0 Ω resistor be added in series with the CLK signal. If necessary, in noisy environments, this resistor can be replaced with a small resistor to create a RC filter on the CLK signal to reduce CLK noise. This filter is used to soften the clock edges and provide a cleaner clock for those environments where this could be problematic.
- The VCC output must have a 1.0 μF capacitor at the smart card connector for proper operation.
- The VPC input is the power supply input for the smart card power. It is recommended that both a 10 μF and a 0.1 μF capacitor are connected to provide proper decoupling for this input.
- The PRES input on the 73S1209F contains a very weak pull down resistor. As a result, an additional external pull down resistor is recommended to prevent any system noise from triggering a false card event. The same holds true for the $\overline{\text{PRES}}$ input, except a pull up resistor is utilized as the logic is inverted from the PRES input.

The smart card interface layout is important. The following guidelines should be followed to provide the optimum smart card interface operation:

- Route auxiliary signals away from card interface signals
- Keep CLK signal as short as possible and with few bends in the trace. Keep route of the CLK trace to one layer (avoid vias to other plane). Keep CLK trace away from other traces especially RST and VCC. Filtering of the CLK trace is allowed for noise purpose. Up to 30 pF to ground is allowed at the CLK pin of the smart card connector. Also, the zero ohm series resistor, R7, can be replaced for additional filtering (no more than 100 Ω).
- Keep VCC trace as short as possible. Make trace a minimum of 0.5 mm thick. Also, keep VCC away from other traces especially RST and CLK.
- Keep CLK trace away from VCC and RST traces. Up to 30 pF to ground is allowed for filtering
- Keep 0.1 μF close to VDD pin of the device and directly take other end to ground
- Keep 10 μF and 0.1 μF capacitors close to VPC pin of the device and directly take other end to ground
- Keep 1.0 μF close to VCC pin of the smart card connector and directly take other end to ground

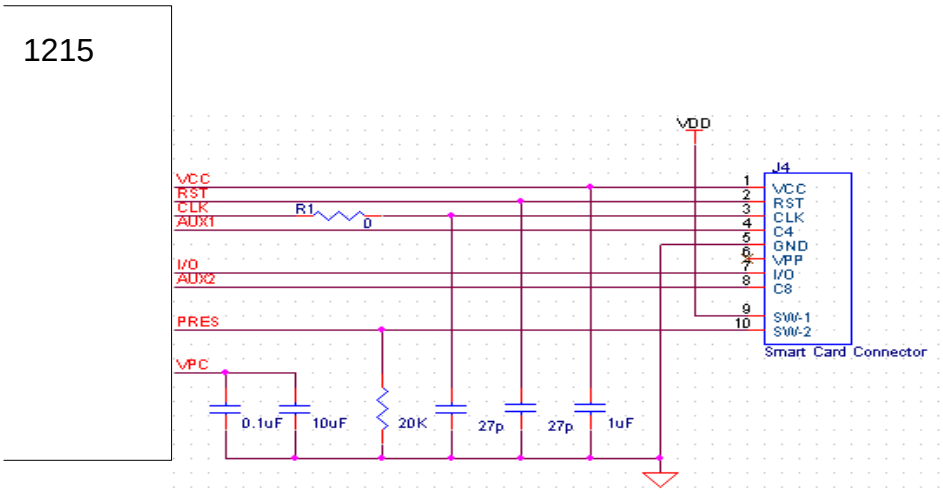


Figure 17: Smart Card Connections

5 Ordering Information

Part Description	Order Number
73S1209F 68-Pin QFN Evaluation Board	73S1209F-EB

6 Related Documentation

The following 73S1209F documents are available from Teridian Semiconductor Corporation:

73S1209F Data Sheet
73S1209F Evaluation Board Quick Start Guide
TSC Flash Programmer Model TFP2 User's Manual

7 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S1209F contact us at:

6440 Oak Canyon Road
Suite 100
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: scr.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	January 22, 2007	Document Creation.
1.1	April 2, 2007	Update BOM and change to Rev C PWB. Remove board errata section.
1.2	August 8, 2007	Modify incorrect part number for S1 in BOM.
1.3	August 19, 2009	Remove 44-pin board and LAPIE references. Miscellaneous editorial modifications.