

56F8025 Digital Signal Controller Product Brief

1 56F8025 Description

The 56F8025 is a member of the 56800E core-based family of Digital Signal Controllers (DSCs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F8025 is well-suited for many applications. The 56F8025 includes many peripherals that are especially useful for industrial control, motion control, home appliances, general-purpose inverters, smart sensors, fire and security systems, switched-mode power supply, power management, and medical monitoring applications.

The 56800E core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

Contents

1	56F8025 Description	1
2	Digital Signal Controller Core	3
3	Memory	3
4	Peripheral Circuits for 56F8025	3
5	Recommended Operating Conditions	5
6	Product Documentation	6
7	56F8025 Package and Pin-Out	7

The 56F8025 supports program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The 56F8025 also offers up to 35 General-Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F8025 Digital Signal Controller includes 32KB of Program Flash and 4KB of Unified Data/Program RAM. Program Flash memory can be independently bulk erased or erased in pages. Program Flash page erase size is 512 Bytes (256 Words).

A full set of programmable peripherals — PWM, ADCs, QSCI, QSPI, I2C, PIT, Quad Timers, DACs, and analog comparators — supports various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as General Purpose Input/Outputs (GPIOs).

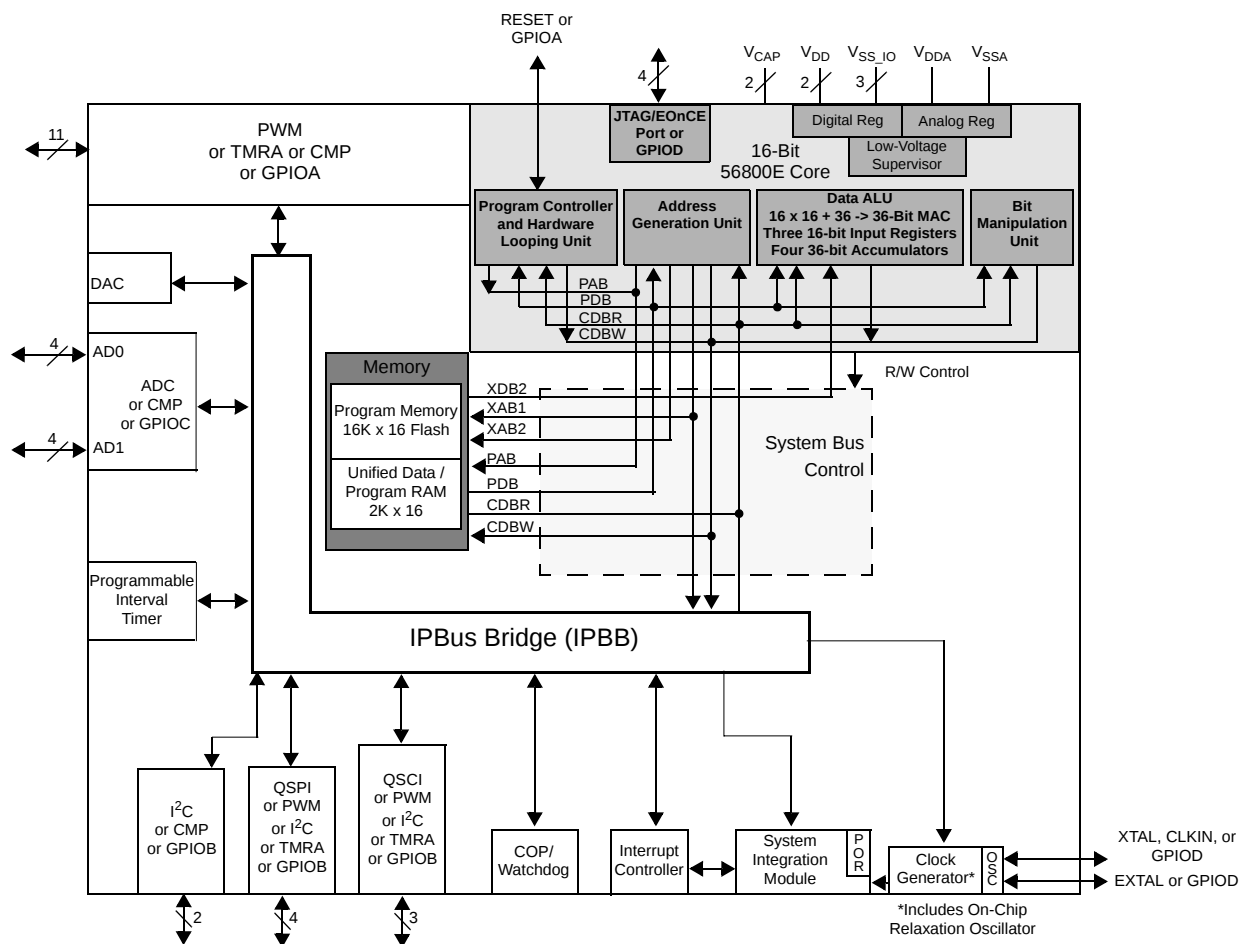


Figure 1. 56F8025 Block Diagram

2 Digital Signal Controller Core

- Efficient 16-bit 56800E family Digital Signal Controller (DSC) engine with dual Harvard architecture
- As many as 32 Million Instructions Per Second (MIPS) at 32MHz core frequency
- Single-cycle 16×16 -bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent real-time debugging

3 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal Flash
- On-chip memory
 - 32KB of Program Flash
 - 4KB of Unified Data/Program RAM
- EEPROM emulation capability using Flash

4 Peripheral Circuits for 56F8025

- One multi-function six-output Pulse Width Modulator (PWM) module
 - Up to 96MHz PWM operating clock
 - 15 bits of resolution
 - Center-aligned and edge-aligned PWM signal mode
 - Four programmable fault inputs with programmable digital filter
 - Double-buffered PWM registers
 - Each complementary PWM signal pair allows selection of a PWM supply source from:
 - PWM generator
 - External GPIO
 - Internal timers
 - Analog comparator outputs
 - ADC conversion result which compares with values of ADC high- and low-limit registers to set PWM output

- Two independent 12-bit Analog-to-Digital Converters (ADCs)
 - 2 x 4 channel inputs
 - Supports both simultaneous and sequential conversions
 - ADC conversions can be synchronized by both PWM and timer modules
 - Sampling rate up to 2.67MSPS
 - 16-word result buffer registers
- Two internal 12-bit Digital-to-Analog Converters (DACs)
 - 2 microsecond settling time when output swing from rail to rail
 - Automatic waveform generation generates square, triangle and sawtooth waveforms with programmable period, update rate, and range
- One 16-bit multi-purpose Quad Timer module (TMR)
 - Up to 96MHz operating clock
 - Eight independent 16-bit counter/timers with cascading capability
 - Each timer has capture and compare capability
 - Up to 12 operating modes
- One Queued Serial Communication Interface (QSCI) with LIN Slave functionality
 - Full-duplex or single-wire operation
 - Two receiver wake-up methods:
 - Idle line
 - Address mark
 - Four-bytes-deep FIFOs are available on both transmitter and receiver
- One Queued Serial Peripheral Interfaces (QSPI)
 - Full-duplex operation
 - Master and slave modes
 - Four-words-deep FIFOs available on both transmitter and receiver
 - Programmable Length Transactions (2 to 16 bits)
- One Inter-Integrated Circuit (I²C) port
 - Operates up to 400kbps
 - Supports both master and slave operation
 - Supports both 10-bit address mode and broadcasting mode
- Three 16-bit Programmable Interval Timers (PITs)
- Two analog Comparators (CMPs)
 - Selectable input source includes external pins, DACs
 - Programmable output polarity
 - Output can drive Timer input, PWM fault input, PWM source, external pin output and trigger ADCs

- Output falling and rising edge detection able to generate interrupts
- Computer Operating Properly (COP)/Watchdog timer capable of selecting different clock sources
- Up to 35 General-Purpose I/O (GPIO) pins with 5V tolerance
- Integrated Power-On Reset (POR) and Low-Voltage Interrupt (LVI) module
- Phase Lock Loop (PLL) provides a high-speed clock to the core and peripherals
- Clock sources:
 - On-chip relaxation oscillator
 - External clock: Crystal oscillator, ceramic resonator, and external clock source
- JTAG/EOnCE debug programming interface for real-time debugging

5 Recommended Operating Conditions

Table 1. Recommended Operating Conditions

($V_{REFL\ x} = 0V$, $V_{SSA} = 0V$, $V_{SS} = 0V$)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD} , V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High	V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD_IO} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS_IO} to V_{SSA}	ΔV_{SS}		-0.3	0	0.3	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		1 0		32 32	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3		0.8	V
Oscillator Input Voltage High XTAL not driven by an external clock XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	$V_{DDA} - 0.8$ 2.0		$V_{DDA} + 0.3$ $V_{DDA} + 0.3$	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Analog Input Voltage	V_{IA}	Pin Group 3	0.0		V_{DDA}	V

Table 1. Recommended Operating Conditions (continued)(V_{REFL} = 0V, V_{SSA} = 0V, V_{SS} = 0V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Output Source Current High at V _{OH} min.) ¹ When programmed for low drive strength When programmed for high drive strength	I _{OH}	Pin Group 1 Pin Group 1	— —		-4 -8	mA
Output Source Current Low (at V _{OL} max.) ¹ When programmed for low drive strength When programmed for high drive strength	I _{OL}	Pin Groups 1, 2 Pin Groups 1, 2	— —		4 8	mA
Ambient Operating Temperature (Automotive)	T _A		-40		125	°C
Ambient Operating Temperature (Extended Industrial)	T _A		-40		105	°C
Flash Endurance (Program Erase Cycles)	N _F	T _A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention	T _R	T _J ≤ 70°C average	15		—	years

¹ Total chip source or sink current cannot exceed 75mA

6 Product Documentation

The documents listed in [Table 2](#) are required for a complete description and proper design with the 56F8025. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at:

<http://www.freescale.com>

Table 2. 56F8025 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit Digital Signal Controller core processor, and the instruction set	DSP56800ERM
56F802X and 56F803X Peripheral Reference Manual	Detailed description of peripherals of the 56F802x and 56F803x family of devices	MC56F80XXRM
56F802X and 56F803X Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F802x and 56F803x family of devices	56F80XXBLUG
56F8025 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8025
56F8025 Errata	Details any chip issues that might be present	MC56F8025E

7 56F8025 Package and Pin-Out

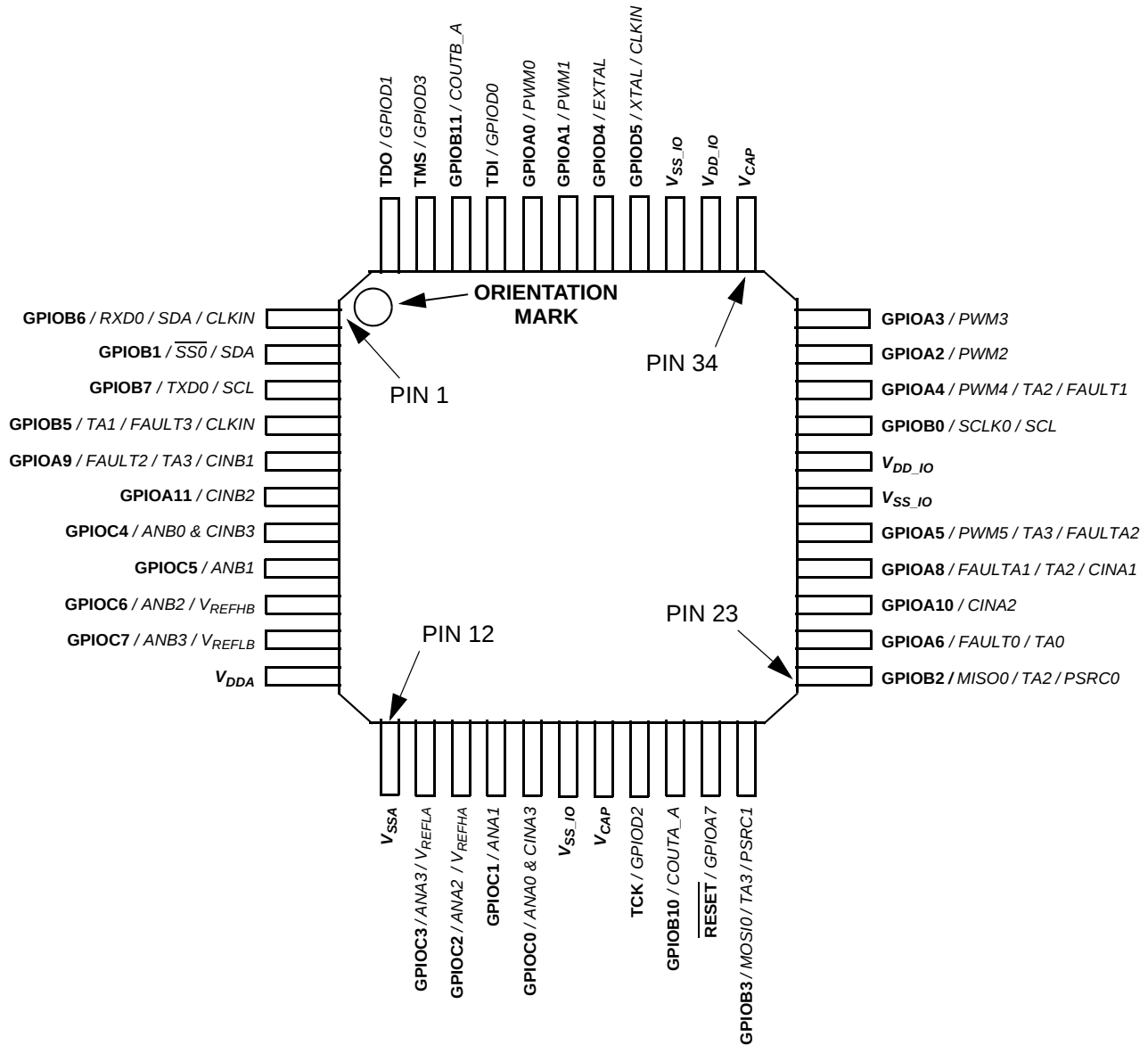


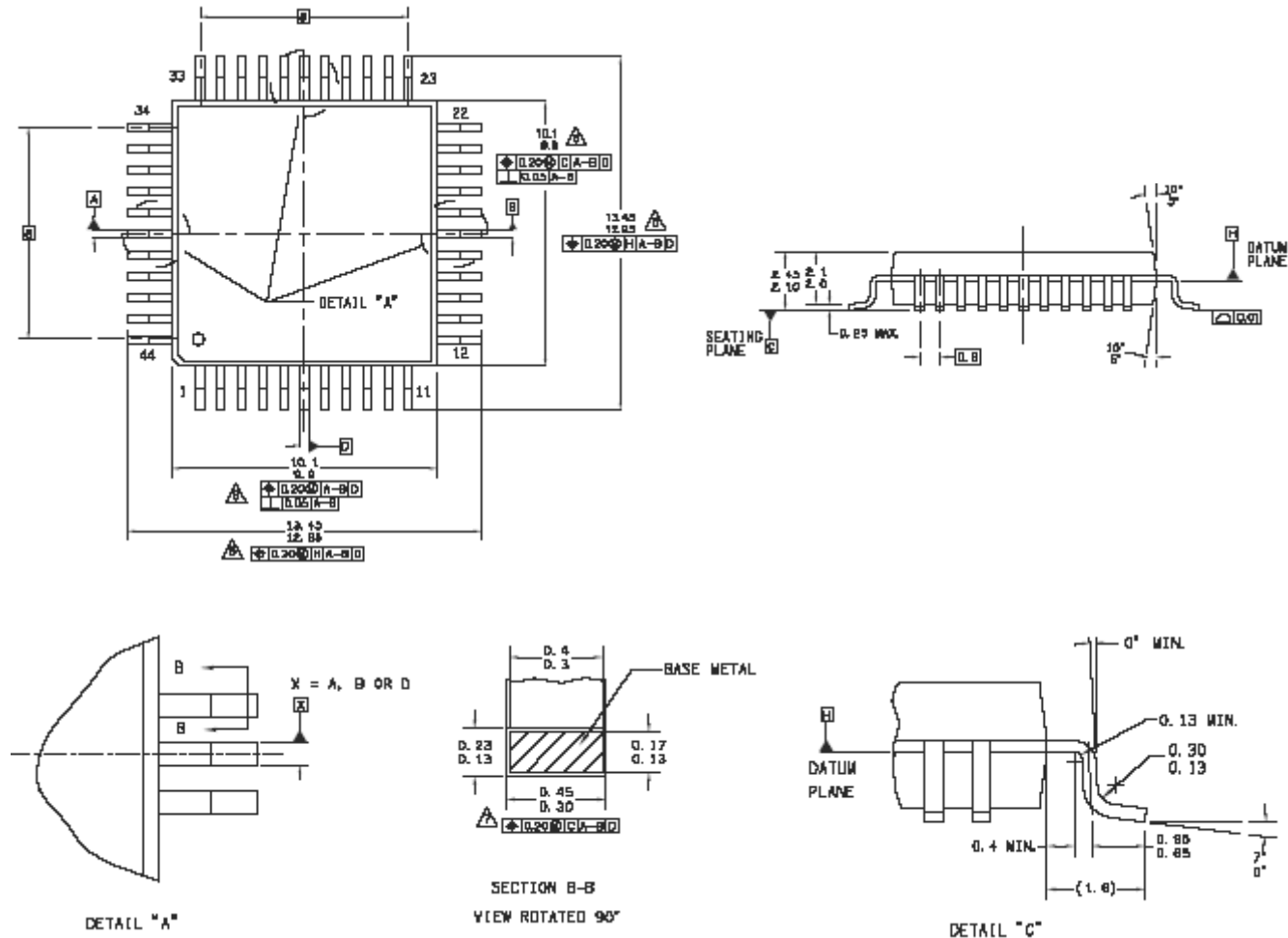
Figure 2. Top View, 56F8025 48-Pin LQFP Package

Peripheral pins in bold identify the reset state in [Table 3](#).

Table 3. 56F8025 44-Pin LQFP Package Identification by Pin Number¹

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	GPIOB6 <i>RXD0 / SDA / CLKIN</i>	12	V_{SSA}	23	GPIOB2 <i>MISO0 / TA2 / PSRC0</i>	34	V_{CAP}
2	GPIOB1 <i>SS0 / SDA</i>	13	GPIOC3 <i>ANA3 / V_{REFLA}</i>	24	GPIOA6 <i>FAULT0 / TA0</i>	35	V_{DD_IO}
3	GPIOB7 <i>TXD0 / SCL</i>	14	GPIOC2 <i>ANA2 / V_{REFHA}</i>	25	GPIOA10 <i>CINA2</i>	36	V_{SS_IO}
4	GPIOB5 <i>TA1 / FAULT3 / CLKIN</i>	15	GPIOC1 <i>ANA1</i>	26	GPIOA8 <i>FAULT1 / TA2 / CINA1</i>	37	GPIOD5 <i>XTAL / CLKIN</i>
5	GPIOA9 <i>FAULT2 / TA3 / CINB1</i>	16	GPIOC0 <i>ANA0 & CINA3</i>	27	GPIOA5 <i>PWM5 / TA3 / FAULT2</i>	38	GPIOD4 <i>EXTAL</i>
6	GPIOA11 <i>CINB2</i>	17	V_{SS_IO}	28	V_{SS_IO}	39	GPIOA1 <i>PWM1</i>
7	GPIOC4 <i>ANB0 & CINB3</i>	18	V_{CAP}	29	V_{DD_IO}	40	GPIOA0 <i>PWM0</i>
8	GPIOC5 <i>ANB1</i>	19	TCI <i>GPIOD2</i>	30	GPIOB0 <i>SCLK0 / SCL</i>	41	TDI <i>GPIOD0</i>
9	GPIOC6 <i>ANB2 / V_{REFHB}</i>	20	GPIOB10 <i>COUTA_A</i>	31	GPIOA4 <i>PWM4 / TA2 / FAULT1</i>	42	GPIOB11 <i>COUTB_A</i>
10	GPIOC7 <i>ANB3 / V_{REFLB}</i>	21	RESET <i>GPIOA7</i>	32	GPIOA2 <i>PWM2</i>	43	TMS <i>GPIOD3</i>
11	V_{DDA}	22	GPIOB3 <i>MOSI0 / TA3 / PSRC1</i>	33	GPIOA3 <i>PWM3</i>	44	TDO <i>GPIOD1</i>

¹ Alternate signals are in italic



NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUMPLANE —H— IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A—B AND —D— TO BE DETERMINED AT DATUM PLANE —H—.
5. THIS DIMENSION TO BE DETERMINED AT SEATING PLANE —C—.
6. THIS DIMENSION DO NOT INCLUDE MOLD PROTRUSION, ALLOWABLE PROTRUSION IS 0.25 PER SIDE, DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE —H—.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

Figure 3. 56F8025 44-Pin LQFP Mechanical Information

Please see www.freescale.com for the most current case outline.



THIS PAGE IS INTENTIONALLY BLANK



THIS PAGE IS INTENTIONALLY BLANK

How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2006. All rights reserved.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics as their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

Document Number: MC56F8025PB
Rev. 0
09/2006

Preliminary—Subject to Change Without Notice

