PCI-EXPRESS GEN1 CLOCK SOURCE

ICS557-01

Description

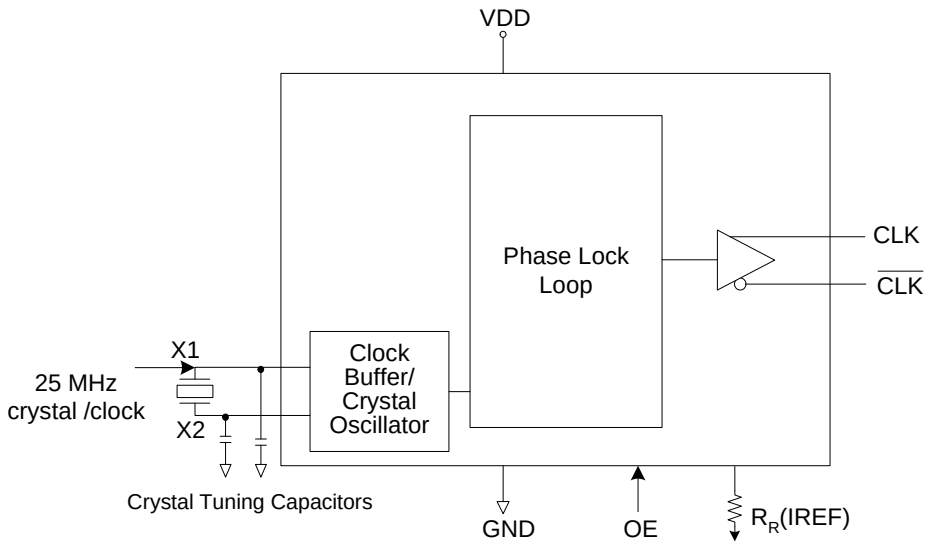
The ICS557-01 is a clock chip designed for use in PCI-Express Cards as a clock source. It provides a pair of differential outputs at 100 MHz in a small 8-pin SOIC package.

Using IDT's patented Phase-Locked Loop (PLL) techniques, the device takes a 25 MHz crystal input and produces HCSL (Host Clock Signal Level) differential outputs at 100 MHz clock frequency. LVDS signal levels can also be supported via an alternative termination scheme.

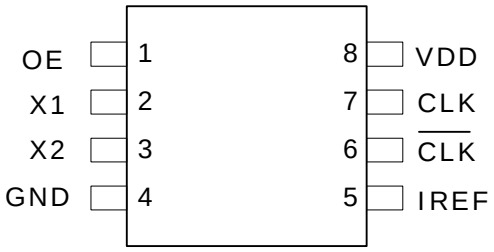
Features

- Supports PCI-Express™ HCSL Outputs 0.7 V current mode differential pair
- Supports LVDS Output Levels
- Packaged in 8-pin SOIC
- RoHS 5 (green) or RoHS 6 (green and lead free) compliant packaging
- Operating voltage of 3.3 V
- Low power consumption
- Input frequency of 25 MHz
- Short term jitter 100 ps (peak-to-peak)
- Output Enable via pin selection
- Industrial temperature range available
- **For PCIe Gen2 applications, see the 5V41064**
- **For PCIe Gen3 applications, see the 5V41234**

Block Diagram



Pin Assignment



8 Pin (150 mil) SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	OE	Input	Output Enable signal (H = outputs are enabled, L = outputs are disabled/tristated). Internal pull-up resistor.
2	X1	Input	Crystal or clock input. Connect to a 25 MHz crystal or single ended clock.
3	X2	XO	Crystal Connection. Connect to a parallel mode crystal. Leave floating if clock input.
4	GND	Power	Connect to ground.
5	IREF	Output	A 475Ω precision resistor connected between this pin and ground establishes the external reference current.
6	CLK	Output	HCSL differential complementary clock output.
7	CLK	Output	HCSL differential clock output.
8	VDD	Power	Connect to +3.3 V.

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 µF should be connected between VDD and the ground plane (pin 4) as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into IDT pin.

Crystal

A 25 MHz fundamental mode parallel resonant crystal with C_L = 16 pF should be used. This crystal must have less than 300 ppm of error across temperature in order for the ICS557-01 to meet PCI Express specifications.

Crystal Capacitors

Crystal capacitors are connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

C_L= Crystal's load capacitance in pF

Crystal Capacitors (pF) = (C_L- 8) * 2

For example, for a crystal with a 16 pF load cap, each external crystal cap would be 16 pF. (16-8)*2=16.

Current Source (Iref) Reference Resistor - R_R

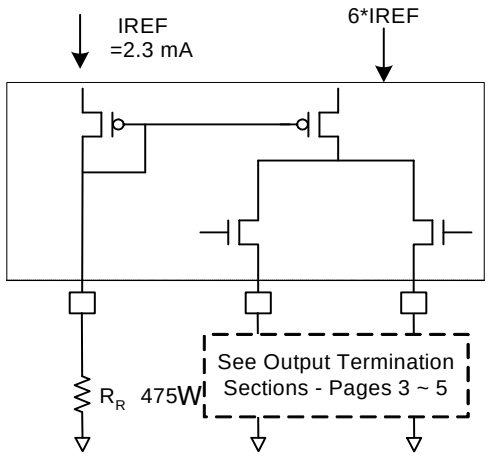
If board target trace impedance (Z) is 50Ω, then R_R = 475Ω (1%), providing IREF of 2.32 mA. The output current (I_{OH}) is equal to 6*IREF.

Output Termination

The PCI-Express differential clock outputs of the ICS557-01 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The ICS557-01can also be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section

Output Structures



General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.

2. No vias should be used between decoupling capacitor and VDD pin.

3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the ICS557-01.This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

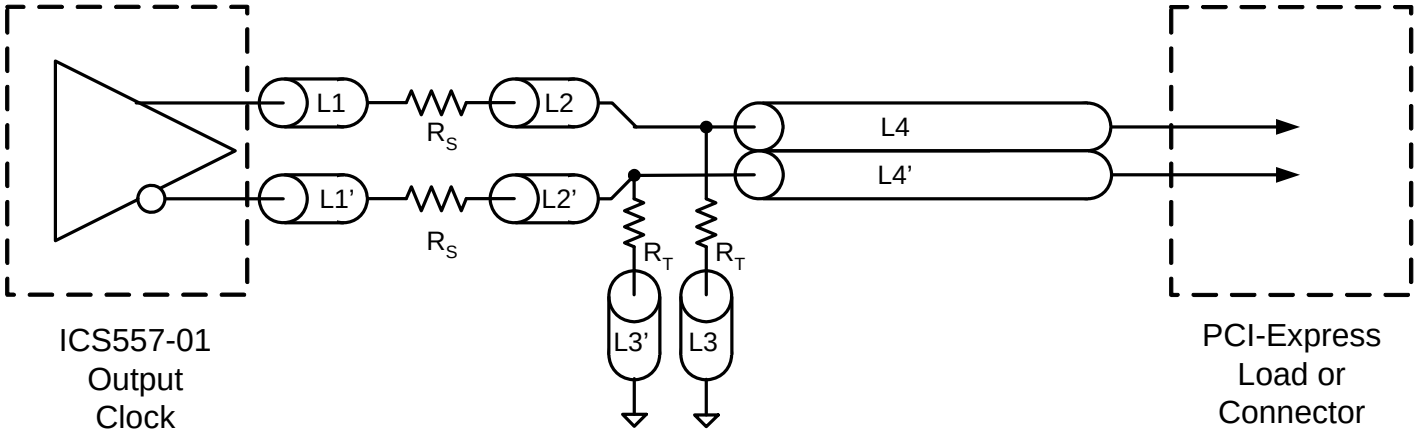
PCI-Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure	Notes
L1 length, Route as non-coupled 50 ohm trace.	0.5 max	inch	1,2	
L2 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	1,2	
L3 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	1,2	
R_S	33	ohm	1,2	
R_T	49.9	ohm	1,2	

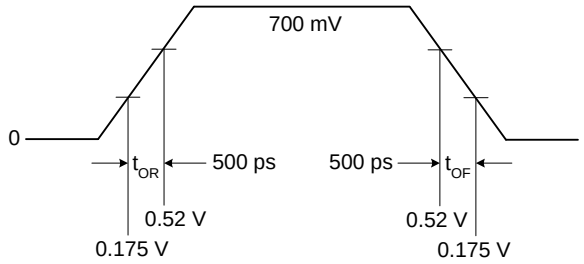
Differential Routing on a Single PCB	Dimension or Value	Unit	Figure	Notes
L4 length, Route as coupled **microstrip** 100 ohm differential trace.	2 min to 16 max	inch	1	
L4 length, Route as coupled **stripline** 100 ohm differential trace.	1.8 min to 14.4 max	inch	1	

Differential Routing to a PCI Express Connector	Dimension or Value	Unit	Figure	Notes
L4 length, Route as coupled **microstrip** 100 ohm differential trace.	0.25 to 14 max	inch	2	
L4 length, Route as coupled **stripline** 100 ohm differential trace.	0.225 min to 12.6 max	inch	2	

Figure 1: PCI-Express Device Routing



Typical PCI-Express (HCSL) Waveform

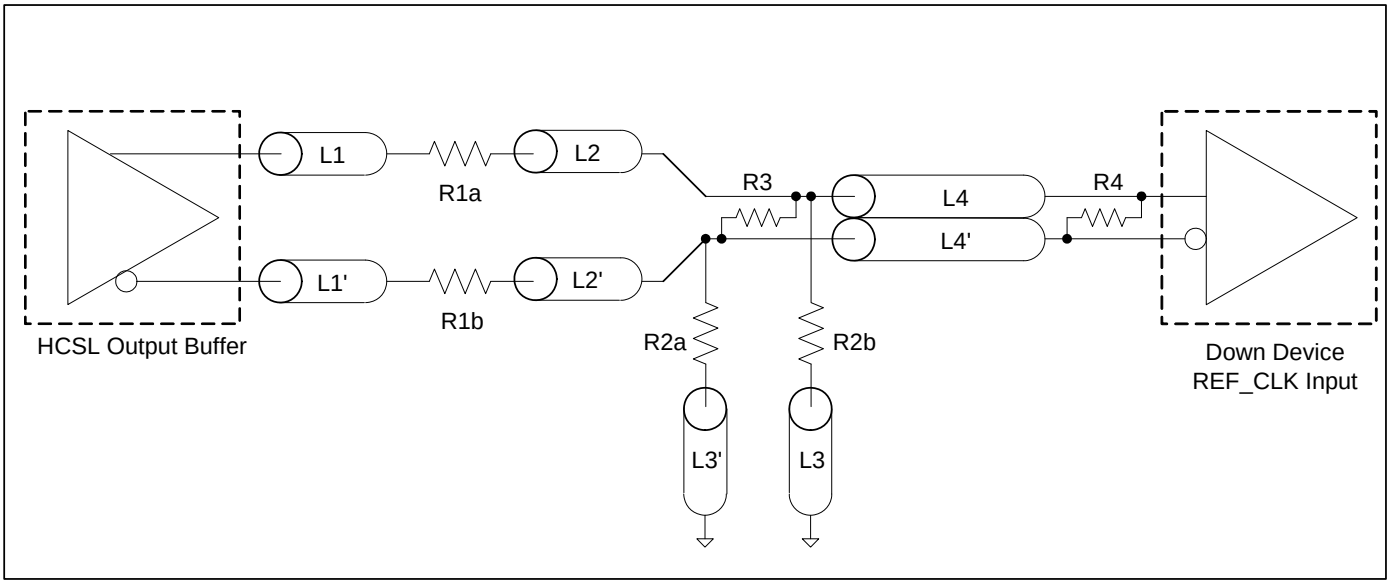


LVDS Compatible Layout Guidelines

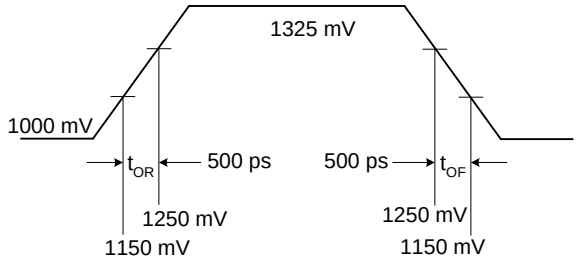
Alternative Termination for LVDS and other Common Differential Signals							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

R1a = R1b = R1
R2a = R2b = R2

Figure: LVDS Device Routing



Typical LVDS Waveform



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS557-01. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD, VDDA	5.5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70° C
Ambient Operating Temperature (industrial)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C
ESD Protection (Input)	2000 V min. (HBM)

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V		3.135		3.465	
Input High Voltage[1]	V_{IH}		2.0		VDD +0.3	V
Input Low Voltage[1]	V_{IL}		VSS-0.3		0.8	V
Input Leakage Current[2]	I_{IL}	0 < Vin < VDD	-5		5	µA
Operating Supply Current	I_{DD}	With 50Ω and 2 pF load			55	mA
	I_{DDOE}	OE =Low			35	mA
Input Capacitance	C_{IN}	Input pin capacitance			7	pF
Output Capacitance	C_{OUT}	Output pin capacitance			6	pF
Pin Inductance	L_{PIN}				5	nH
Output Resistance	Rout	CLK outputs	3.0			kΩ
Pull-up Resistor	R_{PUP}	OE		60		kΩ

1 Single edge is monotonic when transitioning through region.

2 Inputs with pull-ups/-downs are not included.

AC Electrical Characteristics - CLK/$\overline{CLK}$

Unless stated otherwise, **VDD=3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				25		MHz
Output Frequency				100		MHz
Output High Voltage[1,2]	V_{OH}		660	700	850	mV
Output Low Voltage[1,2]	V_{OL}		-150	0	27	mV
Crossing Point Voltage[1,2]		Absolute	250	350	550	mV
Crossing Point Voltage[1,2,4]		Variation over all edges			140	mV
Jitter, Cycle-to-Cycle[1,3]					80	ps
Rise Time[1,2]	t_{OR}	From 0.175 V to 0.525 V	175	332	700	ps
Fall Time[1,2]	t_{OF}	From 0.525 V to 0.175 V	175	344	700	ps
Rise/Fall Time Variation[1,2]					125	ps
Duty Cycle[1,3]			45		55	%
Output Enable Time[5]		All outputs		30		µs
Output Disable Time[5]		All outputs		30		µs
Stabilization Time	t_{STABLE}	From power-up VDD=3.3 V		3.0		ms

[1] Test setup is R_L=50 ohms with 2 pF, R_R = 475Ω (1%).

[2] Measurement taken from a single-ended waveform.

[3] Measurement taken from a differential waveform.

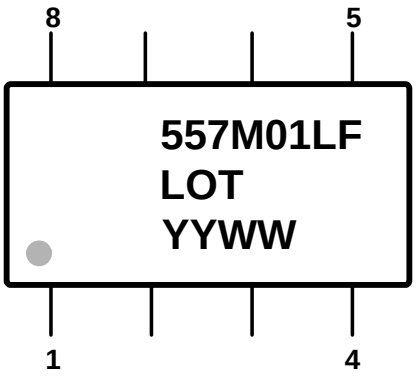
[4] Measured at the crossing point where instantaneous voltages of both CLKOUT and $\overline{CLKOUT}$ are equal.

[5] CLKOUT pins are tri-stated when OE is low asserted. CLKOUT is driven differential when OE is high.

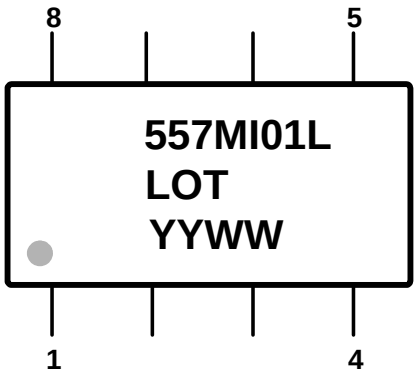
Thermal Characteristics (8-pin SOIC)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram (ICS557M-01LF)



Marking Diagram (ICS557MI-01LF)

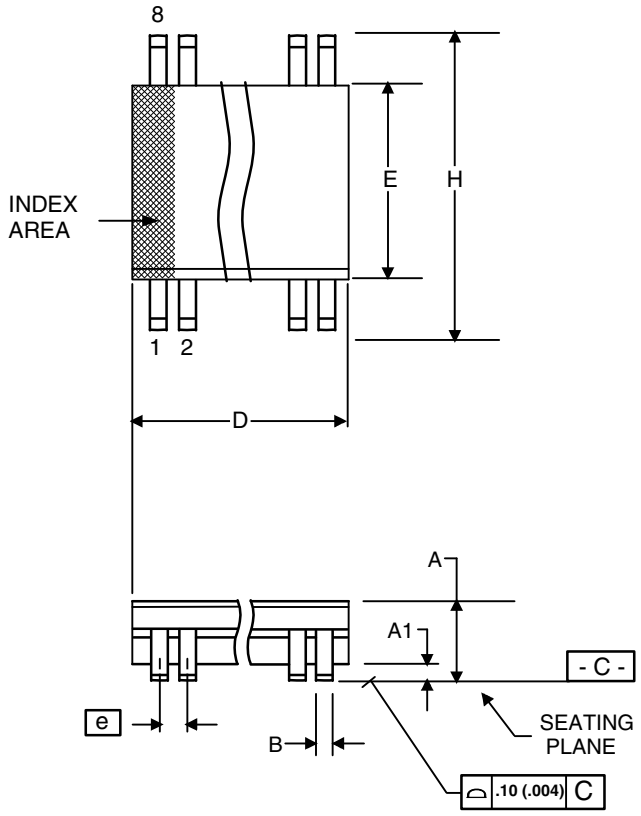


Notes:

1. “LOT” is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. “L” or “LF” designates Pb (lead) free packaging.
4. “I” denotes industrial temperature.
5. Bottom marking: (origin). Origin = country of origin if not USA.

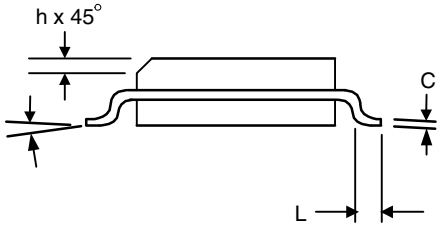
Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
a	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
557M-01LF	See Page 8	Tubes	8-pin SOIC	0 to +70° C
557M-01LFT		Tape and Reel	8-pin SOIC	0 to +70° C
557MI-01LF		Tubes	8-pin SOIC	-40 to +85° C
557MI-01LFT		Tape and Reel	8-pin SOIC	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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