

AN–1612 551012876 Universal Op Amp Evaluation Boards (SOP and MSOP)

1 Overview

The 551012876 universal evaluation board is designed to aid in the evaluation and testing of Texas Instruments low voltage/ low power and some precision operational amplifiers. These boards will accommodate op amps that are assembled in 8-pin SOP and MSOP and 10-pin MSOP.

This board is designed to evaluate one package at a time. Many different circuits can be made such as inverting, non-inverting, and differential-IN-differential-OUT amplifiers and low-pass, high-pass, band-pass, band-reject, or notch second-order filters. The amplifiers can be powered with single or dual supplies. These circuits can be configured without any modifications to the board; all that is necessary is to select the correct resistors and capacitors. The other optional components can be left open or shorted depending on the configuration desired.

This universal evaluation board is designed as a two-layer board; the top side is designed for op amps in 8-pin SOP and 8-pin MSOP as shown in [Figure 1](#).

The bottom side of this board is designed for op amps in the 10-pin MSOP as shown in [Figure 2](#). The board has been manufactured with vias connecting the equivalent pins of the top and bottom amplifiers. For example, Pin 1 of IC₁ on the top side is connected to Pin 1 of IC₁ on the bottom side. Similarly all other equivalent pins of the top and bottom amplifiers are connected. The 10-pin MSOP on the bottom side has connections for enabling and disabling the op amps. This printed circuit board (PCB) setup allows for an efficient use of one board to test amplifiers of different package types while keeping the same components on the board; just make sure that only one package is soldered to the same pads.

Circuit performance of this evaluation board will be comparable to final production designs. Use this evaluation board as a guide for general layout and a tool to aid in device testing and characterization.

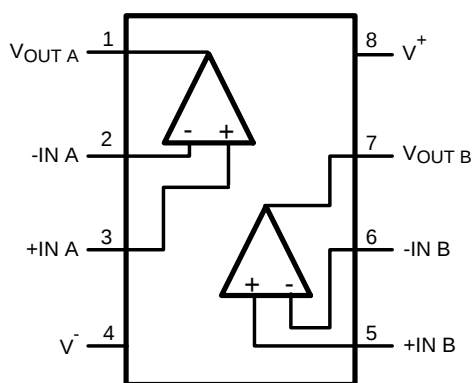


Figure 1. Connection Diagram for 8-Pin SOP and MSOP

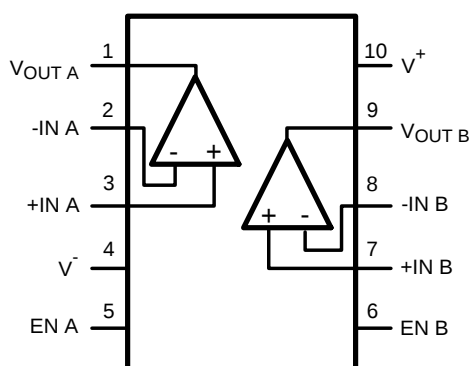


Figure 2. Connection Diagram for 10-Pin MSOP

2 Hardware Setup

2.1 Component Notation

The pins of the footprints for the 8-pin SOP and MSOP on the top side are connected and are also connected to the equivalent pins for the footprint of the 10-pin MSOP on the bottom side. Each of these packages contains two amplifiers, which will be referred to as Amp A and Amp B. The subscript of the PCB component refers to the specific amplifier; for example, R_{4A} is used for Amp A and R_{4B} for Amp B. In this document, components will be referred to, as an example, C_3 . If using Amp A this refers to component C_{3A} , if using Amp B this refers to component C_{3B} .

In some circuits, a resistor will be installed where the PCB is labeled for a capacitor or a capacitor will be installed where a resistor is labeled. For example, CR6 indicates that a capacitor should be in the R_6 position. R_{C5} means that a resistor will be installed in the C_5 position.

2.2 Power

Power is applied to the points labeled J4 for V^- , J6 for V^+ , and J7 for GND. If a single supply is used, then V^- should be connected to GND. A virtual ground, halfway between the positive supply voltage and ground, is the reference point for the input and output voltages. The output voltage swings above and below this virtual ground. Single-supply operation requires the generation of this virtual ground, usually at a voltage equal to $V^+/2$. The circuit in [Figure 3](#) can be used to generate $V^+/2$; R_1 and R_2 should be of equal values. This junction along with capacitor C_1 will form a low-pass filter used to eliminate conducted noise or transients on the positive supply rail.

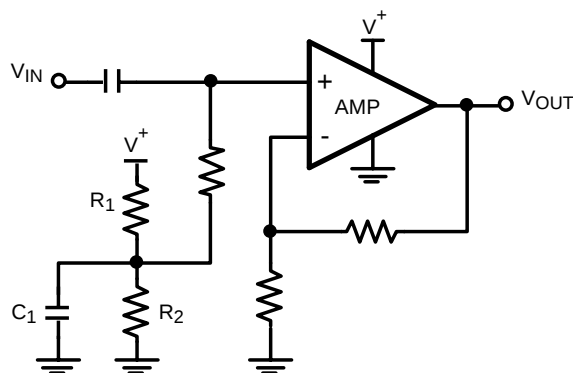


Figure 3. Single Supply Virtual Ground

2.3 Op Amp

Solder a dual op amp package to either the top IC₁ or the bottom IC₁ position. The package outline, showing pin 1, is on each side of the PCB.

2.4 Bypassing

Install the following capacitors:

C_{6A}, C_{9A}: 0.1 µF

C_{7A}, C_{8A}: 1 µF

2.5 Shutdown

To use the shutdown feature of the amplifier in the MSOP-10 package, install a resistor at R₁₅ and an optional capacitor at C₁₁. The shutdown voltage is applied at J3 or J5 depending on the amplifier being used.

2.6 Input and Output

SMA connectors are used for the input and output of signals. They are located on the edges of the PCB.

3 Circuit Configurations

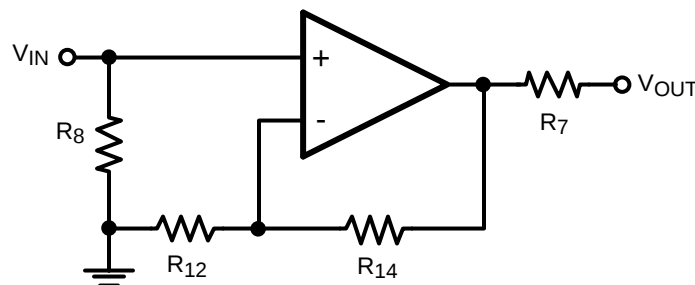
3.1 Non-Inverting Amplifier

Table 1. Non-Inverting Amplifier

C ₃	Short
R ₄	Short
R ₅	Short
R ₈	Input Termination
R ₇	Output series resistance (used for matching transmission lines or isolation)
R ₁₄	Gain Resistor
R ₁₂	Gain Resistor

Where,

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_{14}}{R_{12}} \quad (1)$$



C₃, R₄, R₅ = 0 (SHORT)

Figure 4. Non-Inverting Amplifier

3.2 Inverting Amplifier

Table 2. Inverting Amplifier

C ₃	Short
R ₉	Short
R ₁₃	Short
R ₈	Input Termination
R ₇	Output series resistance (used for matching transmission lines or isolation)
R ₁₄	Gain Resistor
R ₁₁	Gain Resistor

Where,

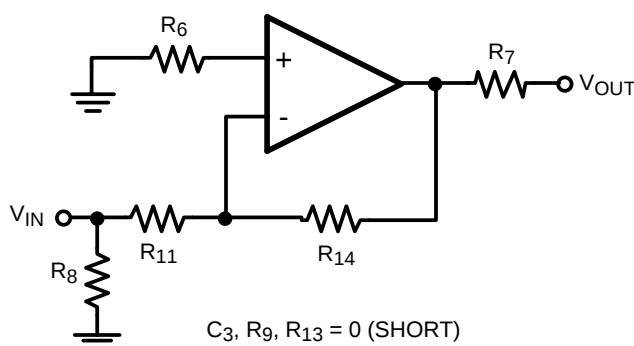
$$\frac{V_{OUT}}{V_{IN}} = - \frac{R_{14}}{R_{11}} \quad (2)$$

Input impedance: Set R_T to the desired input impedance. Calculate R₈ where,

$$R_8 = \frac{R_{11} \times R_T}{R_{11} - R_T} \quad (3)$$

To cancel the input bias current, set R₆ to the value calculated with the following formula:

$$R_6 = \frac{R_{11} \times R_{14}}{R_{11} - R_{14}} \quad (4)$$


Figure 5. Inverting Amplifier

3.3 Active Filter Applications

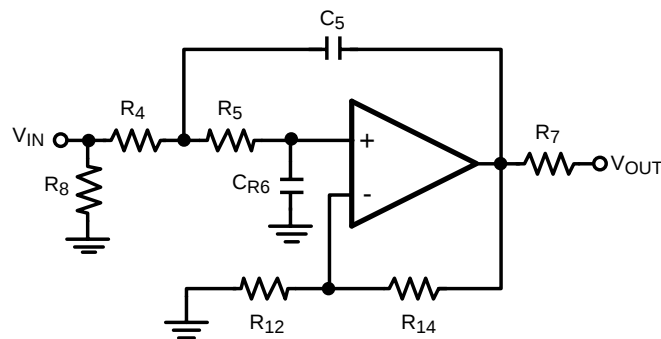
Both Sallen-Key and multiple feedback filters can be built on this PCB. To design a filter, use the WEBENCH tool at www.ti.com. Performance at high frequencies is limited to the gain bandwidth product of the amplifier, but within this frequency range, these active filters can achieve very good accuracy, if low-tolerance resistors and capacitor are used.

3.4 Sallen-Key Low-Pass Filter

Table 3 shows the instructions for configuring a Sallen-Key low-pass filter.

Table 3. Sallen-Key Low-Pass Filter

C_3	Short
R_{13}	Short
R_7	Output series resistance (used for matching transmission lines or isolation)
R_8	Input Termination
Set the following as determined using WEBENCH:	
$R_4, R_5, C_{R6}, R_{14}, R_{12}$	



$C_3, R_{13} = 0$ (SHORT)

Figure 6. Sallen-Key Low-Pass Filter

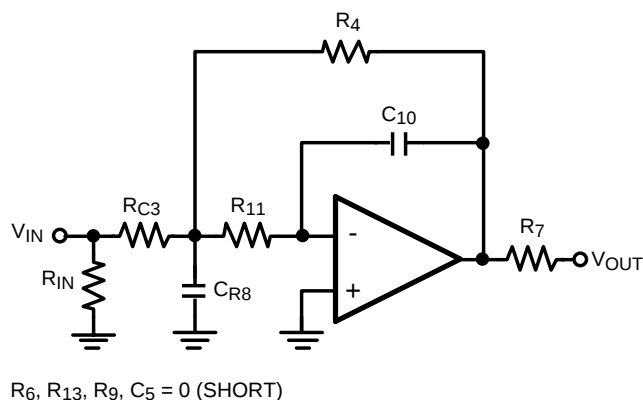
3.5 Multiple Feedback Low-Pass Filter

Table 4 shows the instructions for configuring a multiple feedback low-pass filter.

Table 4. Multiple Feedback Low-Pass Filter

R_6	Short
R_{13}	Short
R_9	Short
C_5	Short
R_7	Output series resistance (used for matching transmission lines or isolation)
Set the following as determined using WEBENCH:	
$R_{C3}, C_{R8}, R_4, R_{11}, C_{10}$	

Note: If needed, an input termination resistor will need to be soldered on to the SMA connector between the signal pin and the ground pin.

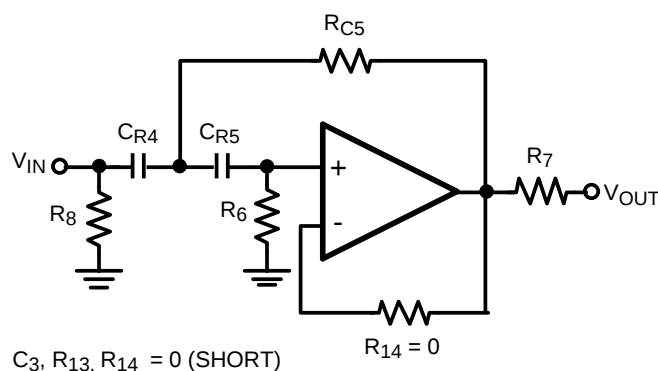

Figure 7. Multiple Feedback Low-Pass Filter

3.6 Sallen-Key High-Pass Filter

Table 5 shows the instructions for configuring a Sallen-Key high-pass filter.

Table 5. Sallen-Key High-Pass Filter

C_3	Short
R_{13}	Short
R_{14}	Short
R_7	Output series resistance (used for matching transmission lines or isolation)
R_8	Input Termination
Set as determined using WEBENCH:	
$C_{R4}, C_{R5}, R_{C5}, R_6$	


Figure 8. Sallen-Key High-Pass Filter

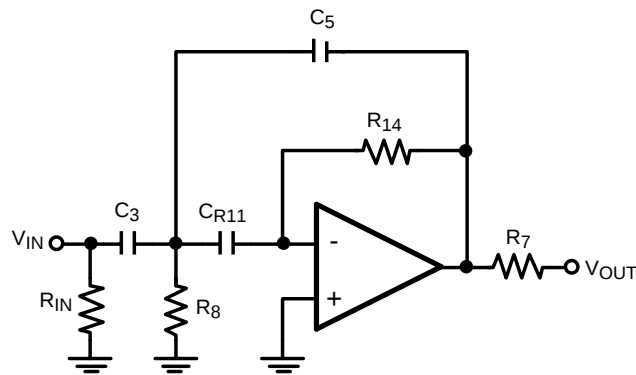
3.7 Multiple Feedback High-Pass Filter

Table 6 shows the instructions for configuring a multiple feedback high-pass filter.

Table 6. Multiple Feedback High-Pass Filter

R ₉	Short
R ₄	Short
R ₇	Output series resistance (used for matching transmission lines or isolation)
Set the following as determined using WEBENCH:	
C ₃ , R ₈ , C ₅ , C _{R11} , R ₁₄	

Note: If needed, an input termination resistor will need to be soldered on to the SMA connector between the signal pin and the ground pin.



R₉, R₄ = 0 (SHORT)

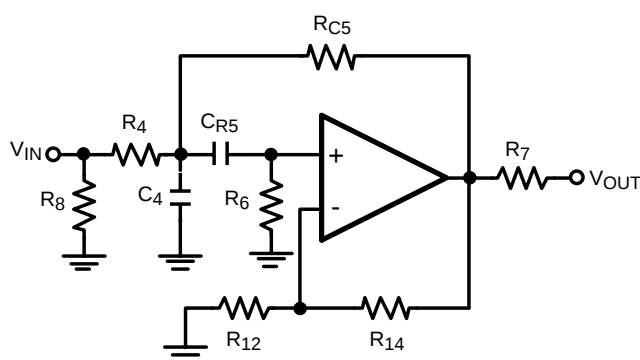
Figure 9. Multiple Feedback High-Pass Filter

3.8 Sallen-Key Band-Pass Filter

Table 7 shows the instructions for configuring a band-pass filter.

Table 7. Sallen-Key Band-Pass Filter

C ₃	Short
R ₁₃	Short
R ₇	Output series resistance (used for matching transmission lines or isolation)
R ₈	Input Termination
Set as determined using WEBENCH:	
R ₄ , C ₄ , C _{R5} , R ₆ , R _{C5} , R ₁₄ , R ₁₂	



$C_3, R_{13} = 0$ (SHORT)

Figure 10. Sallen-Key Band-Pass Filter

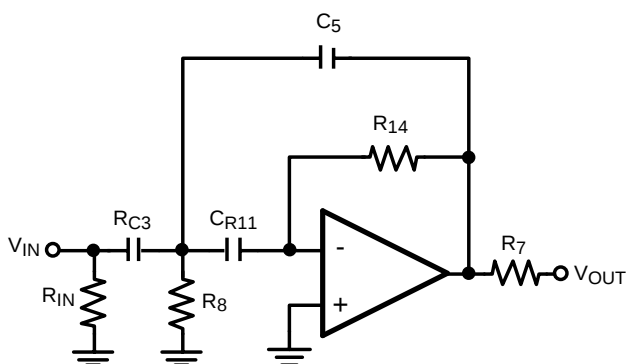
3.9 Multiple Feedback Band-Pass Filter

Table 8 shows the instructions for configuring a multiple feedback high-pass filter.

Table 8. Multiple Feedback Band-Pass Filter

R_6	Short
R_{13}	Short
R_9	Short
R_4	Short
R_7	Output series resistance (used for matching transmission lines or isolation)
Set the following as determined using WEBENCH:	
$R_{C3}, R_8, C_5, C_{R11}, R_{14}$	

Note: If needed, an input termination resistor will need to be soldered on to the SMA connector between the signal pin and the ground pin.



$R_6, R_{13}, R_9, R_4 = 0$ (SHORT)

Figure 11. Multiple Feedback Band-Pass Filter

4 Applications Using Two Amplifiers

4.1 Two-Amplifier Filters

Filters using two amplifiers can be built by connecting the output of Amp A to the input of Amp B.

4.2 Single Ended to Differential Conversion

The circuit in Figure 12 will convert a single ended signal to a differential signal. This is done by using the combination of an inverting amplifier and a non-inverting amplifier. Each amplifier generates output signals of equal magnitude but of opposite polarity. This topology is useful in applications where the signal source is single-ended, but the ADC requires a differential input. The board will need to be modified by connecting Input A to Input B with a jumper wire.

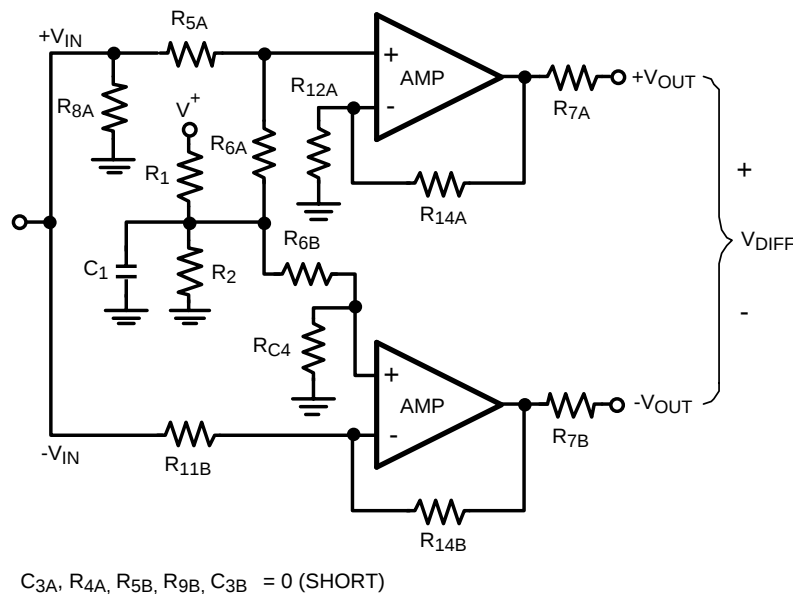


Figure 12. Single Ended to Differential Conversion

4.3 Differential Input, Differential Output, Non-Inverting

Combining two non-inverting amplifiers with a common feedback network, as shown in Figure 13, forms a non-inverting amplifier with a differential input and a differential output. Through the inherent cancellation of the two op amp common-mode error signals this configuration fully exploits the noise reduction benefits of CMRR. In addition the output voltage swing is doubled and depending on the op amp used, the bandwidth and slew rate may also be increased, while maintaining the original gain bandwidth specification.

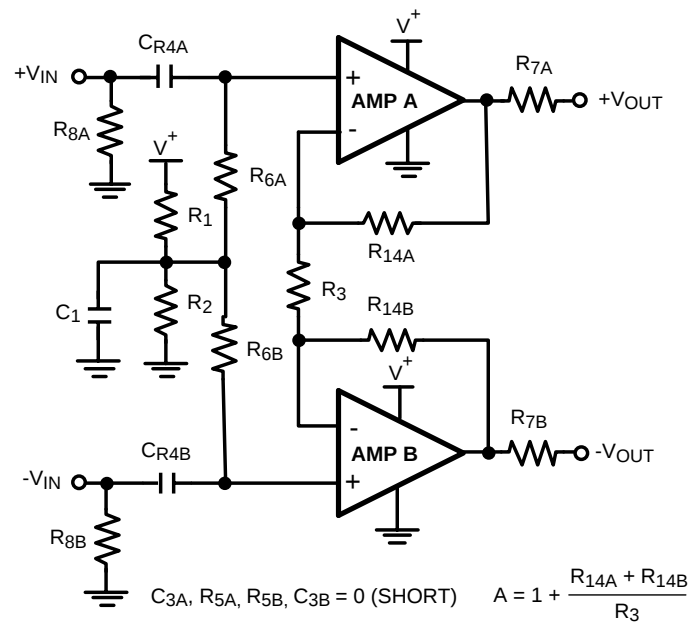


Figure 13. Differential Input, Differential Output, Non-Inverting

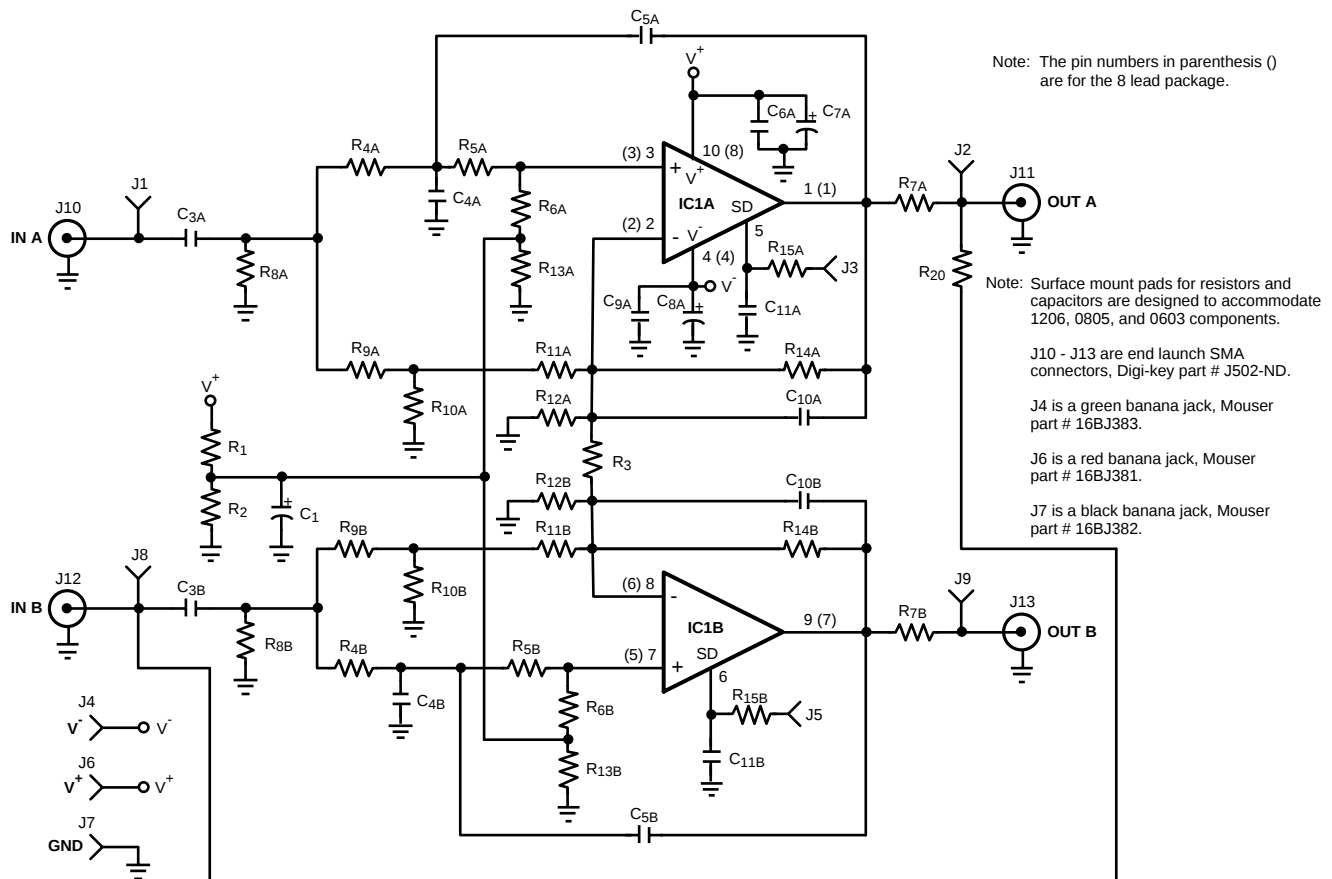


Figure 14. 551012876 Schematic

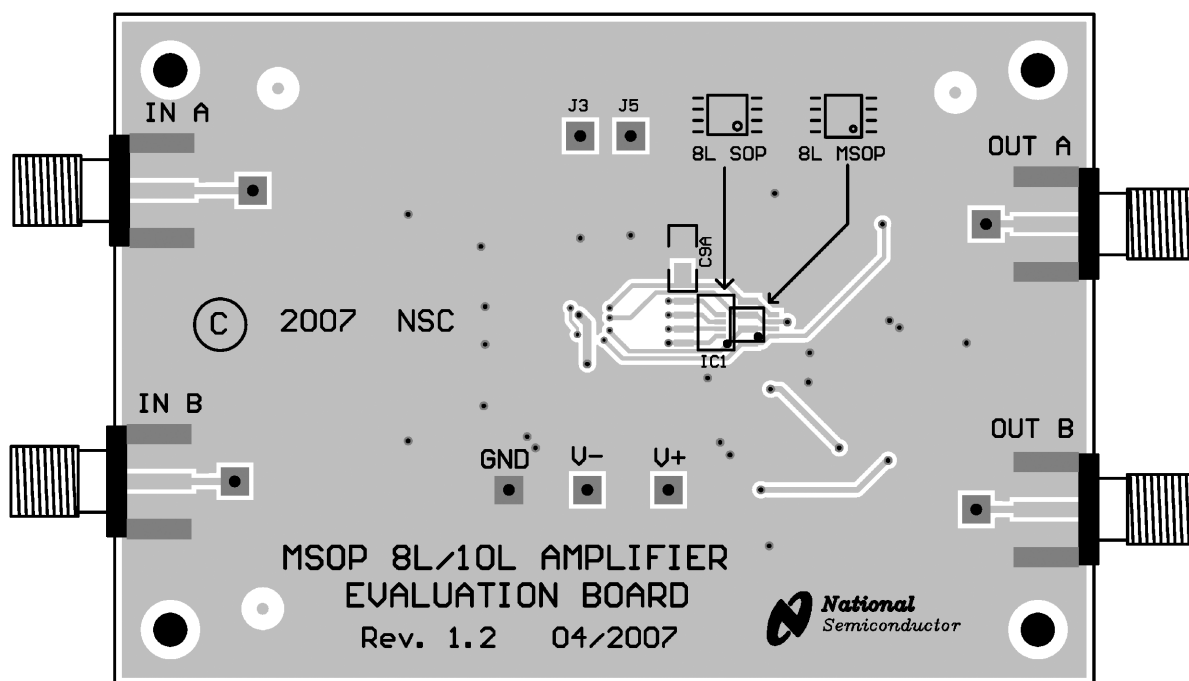


Figure 15. 551012876 Top Layout

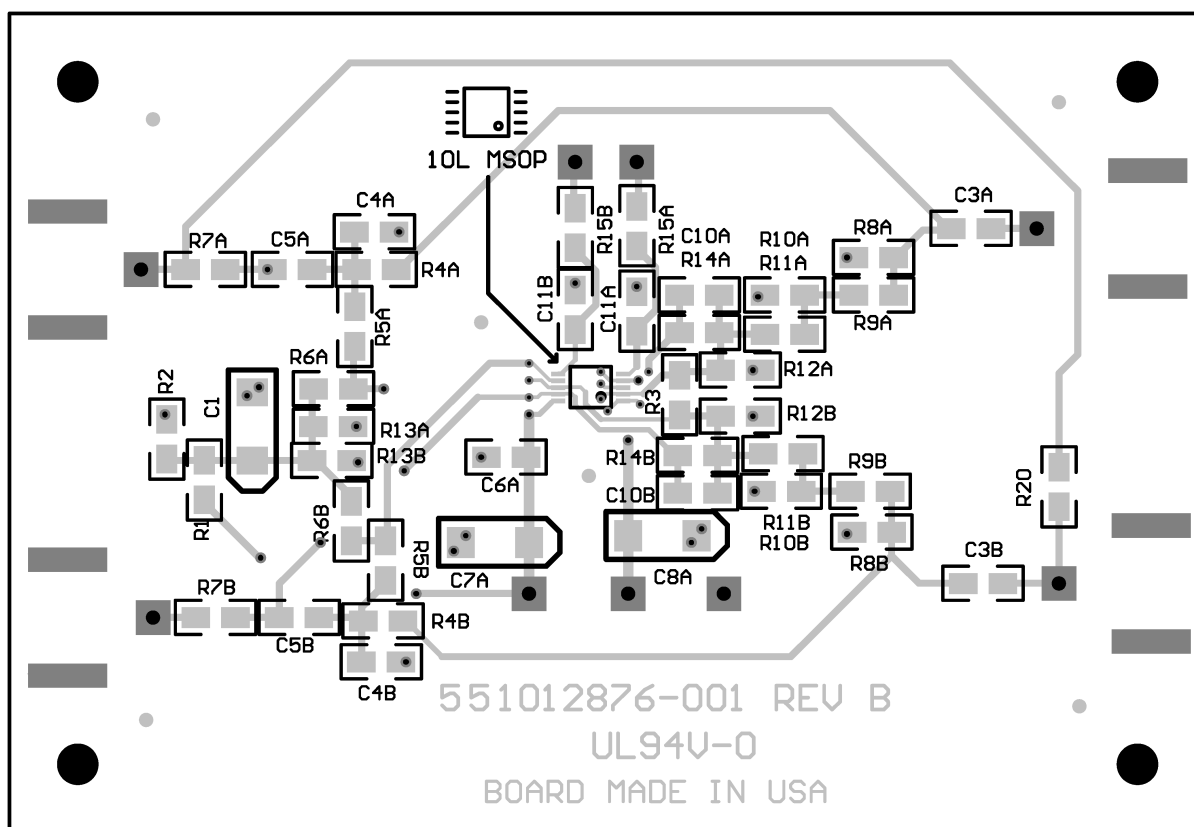


Figure 16. 551012876 Bottom Layout

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