National Semiconductor

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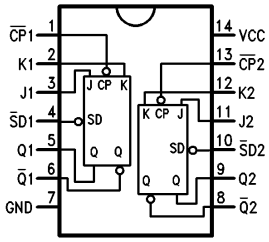
54LS113
Dual JK Edge-Triggered Flip-Flop

General Description

The 54LS113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

Connection Diagram

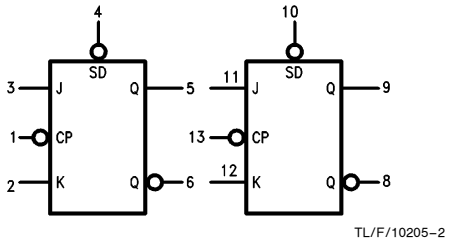
Dual-In-Line Package



TL/F/10205–1

Order Number 54LS113DMQB, 54LS113FMQB or 54LS113LMQB
See NS Package Number E20A, J14A or W14B

Logic Symbol



TL/F/10205–2

V_{CC} = Pin 14
GND = Pin 7

Truth Table

Inputs		Output
@ t_n		@ $t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

t_n = Bit Time before Clock Pulse
$t_n + 1$ = Bit Time after Clock Pulse
H = HIGH Voltage Level
L = LOW Voltage Level

Asynchronous Input:
Low input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

Pin Names	Description
J1, J2, K1, K2	Data Inputs
$\overline{CP}$1, $\overline{CP}$2	Clock Pulse Inputs (Active Falling Edge)
$\overline{SD}$1, $\overline{SD}$2	Direct Set Inputs (Active LOW)
Q1, Q2, $\overline{Q}$1, $\overline{Q}$2	Outputs

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS113			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			4	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}_n$	20 20			ns
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}_n$	0 0			ns
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	20 15			ns
t_w (L)	$\overline{S}_{Dn}$ Pulse Width LOW	15			ns

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V	J, K			0.1	mA
			SD			0.3	
			CP			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			SD			60	
			CP			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	J, K	−30		−400	μA
			CP, SD	−60		−800	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

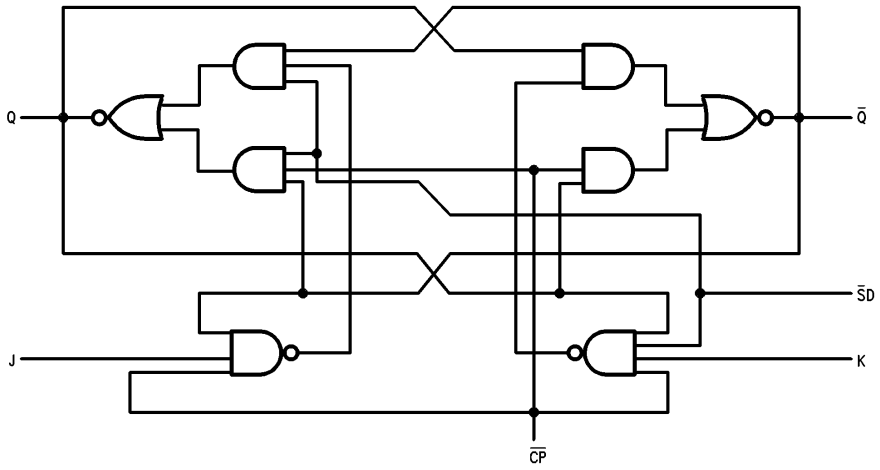
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

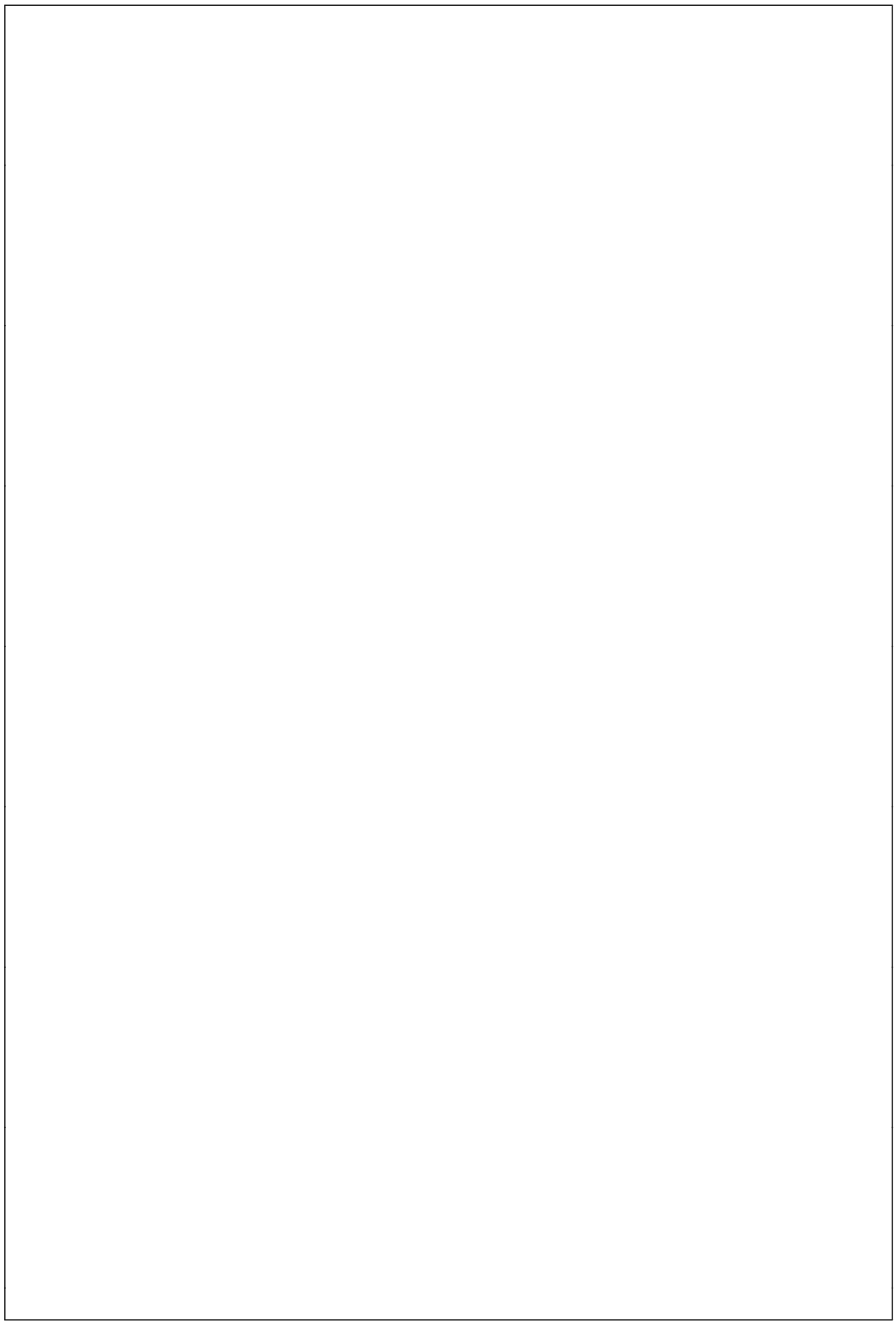
Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	54LS113 $C_L = 15$ pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		16 24	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		16 24	ns

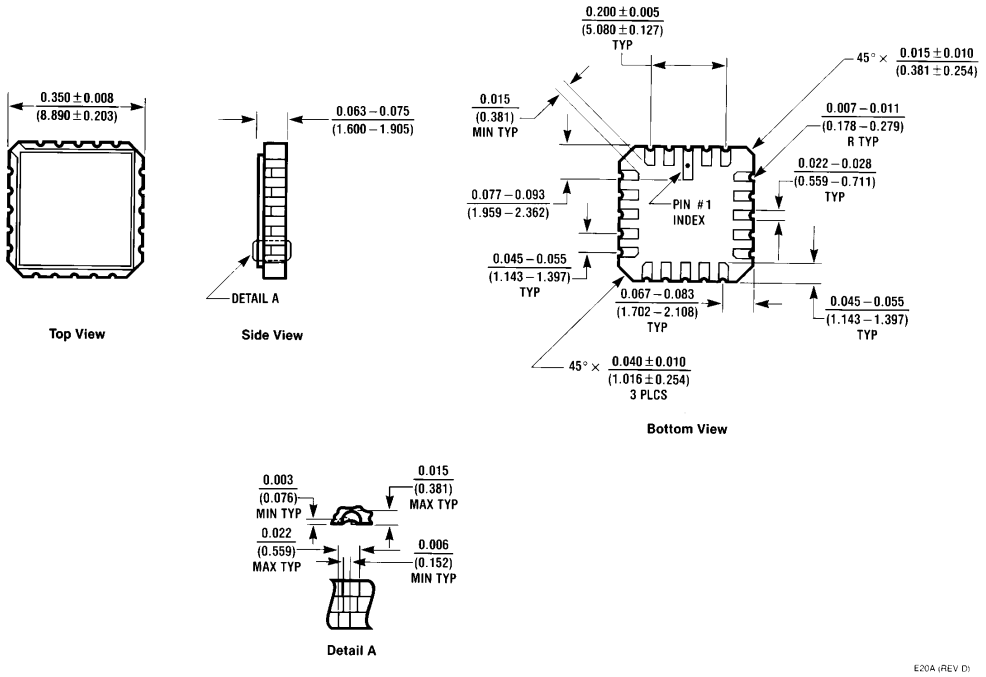
Logic Diagram (one half shown)



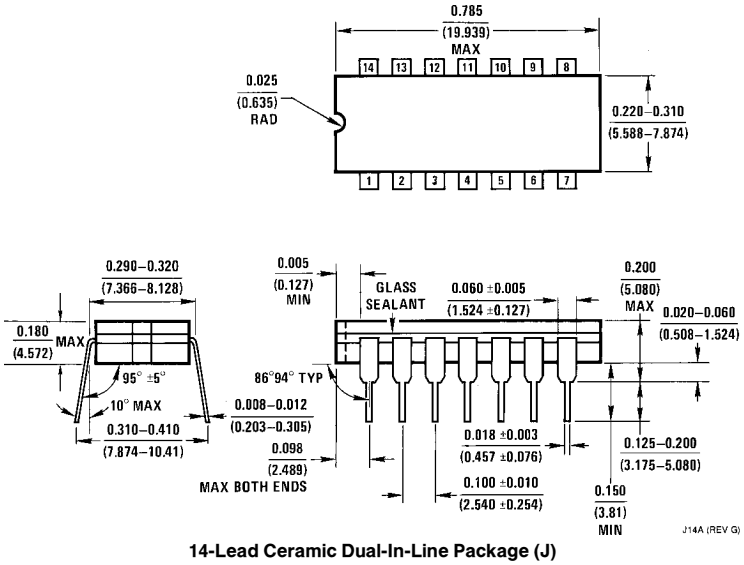
TL/F/10205–3



Physical Dimensions inches (millimeters)

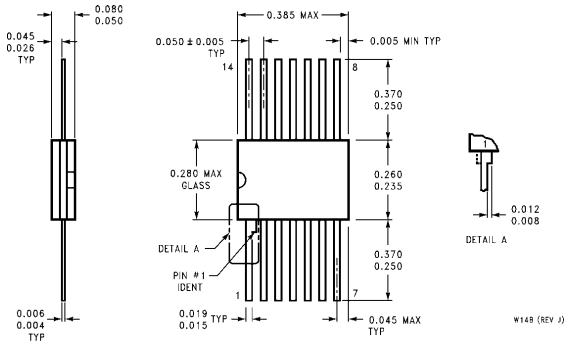


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS113LMQB
NS Package Number E20A



14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS113DMQB
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS113FMQB
NS Package Number W14B

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