54AC253,54ACT253

54AC253 54ACT253 Dual 4-Input Multiplexer with TRI-STATE Outputs



Literature Number: SNOS101

National Semiconductor

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54AC253 • 54ACT253
Dual 4-Input Multiplexer with TRI-STATE® Outputs

General Description

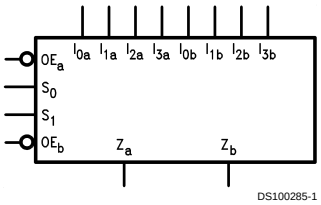
The 'AC/'ACT253 is a dual 4-input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

- Multifunction capability
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT253 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC253: 5962-87693
  - — 'ACT253: 5962-87761

Features

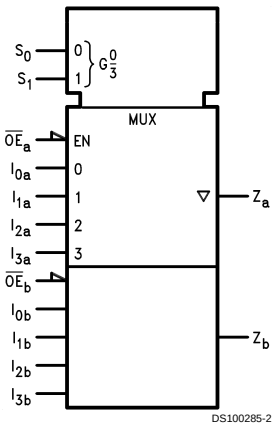
- I_{CC} and I_{OZ} reduced by 50%

Logic Diagrams



DS100285-1

IEEE/IEC



DS100285-2

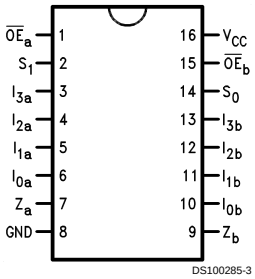
Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	TRI-STATE Outputs

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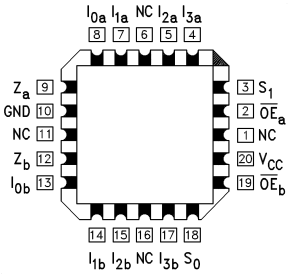
Connection Diagrams

Pin Assignment for DIP and Flatpak



DS100285-3

Pin Assignment for LCC



DS100285-4

Functional Description

The 'AC/'ACT253 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 +$
$I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$

$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 +$
$I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$

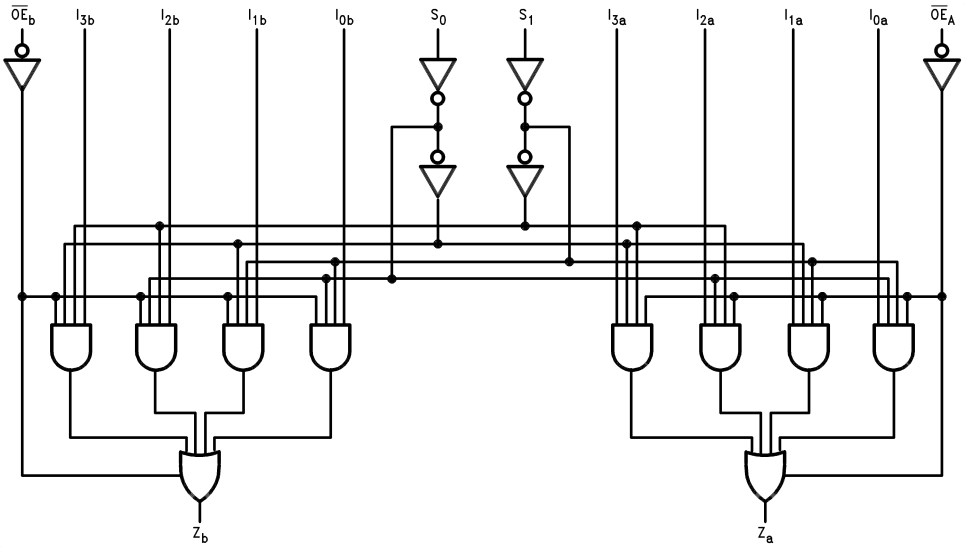
If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



DS100285-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55˚C to +125˚C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 μA
		4.5	4.4		
		5.5	5.4		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4	V	I_{OH} = −12 mA
		4.5	3.7		I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 μA
		4.5	0.1		
		5.5	0.1		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50	V	I_{OL} = 12 mA
		4.5	0.50		I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
	(Note 3)				
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	80.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level	4.5	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level	4.5	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5	4.4	V	I_{OUT} = −50 µA
	Output Voltage	5.5	5.4		
					(Note 5)
					V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level	4.5	0.1	V	I_{OUT} = 50 µA
	Output Voltage	5.5	0.1		
					(Note 5)
					V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input	5.5	±1.0	µA	V_I = V_{CC}, GND
	Leakage Current				
I_{OZ}	Maximum TRI-STATE	5.5	±5.0	µA	V_I = V_{IL}, V_{IH}
	Current				V_O = V_{CC}, GND
I_{CCT}	Maximum	5.5	1.6	mA	V_I = V_{CC} − 2.1V
	I_{CC}/Input				
	(Note 6)				
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent	5.5	80.0	µA	V_{IN} = V_{CC}
	Supply Current				or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Note 7: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 8)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3	1.0	18.0	ns	
		5.0	1.0	12.5		
t_{PHL}	Propagation Delay S_n to Z_n	3.3	1.0	18.5	ns	
		5.0	1.0	13.5		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.0	17.0	ns	
		5.0	1.0	11.5		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.0	15.0	ns	
		5.0	1.0	11.5		
t_{PZH}	Output Enable Time	3.3	1.0	9.0	ns	
		5.0	1.0	7.0		
t_{PZL}	Output Enable Time	3.3	1.0	9.5	ns	
		5.0	1.0	8.0		
t_{PHZ}	Output Disable Time	3.3	1.0	10.5	ns	
		5.0	1.0	9.0		
t_{PLZ}	Output Disable Time	3.3	1.0	9.5	ns	
		5.0	1.0	8.0		

Note 8: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

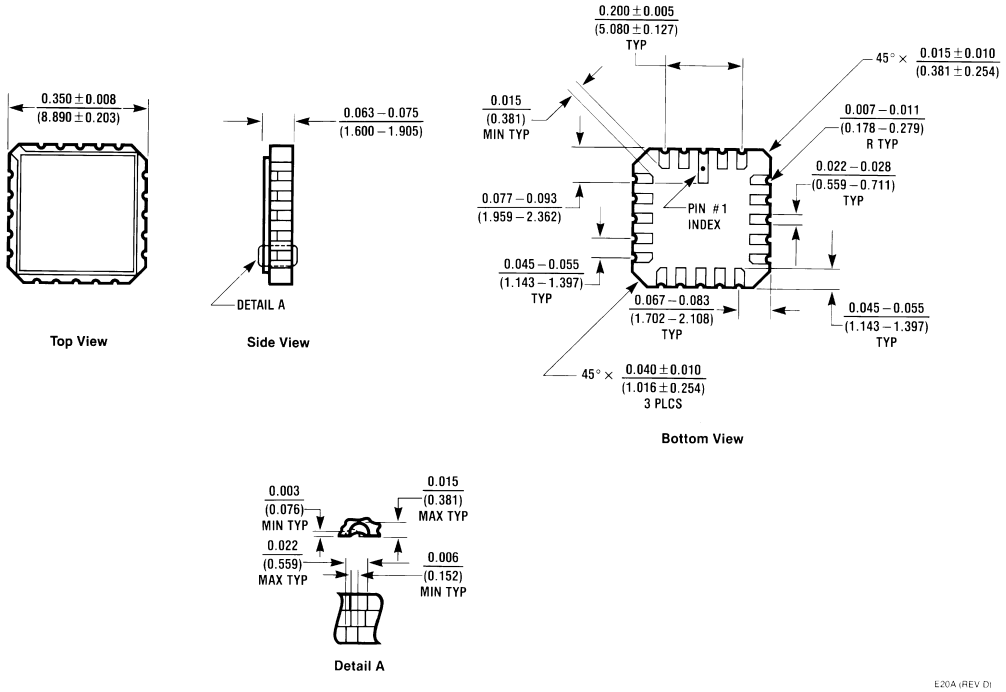
Symbol	Parameter	V_{CC} (V) (Note 9)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	1.0	14.5	ns	
t_{PHL}	Propagation Delay S_n to Z_n	5.0	1.0	16.0	ns	
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	12.0	ns	
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	13.5	ns	
t_{PZH}	Output Enable Time	5.0	1.0	9.5	ns	
t_{PZL}	Output Enable Time	5.0	1.0	9.5	ns	
t_{PHZ}	Output Disable Time	5.0	1.0	11.0	ns	
t_{PLZ}	Output Disable Time	5.0	1.0	9.0	ns	

Note 9: Voltage Range 5.0 is 5.0V ±0.5V

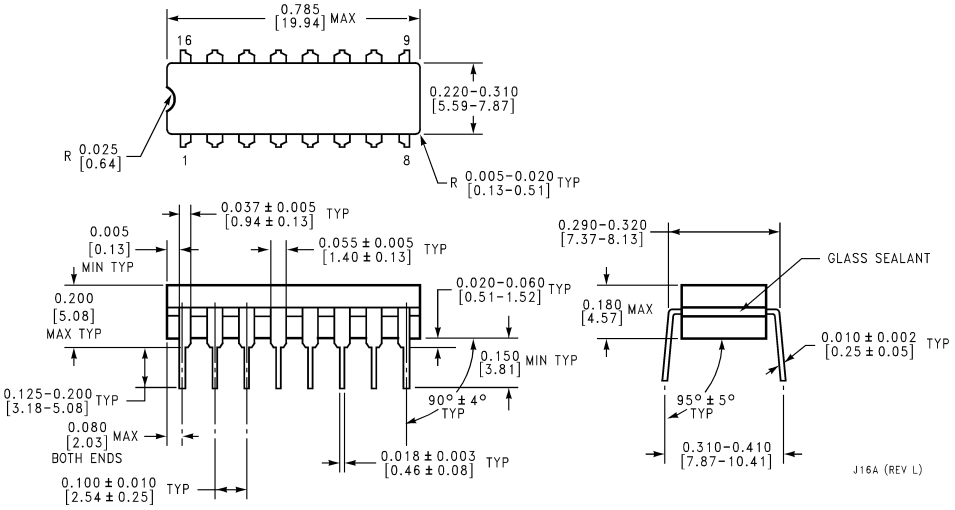
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

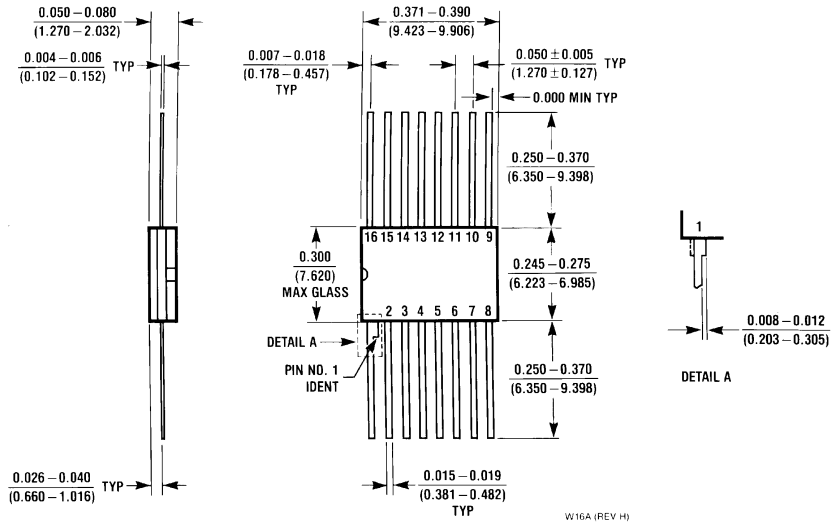


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16 Lead Ceramic Flatpak (F)
NS Package Number W16A

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