4AM13

Silicon N-Channel/P-Channel Power MOS FET Array

HITACHI

Application

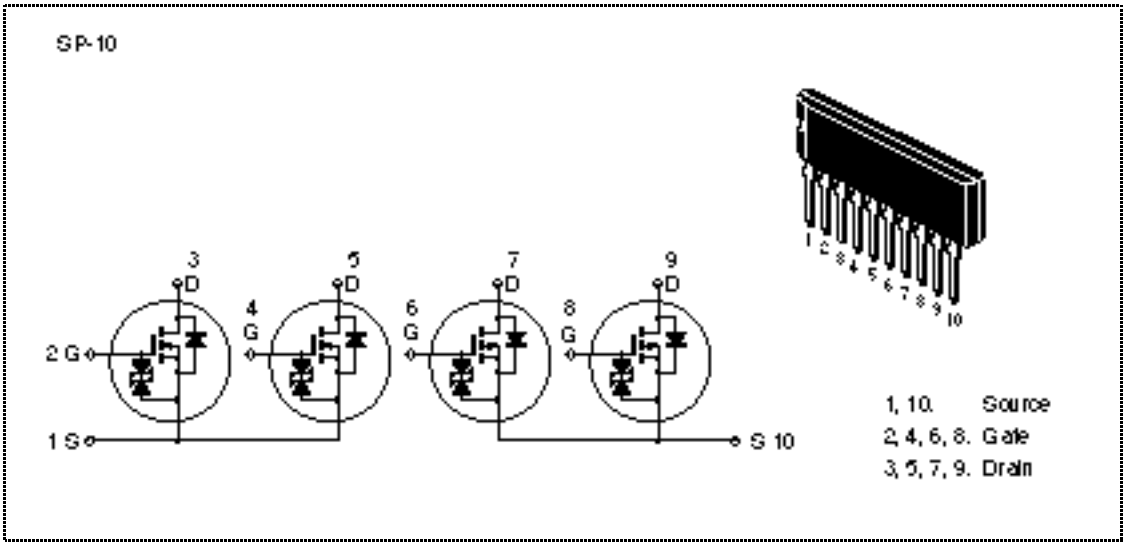
High speed power switching

Features

- Low on-resistance
  N-channel: $R_{DS(on)} \leq 0.4\ \Omega$, $V_{GS} = 10$ V, $I_D = 1.5$ A
  P-channel: $R_{DS(on)} \leq 0.45\ \Omega$, $V_{GS} = -10$ V, $I_D = -1.5$ A
- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

Hitachi semiconductor

Outline



Absolute Maximum Ratings (Ta = 25°C) (1 Unit)

Item	Symbol	Rating Nch	Rating Pch	Unit
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	3	–3	A
Drain peak current	$I_{D(pulse)}$*1	12	–12	A
Body to drain diode reverse drain current	I_{DR}	3	–3	A
Channel dissipation	Pch (Tc = 25°C)*2	28		W
Channel dissipation	Pch*2	4		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

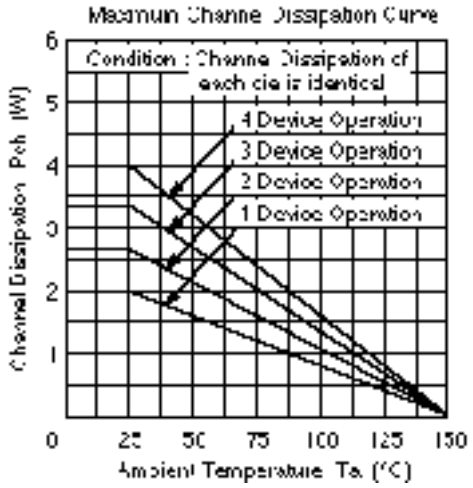
Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. 4 Devices operation

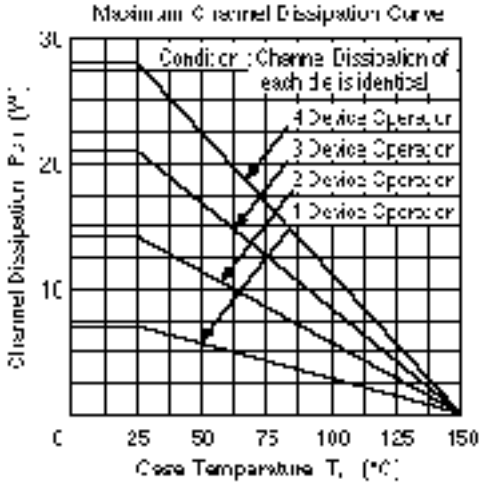
Electrical Characteristics (Ta = 25°C) (1 Unit)

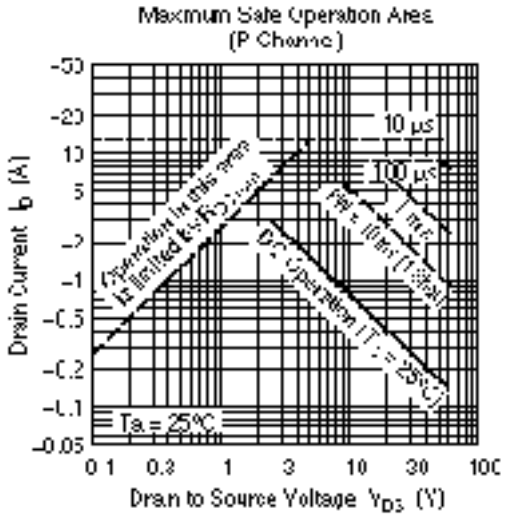
		N channel			P channel				
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test conditions**
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	–60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	—	—	–250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	–1.0	—	–2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.25	0.35	—	0.28	0.4	Ω	I_D = 1.5 A, V_{GS} = 10 V*[1]
		—	0.35	0.5	—	0.4	0.55	Ω	I_D = 1.5 A, V_{GS} = 4 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	1.5	2.5	—	1.5	2.5	—	S	I_D = 1.5 A, V_{DS} = 10 V*[1]
Input capacitance	Ciss	—	240	—	—	400	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	115	—	—	240	—	pF	
Reverse transfer capacitance	Crss	—	35	—	—	70	—	pF	
Turn-on delay time	$t_{d(on)}$	—	4	—	—	5	—	ns	I_D = 1.5 A, V_{GS} = 10 V, R_L = 20 Ω
Rise time	t_r	—	20	—	—	25	—	ns	
Turn-off delay time	$t_{d(off)}$	—	80	—	—	180	—	ns	
Fall time	t_f	—	40	—	—	80	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	—	–1.1	—	V	I_F = 3 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	75	—	—	140	—	ns	I_F = 3 A, V_{GS} = 0, dIF/dt = 50 A/µs

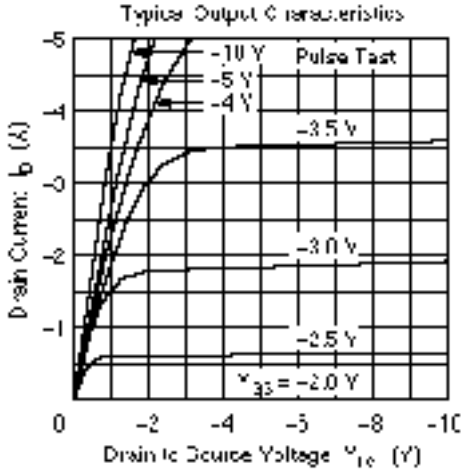
Note: 1. Pulse Test

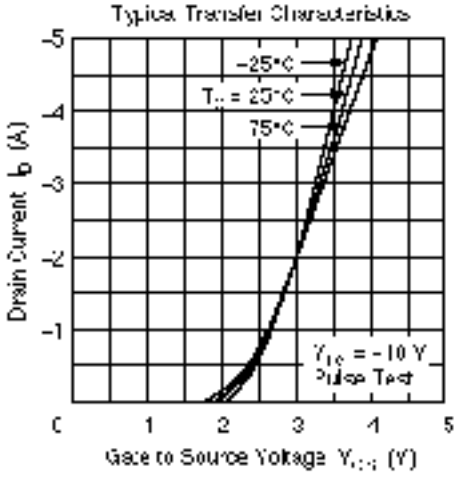
Polarity of test conditions for P channel device is reversed.

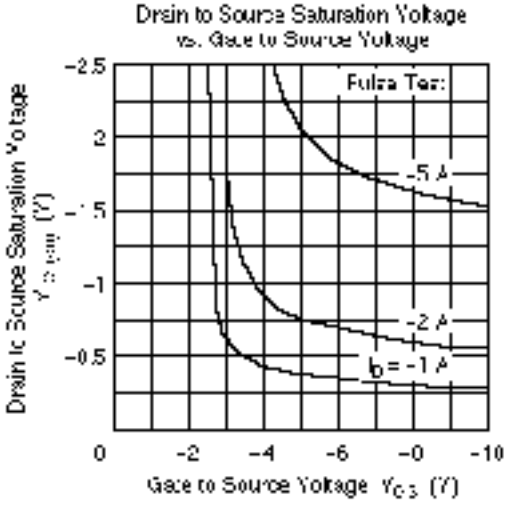

Maximum Channel Dissipation Curve
Condition : Channel Dissipation of each die is identical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
0
1
2
3
4
5
6
25
50
75
100
125
150
Ambient Temperature Ta (°C)

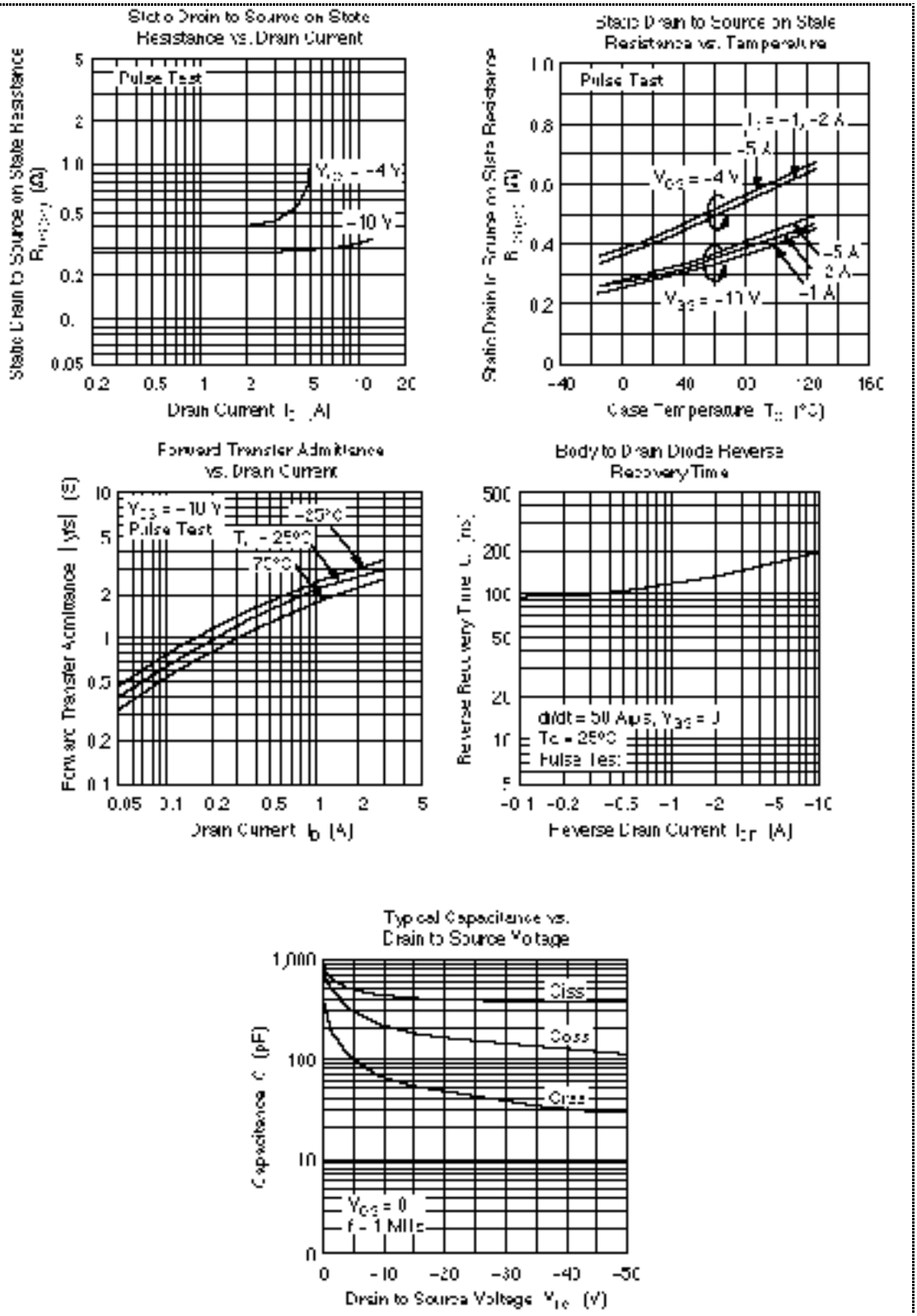

Maximum Channel Dissipation Curve
Condition : Channel Dissipation of each die is identical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation
30
20
10
0
25
50
75
100
125
150
Case Temperature T_c (°C)

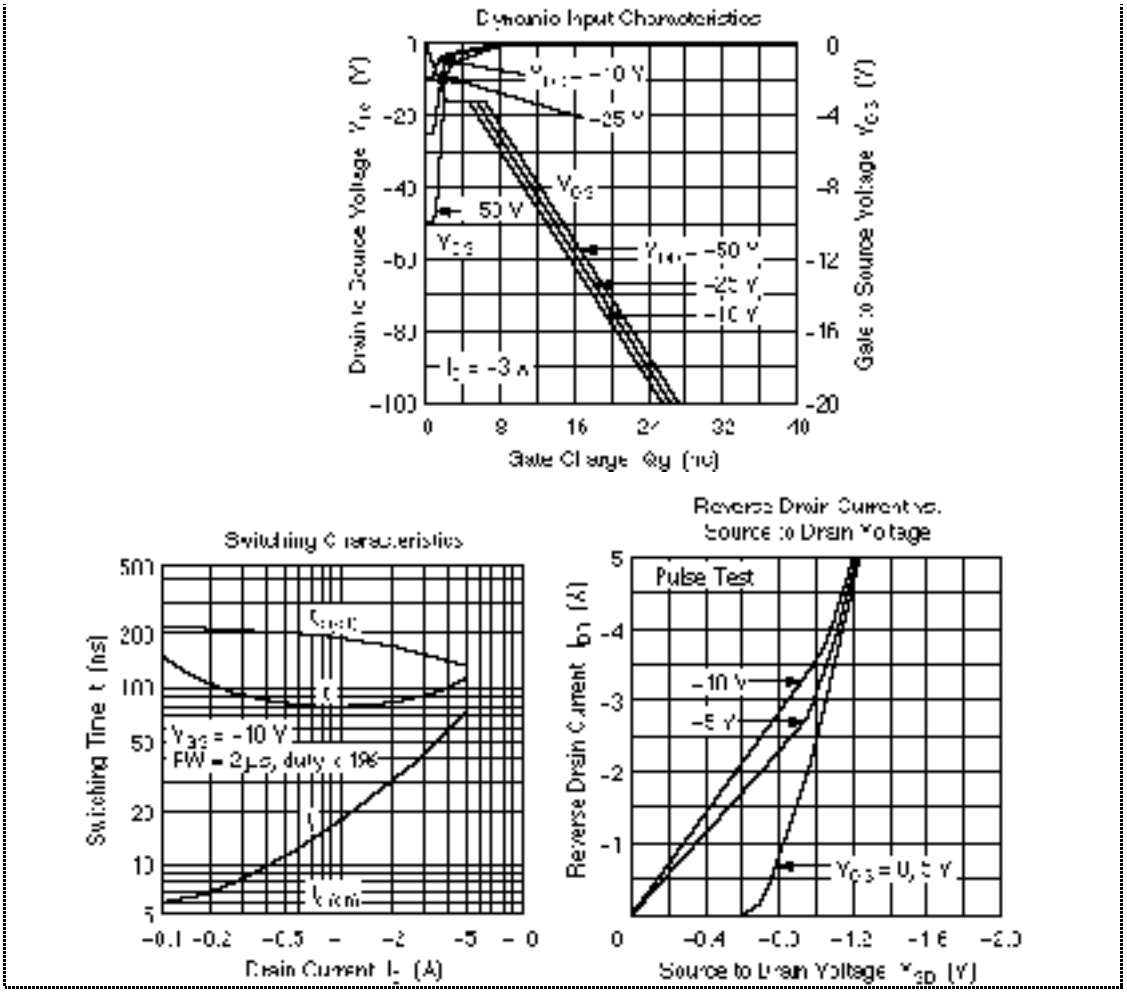

Maximum Safe Operation Area
(P Channel)
Drain Current I_D (A)
10 µs
100 µs
1 ms
PW = 10 ms (1 shot)
DC Operation (T_c = 25°C)
Operation in this area is limited by $R_{DS(on)}$
Ta = 25°C
Drain to Source Voltage V_{DS} (V)

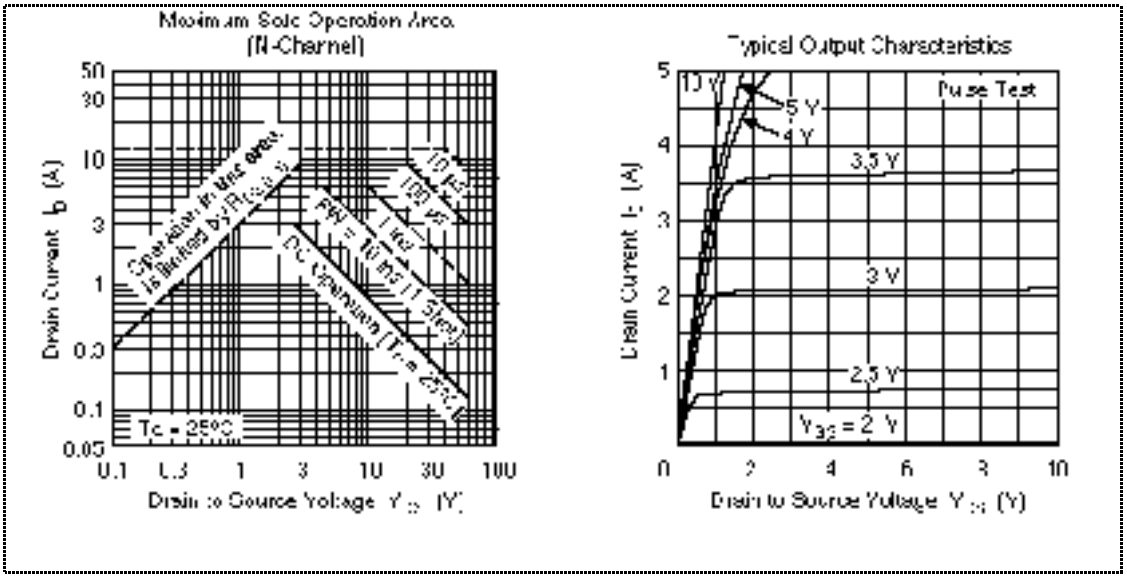

Typical Output Characteristics
Drain Current I_D (A)
-10 V
-5 V
-4 V
Pulse Test
-3.5 V
-3.0 V
-2.5 V
V_{GS} = -2.0 V
Drain to Source Voltage V_{DS} (V)

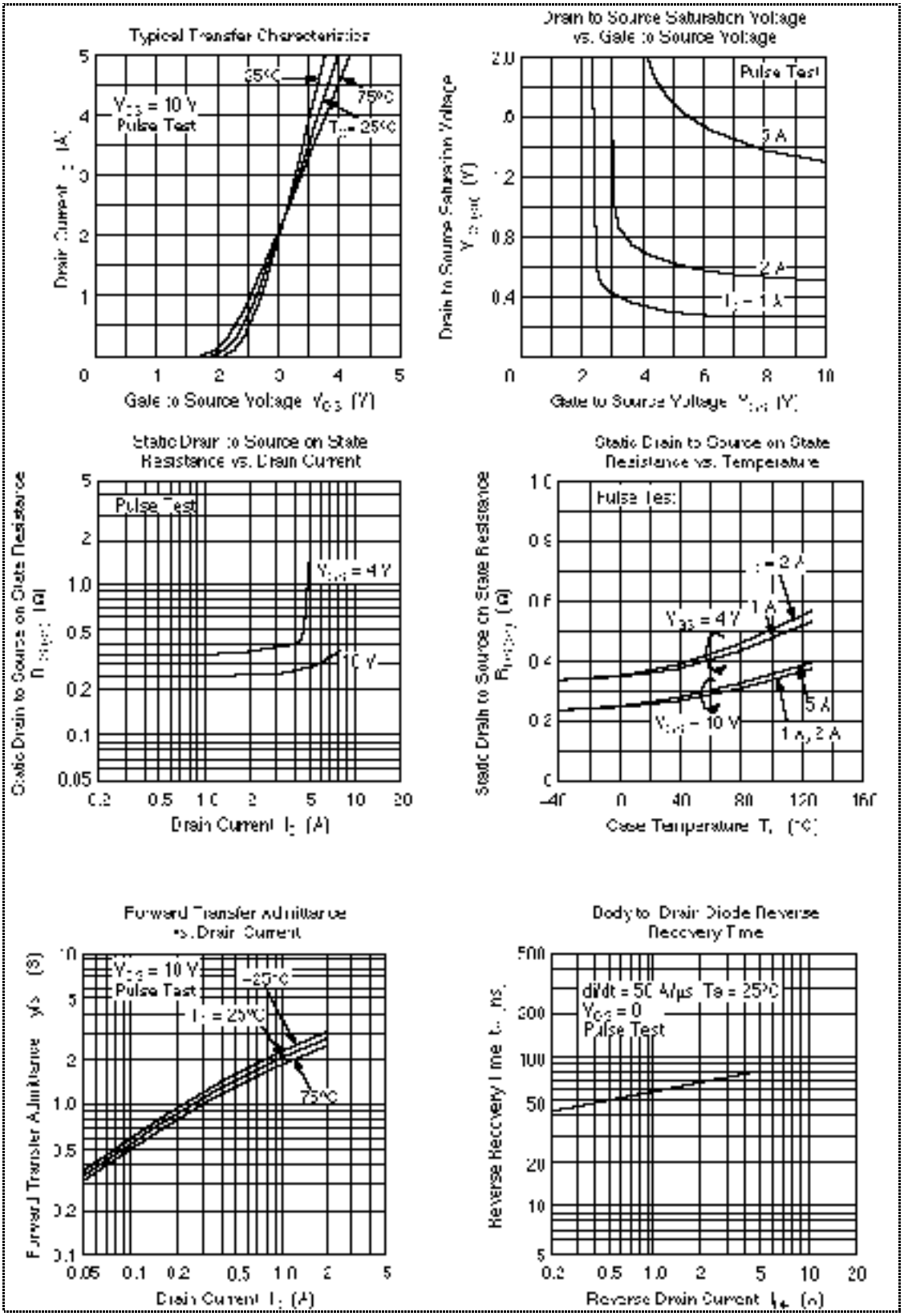

Typical Transfer Characteristics
Drain Current I_D (A)
-25°C
T_c = 25°C
75°C
V_{DS} = -10 V
Pulse Test
Gate to Source Voltage V_{GS} (V)


Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Drain to Source Saturation Voltage
Pulse Test
-5 A
-2 A
I_D = -1 A
Gate to Source Voltage V_{GS} (V)


Static Drain to Source on State Resistance vs. Drain Current
Pulse Test
Drain Current
Static Drain to Source on State Resistance vs. Temperature
Pulse Test
Case Temperature
Forward Transfer Admittance vs. Drain Current
Pulse Test
Drain Current
Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/µs
Tc = 25°C
Pulse Test
Reverse Drain Current
Typical Capacitance vs. Drain to Source Voltage
Ciss
Coss
Crss
f = 1 MHz
Drain to Source Voltage


Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
Gate Charge Q_g (nc)
V_{DD} = −10 V
−25 V
−50 V
I_D = −3 A
Switching Characteristics
Switching Time t (ns)
Drain Current I_D (A)
V_{GS} = −10 V
PW = 2 µs, duty < 1%
Reverse Drain Current vs. Source to Drain Voltage
Pulse Test
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
−10 V
−5 V
V_{GS} = 0, 5 V


Maximum Safe Operation Area (N-Channel)
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
Operation in this area is limited by $R_{DS(on)}$
100 µs
1 ms
PW = 10 ms (1 Shot)
DC Operation (Tc = 25°C)
Tc = 25°C
Typical Output Characteristics
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
10 V
5 V
4 V
3.5 V
3 V
2.5 V
V_{GS} = 2 V
Pulse Test


Typical Transfer Characteristics
25°C
75°C
Pulse Test
Drain Current
Gate to Source Voltage
Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
5 A
2 A
1 A
Drain to Source Saturation Voltage
Gate to Source Voltage
Static Drain to Source on State
Resistance vs. Drain Current
Pulse Test
Static Drain to Source on State Resistance
Drain Current
Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
5 A
1 A, 2 A
Case Temperature
Forward Transfer Admittance
vs. Drain Current
Pulse Test
25°C
75°C
Forward Transfer Admittance
Drain Current
Body to Drain Diode Reverse
Recovery Time
di/dt = 50 A/µs Ta = 25°C
Pulse Test
Reverse Recovery Time
Reverse Drain Current

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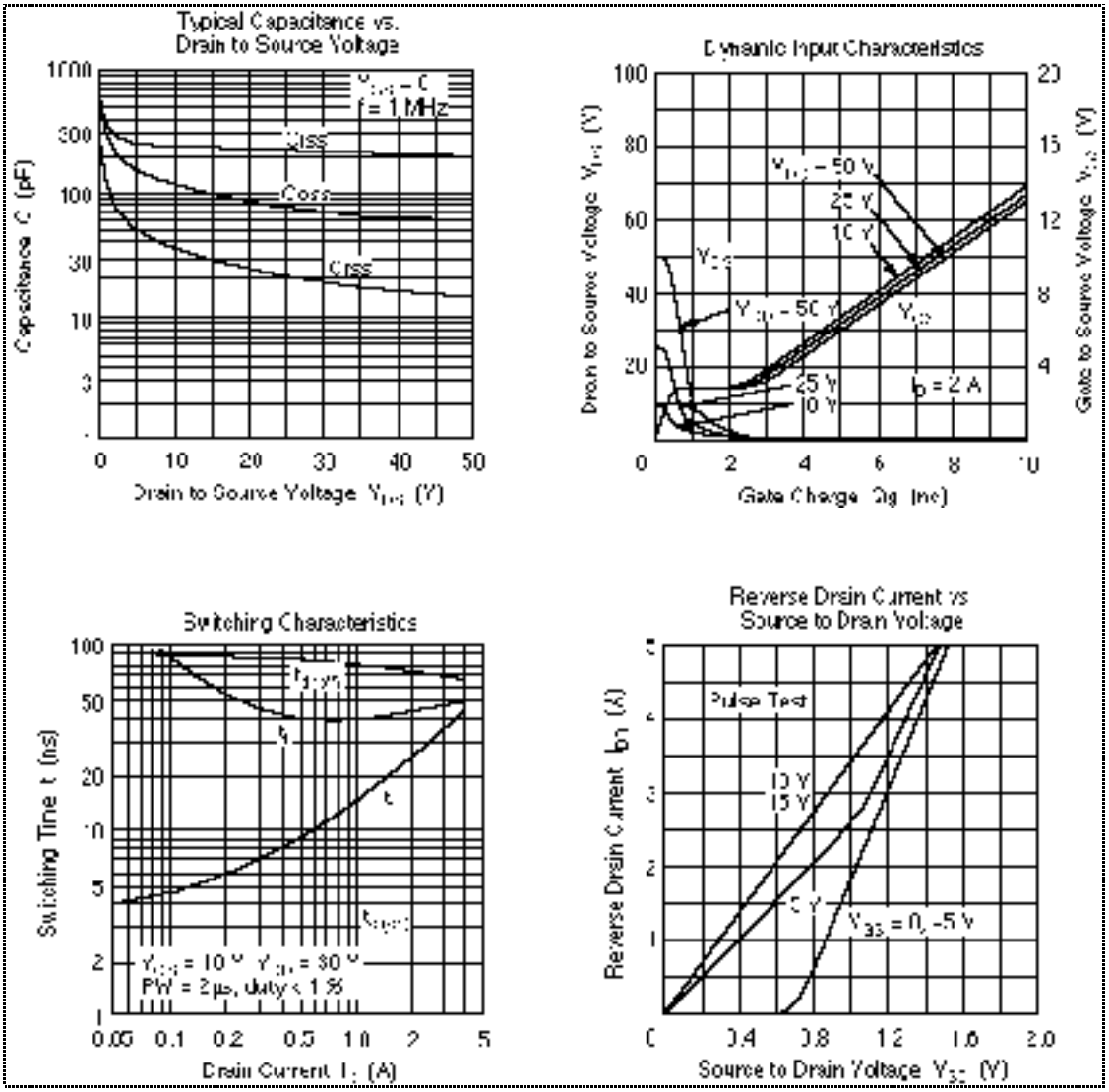
Typical Capacitance vs.
Drain to Source Voltage
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
Drain to Source Voltage
Dynamic Input Characteristics
Drain to Source Voltage
Gate to Source Voltage
Gate Charge
Switching Characteristics
Switching Time t (ns)
Drain Current
PW = 2µs, duty < 1 %
Reverse Drain Current vs
Source to Drain Voltage
Pulse Test
Reverse Drain Current
Source to Drain Voltage

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