4518B

DUAL 4-BIT DECADE COUNTER

DESCRIPTION – The 4518B is a Dual 4-Bit Internally Synchronous BCD Counter. Each counter has both an active HIGH Clock Input (CP_0) and an active LOW Clock Input ($\overline{CP}_1$), buffered Outputs from all four bit positions (Q_0-Q_3) and an active HIGH overriding asynchronous Master Reset Input (MR).

The counter advances on either the LOW-to-HIGH transition of the CP_0 Input if $\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of the $\overline{CP}_1$ Input if CP_0 is LOW (see the Truth Table). Either Clock Input (CP_0, $\overline{CP}_1$) may be used as the Clock Input to the counter and the other Clock Input may be used as a Clock Inhibit Input.

A HIGH on the Master Reset Input (MR) resets the counter (Q_0-Q_3 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP}_1$).

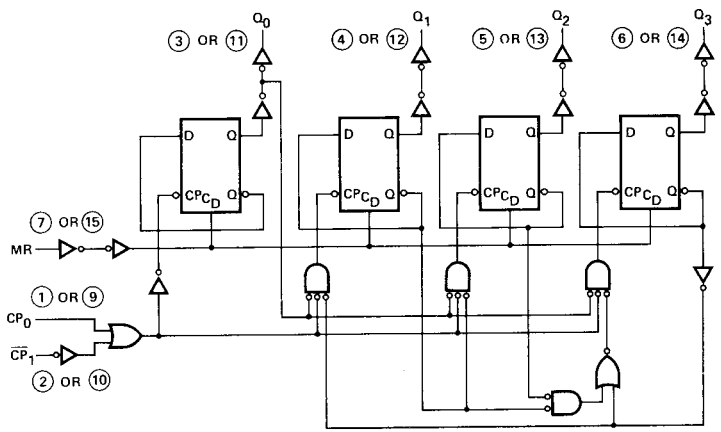
- **TYPICAL COUNT FREQUENCY OF 10 MHz AT V_{DD} = 10 V**
- **TRIGGERED ON EITHER A LOW-TO-HIGH OR A HIGH-TO-LOW TRANSITION**
- **ASYNCHRONOUS ACTIVE HIGH MASTER RESET**
- **BUFFERED OUTPUTS FROM ALL FOUR BIT POSITIONS**
- **FULLY SYNCHRONOUS COUNTING**

TRUTH TABLE

CP_0	$\overline{CP}_1$	MR	MODE
↗	H	L	Counter Advances
L	↘	L	Counter Advances
↘	X	L	No Change
X	↗	L	No Change
↗	L	L	No Change
H	↘	L	No Change
X	X	H	Reset (Asynchronous)

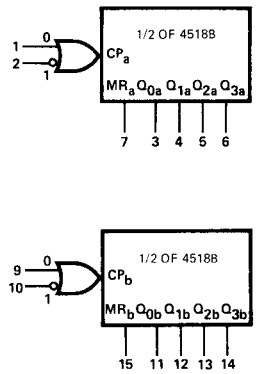
X = Don't Care
L = LOW Level
H = HIGH Level
↗ = Positive-Going Transition
↘ = Negative-Going Transition

1/2 OF A 4518B LOGIC DIAGRAM



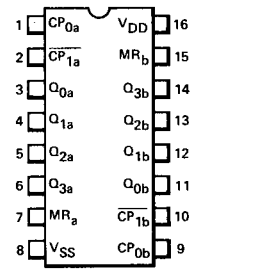
V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

LOGIC SYMBOLS



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

PIN NAMES

CP_{0a}, CP_{0b}	Clock Input (L → H (Triggered)
$\overline{CP}_{1a}$, $\overline{CP}_{1b}$	Clock Input (H → L Triggered)
MR_a, MR_b	Master Reset Inputs
Q_{0a}–Q_{3a}	Outputs
Q_{0b}–Q_{3b}	Outputs

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DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

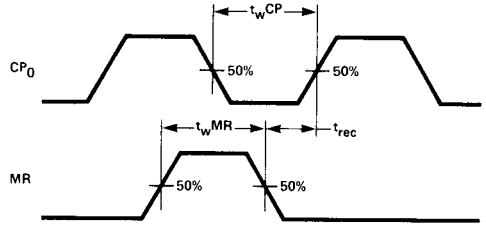
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, F_{SS} = 0 V, T_A = 25°C (See Note 2)

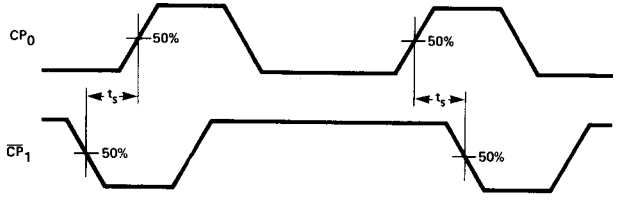
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP_1}$		220	480		95	210		60	168	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PLH}	to Q_n		220	480		95	210		60	168	ns	
t_{PHL}	Propagation Delay, MR to Q_n		220	480		90	210		60	168	ns	
t_{TLH}	Output Transition Time		65	135		35	70		25	45	ns	
t_{THL}			65	135		35	70		25	45	ns	
t_wMR	MR Minimum Pulse Width	180	70		70	30		56	20		ns	
t_wCP	CP_0 or $\overline{CP_1}$ Minimum Pulse Width	275	120		120	50		96	35		ns	
t_{rec}	MR Recovery Time	40	15		25	5		20	0		ns	
t_s	Set-Up Time, CP_0 to $\overline{CP_1}$	275	130		125	57		100	40		ns	
t_s	Set-Up Time, $\overline{CP_1}$ to CP_0	275	130		125	57		100	40		ns	
f_{MAX}	Input Count Frequency (Note 3)	2	4		4	10		5	12		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTHS FOR CP_0, $\overline{CP_1}$ AND MR AND MR RECOVERY TIME



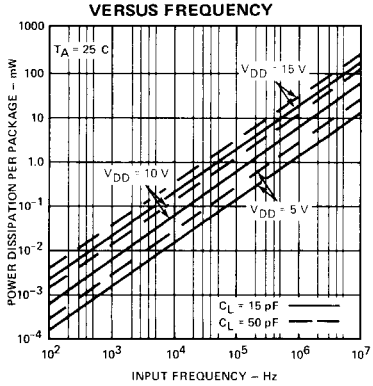
SET-UP TIMES, CP_0 TO $\overline{CP_1}$ AND $\overline{CP_1}$ TO CP_0

CONDITIONS: $\overline{CP_1}$ = HIGH and the device triggers on a LOW-to-HIGH transition at CP_0. The timing also applies when CP_0 = LOW and the device triggers on a HIGH-to-LOW transition at $\overline{CP_1}$.

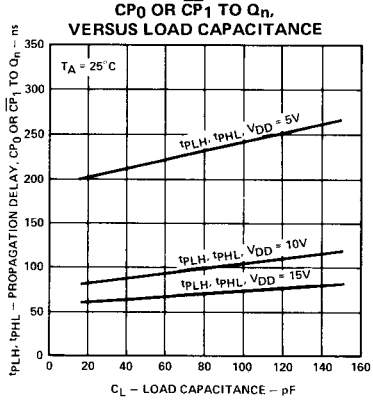
NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL ELECTRICAL CHARACTERISTICS

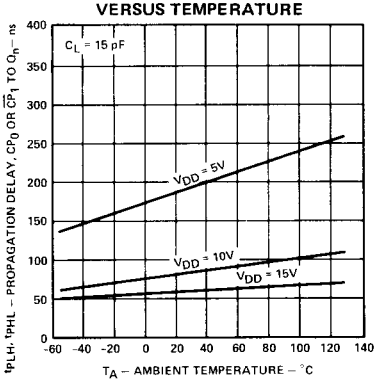
POWER DISSIPATION VERSUS FREQUENCY



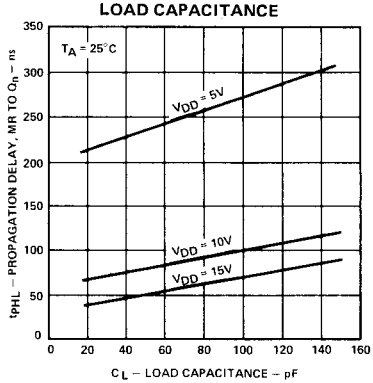
PROPAGATION DELAY, CP_0 OR $\overline{CP}_1$ TO Q_n, VERSUS LOAD CAPACITANCE



PROPAGATION DELAY, CP_0 OR $\overline{CP}_1$ TO Q_n, VERSUS TEMPERATURE



PROPAGATION DELAY, MR TO Q_n, VERSUS LOAD CAPACITANCE



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