

**4053****CMOS IC**

TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

DESCRIPTION

UTC **4053** is triple 2-channel analog multiplexers/demultiplexers for application as digitally-controlled analog switches.

The device has three separate digital control inputs and an inhibit input. It features low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

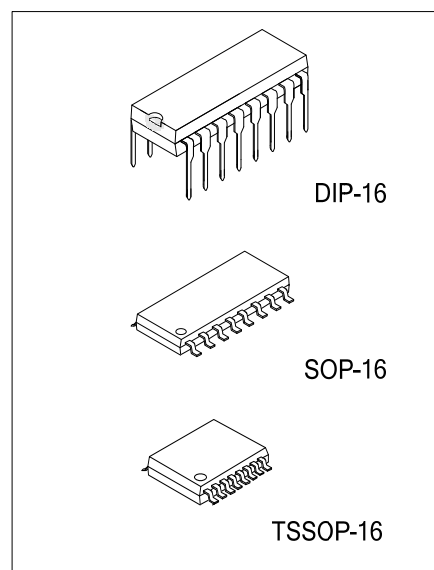
FEATURES

- * Wide Analog Voltage Range: $V_{DD}-V_{EE} = 3V \sim 18V$.
(Note: V_{EE} must be $\leq V_{SS}$)
- * Break-Before-Make Switching Eliminates Channel Overlap.
- * Linearized Transfer Characteristics
- * Implement an SPDT Switch Effectively.
- * Pin to Pin Replacement for CD4053

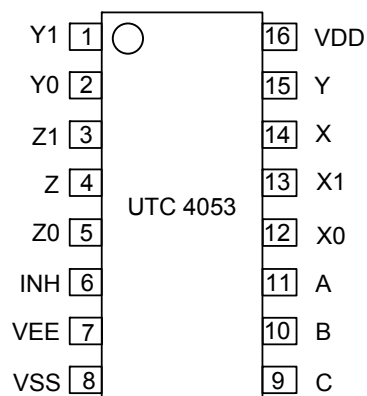
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
4053L-D16-T	4053G-D16-T	DIP-16	Tube
4053L-P16-R	4053G-P16-R	TSSOP-16	Tape Reel
4053L-P16-T	4053G-P16-T	TSSOP-16	Tube
4053L-S16-R	4053G-S16-R	SOP-16	Tape Reel
4053L-S16-T	4053G-S16-T	SOP-16	Tube

4053L-D16-R (1) Packing Type (2) Package Type (3) Lead Free	(1) T: Tube, R: Tape Reel (2) D16: DIP-16, P16: TSSOP-16, S16: SOP-16 (3) G: Halogen Free, L: Lead Free
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■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN No.	SYMBAL	NAME AND FUNCTION
14,15,4	X,Y,Z	Commons Input/Output
6	INH	Inhibit Input
7	V _{EE}	Supply Voltage
8	V _{SS}	Ground
11,10,9	A,B,C	Digital Control Inputs
12,13	X0,X1	A-X Switches Inputs/Outputs
2,1	Y0,Y1	B-Y Switches Inputs/Outputs
5,3	Z0,Z1	C-Z Switches Inputs/Outputs
16	V _{DD}	Positive Supply Voltage

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Referenced to V_{EE} , $V_{SS} \geq V_{EE}$)	V_{DD}	-0.5 ~ +18	V
Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	V_{IN} , V_{OUT}	-0.5 ~ $V_{DD} + 0.5$	V
Input Current (DC or Transient), per Control Pin	I_{IN}	± 10	mA
Switch Through Current	I_{SW}	± 25	mA
Power Dissipation	P_D	500	mW
Derating above 65°C		7	mW/°C
Junction Temperature	T_J	125	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY REQUIREMENTS (Voltages Referenced to V _{EE})							
Power Supply Voltage Range		V _{DD}	V _{DD} – 3 ≥ V _{SS} ≥ V _{EE}	3		18	V
Quiescent Current per Package	V _{DD} =5V	I _Q	Control Inputs: V _{IN} = V _{SS} or V _{DD} Switch I/O: V _{EE} ≤ V _{I/O} ≤ V _{DD} , ΔV _{SW} ≤ 500mV (Note 2)		0.005	5	μA
	V _{DD} =10V				0.010	10	μA
	V _{DD} =15V				0.015	20	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	V _{DD} =5V	I _{D(AV)}	T _A =25°C only (The channel component, (V _{IN} -V _{OUT})/R _{ON} , is excluded)	(0.07 μA/kHz) f + I _Q			μA
	V _{DD} =10V			(0.20 μA/kHz) f + I _Q			μA
	V _{DD} =15V			(0.36 μA/kHz) f + I _Q			μA
SWITCHES IN/OUT AND COMMONS OUT/IN -- X, Y, Z (Voltages Referenced to V _{EE})							
Recommended Peak-to-Peak Voltage Into or Out of the Switch		V _{I/O}	Channel On or Off	0		V _{DD}	V _{PP}
Recommended Static or Dynamic Voltage Across the Switch (Note2)		ΔV _{SW}	Channel On	0		600	mV
Output Offset Voltage		V _{O(OFF)}	V _{IN} = 0V, No Load		10		μV
ON Resistance	V _{DD} =5V	R _{ON}	ΔV _{SW} ≤ 500mV V _{IN} = V _{IL} or V _{IH} (Control), and V _{IN} = 0 to V _{DD} (Switch)		250	1050	Ω
	V _{DD} =10V				120	500	Ω
	V _{DD} =15V				80	280	Ω
Δ ON Resistance Between Any Two Channels in the Same Package	V _{DD} =5V	ΔR _{ON}			25	70	Ω
	V _{DD} =10V				10	50	Ω
	V _{DD} =15V				10	45	Ω
Off-Channel Leakage Current		I _{OFF}	V _{IN} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel, V _{DD} =15V		±0.05	±100	nA
Capacitance, Switch I/O		C _{I/O}	Inhibit = V _{DD}		10		pF
Capacitance, Common O/I		C _{O/I}	Inhibit = V _{DD}		17		pF
Capacitance, Feedthrough (Channel Off)		C _{I/O}	Pins Not Adjacent		0.15		pF
			Pins Adjacent		0.47		Pf
CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V _{SS})							
Low Level Input Voltage	V _{DD} =5V	V _{IL}	R _{ON} = per spec, I _{OFF} = per spec		2.25	1.5	V
	V _{DD} =10V				4.50	3.0	V
	V _{DD} =15V				6.75	4.0	V
High Level Input Voltage	V _{DD} =5V	V _{IH}	R _{ON} = per spec, I _{OFF} = per spec	3.5	2.75		V
	V _{DD} =10V			7.0	5.50		V
	V _{DD} =15V			11	8.25		V
Input Leakage Current		I _{LEAK}	V _{IN} = 0 or V _{DD} , V _{DD} =15V		±0.00001	±0.1	μA
Input Capacitance		C _{IN}			5.0	7.5	pF

■ DYNAMIC ELECTRICAL CHARACTERISTICS

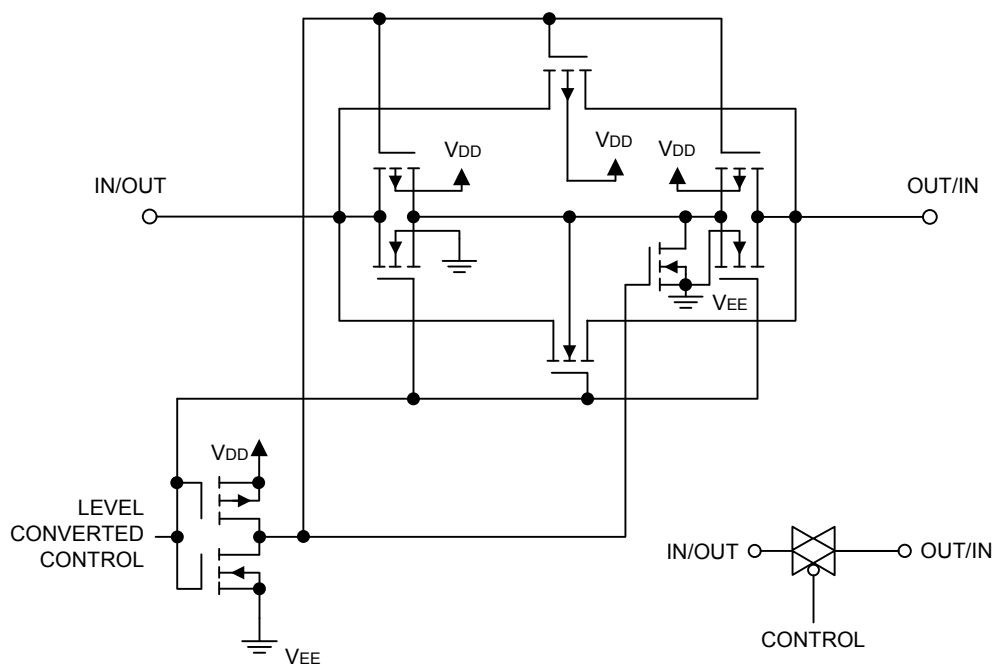
($C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$, $V_{EE} \leq V_{SS}$, unless otherwise specified)

PARAMETER	SYMBOL	$V_{DD}-V_{EE}$ V_{DC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Times Switch Input to Switch Output ($R_L = 10\text{ k}\Omega$)	t_{PLH} , t_{PHL}	5	t_{PLH} , $t_{PHL} = (0.17\text{ ns/pF})C_L + 16.5\text{ns}$		25	65	ns
		10	t_{PLH} , $t_{PHL} = (0.08\text{ ns/pF})C_L + 4.0\text{ns}$		8.0	20	ns
		15	t_{PLH} , $t_{PHL} = (0.06\text{ ns/pF})C_L + 3.0\text{ns}$		6.0	15	ns
Inhibit to Output	t_{PHZ} , t_{PLZ} t_{PZH} , t_{PZL}	5	$(R_L = 10\text{k}\Omega, V_{EE} = V_{SS})$, Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level		275	550	ns
		10			140	280	ns
		15			110	220	ns
Control Input to Output	t_{PLH} , t_{PHL}	5	$R_L = 10\text{k}\Omega, V_{EE} = V_{SS}$		300	600	ns
		10			120	240	ns
		15			80	160	ns
Total Harmonic Distortion	THD	10	$R_L = 10\text{k}\Omega, f = 1\text{ kHz}, V_{IN} = 5\text{ V}_{PP}$		0.07		%
Bandwidth	BW	10	$R_L = 1\text{k}\Omega, V_{IN} = 1/2(V_{DD}-V_{EE})\text{ p-p}$, $C_L = 50\text{pF}$, $20\text{ Log}(V_{OUT}/V_{IN}) = -3\text{dB}$		17		MHz
Off Channel Feedthrough Attenuation		10	$R_L = 1\text{k}\Omega, V_{IN} = 1/2(V_{DD}-V_{EE})\text{ p-p}$ $f_{IN} = 55\text{MHz}$		-50		dB
Channel Separation		10	$R_L = 1\text{k}\Omega, V_{IN} = 1/2(V_{DD}-V_{EE})\text{ p-p}$ $f_{IN} = 3\text{MHz}$		-50		dB
Crosstalk, Control Input to Common O/I		10	$R_1 = 1\text{k}\Omega, R_L = 10\text{k}\Omega$ Control $t_{TLH} = t_{THL} = 20\text{ns}$, Inhibit = V_{SS}		75		mV

Note: 1. Data of "TYP" is intended as an indication of the IC's potential performance.

2. For voltage drops across the switch (ΔV_{SW}) $> 600\text{mV}$ ($> 300\text{mV}$ at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

■ TEST CIRCUIT

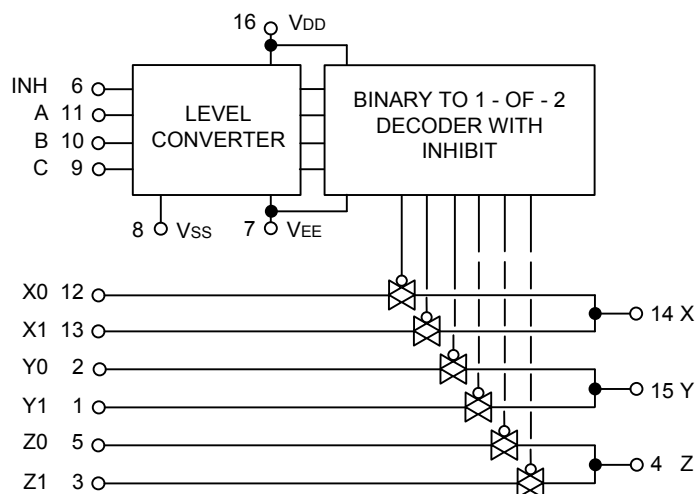


Switch Circuit Schematic

■ TRUTH TABLE

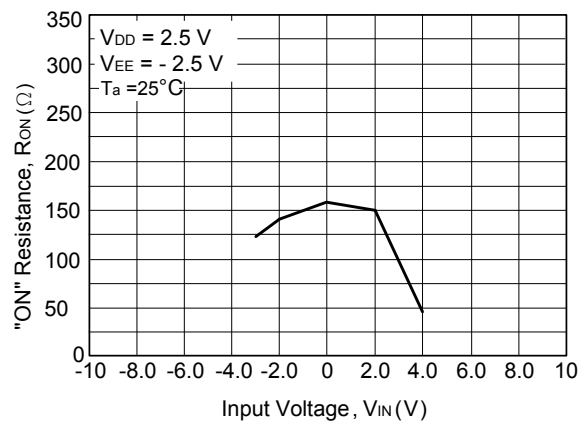
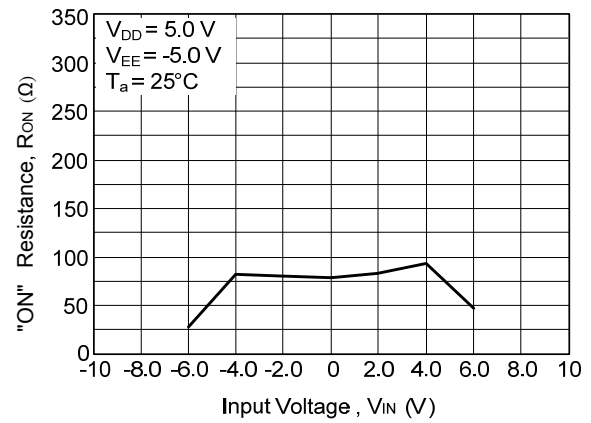
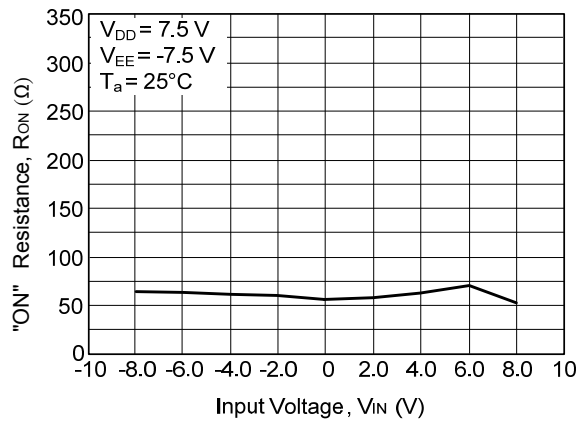
Control Inputs				ON Switches		
INHIBIT	Select			UTC 4053		
	C	B	A			
0	0	0	0	Z0	Y0	X0
0	0	0	1	Z0	Y0	X1
0	0	1	0	Z0	Y1	X0
0	0	1	1	Z0	Y1	X1
0	1	0	0	Z1	Y0	X0
0	1	0	1	Z1	Y0	X1
0	1	1	0	Z1	Y1	X0
0	1	1	1	Z1	Y1	X1
1	x	x	x	None		

x = Don't Care



UTC 4053 Functional Diagram

■ TYPICAL CHARACTERISTICS



UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.