

- Frequency range 50.01MHz to 200MHz
- LVCMOS Output
- Supply Voltage 3.3 VDC
- High Q fundamental mode crystal
- Low jitter multiplier circuit
- Low unit cost

DESCRIPTION

GV64 VCXOs, are packaged in an industry-standard, 6 pad, 11.4mm x 9.6mm x 4.7mm SMD package. The VCXO incorporates a high Q fundamental mode crystal and a low jitter multiplier circuit.

SPECIFICATION

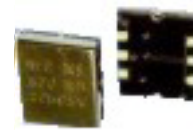
Frequency Range:	50.01MHz to 200.0MHz
Supply Voltage:	3.3 VDC $\pm 5\%$
Output Logic:	LVCMOS
Integrated Phase Jitter:	2.3ps typical, 4.0ps maximum (for 155.250MHz)
Period Jitter RMS:	4.0ps typical (for 155.250MHz)
Period Jitter Peak to peak:	27.0ps typical (for 155.250MHz)
Phase Noise:	See table below
Initial Frequency Accuracy:	Tune to the nominal frequency with $V_c = 1.65 \pm 0.2VDC$
Output Voltage HIGH (1):	90% Vdd minimum
Output Voltage LOW (0):	10% Vdd maximum
Pulling Range:	From $\pm 30ppm$ to $\pm 150ppm$
Temperature Stability:	See table
Output Load:	15pF
Start-up Time:	10ms maximum, 5ms typical
Duty Cycle:	50% $\pm 5\%$ measured at 50% Vdd
Rise/Fall Times:	1.2ns typical (15pF load)
Current Consumption:	25mA maximum (15pF load)
Linearity:	10% maximum, 6% typical
Modulation Bandwidth:	25kHz minimum
Input Impedance:	2 M Ω minimum
Slope Polarity:	Monotonic and Positive. (An increase of control voltage always increases output frequency.)
Storage Temperature:	-50° to +100°C
Ageing:	$\pm 5ppm$ per year maximum
Enable/Disable (Tristate):	Pads 2 or 5, Enable high or 70% Vdd min applied to Tri-state pad to enable output. 30% Vdd max. to disable output (high impedance)
RoHS Status:	Fully compliant

FREQUENCY STABILITY

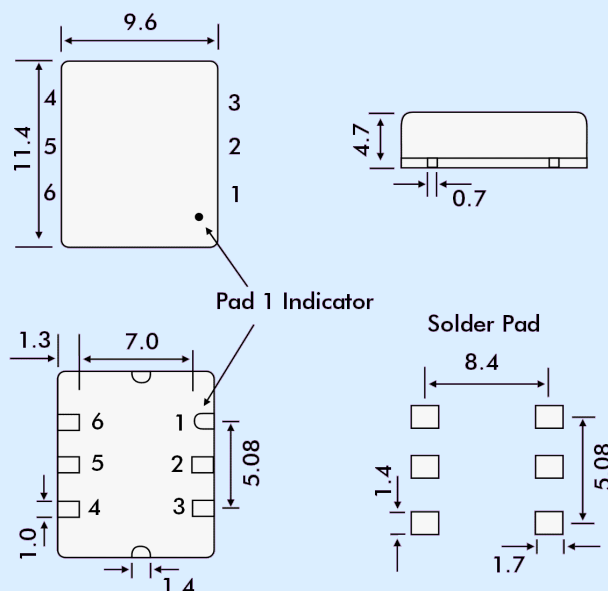
Stability Code	Stability $\pm ppm$	Temp. Range
A	25	0°~+70°C
B	50	0°~+70°C
C	100	0°~+70°C
D	25	-40°~+85°C
E	50	-40°~+85°C
F	100	-40°~+85°C

If non-standard frequency stability is required
Use 'I' followed by stability, i.e. I20 for $\pm 20ppm$

11.4 x 9.6 x 4.7mm 6 pad SMD



OUTLINE & DIMENSIONS



Pad Connections

- 1 Voltage Control (rounded pad)
- 2 Tri-state*
- 3 Ground
- 4 Output
- 5 Tristate*
- 6 Supply Voltage

*Pads 2 and 5 are connected internally

PHASE NOISE

Offset	Frequency 155.25MHz
10Hz	-65dBc/Hz
100Hz	-95dBc/Hz
1kHz	-120dBc/Hz
10kHz	-128dBc/Hz
100kHz	-122dBc/Hz
1MHz	-120dBc/Hz
10MHz	-140dBc/Hz

PART NUMBER SCHEDULE

Example: **3GV64B-80N-155.25**

