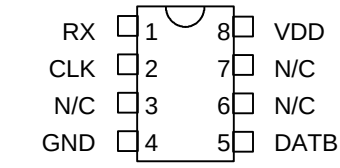
MONOLITHIC MANCHESTER DECODER (SERIES 3D7502)

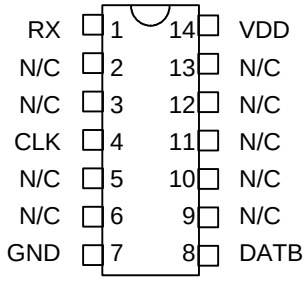
FEATURES

- All-silicon, low-power CMOS technology
- TTL/CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP pkg.)
- Low ground bounce noise
- **Maximum data rate:** 50 MBaud
- **Data rate range:** ±15%

PACKAGES



3D7502M-xxx DIP (.300)
3D7502H-xxx Gull Wing (.300)
3D7502Z-xxx SOIC (.150)



3D7502-xxx DIP (.300)
3D7502G-xxx Gull Wing (.300)
3D7502D-xxx SOIC (.150)

FUNCTIONAL DESCRIPTION

PIN DESCRIPTIONS

RX	Signal Input
CLK	Signal Output (Clock)
DATB	Signal Output (Data)
VCC	+5 Volts
GND	Ground

The 3D7502 product family consists of monolithic CMOS Manchester Decoders. The unit accepts at the RX input a bi-phase-level, embedded-clock signal. In this encoding mode, a logic one is represented by a high-to-low transition within the bit cell, while a logic zero is represented by a low-to-high transition. The recovered clock and data signals are presented on CLK and DATB, respectively, with the data signal inverted. The operating baud rate (in MBaud) is specified by the dash number. The input baud rate may vary by as much as ±15% from the nominal device baud rate without compromising the integrity of the information received.

Because the 3D7502 is not PLL-based, it does not require a long preamble in order to lock onto the received signal. Rather, the device requires at most one bit cell before the data presented at the output is valid. This is extremely useful in cases where the information arrives in bursts and the input is otherwise turned off.

The all-CMOS 3D7502 integrated circuit has been designed as a reliable, economic alternative to hybrid TTL Manchester Decoders. It is TTL- and CMOS-compatible, capable of driving ten 74LS-type loads. It is offered in standard 8-pin and 14-pin auto-insertable DIPs and space saving surface mount 8-pin and 14-pin SOICs.

TABLE 1: PART NUMBER SPECIFICATIONS

PART NUMBER	BAUD RATE (MBaud)		
	Nominal	Minimum	Maximum
3D7502-5	5.00	4.25	5.75
3D7502-10	10.00	8.50	11.50
3D7502-20	20.00	17.00	23.00
3D7502-25	25.00	21.25	28.75
3D7502-30	30.00	25.50	34.50
3D7502-40	40.00	34.00	46.00
3D7502-50	50.00	42.50	57.50

NOTES: Any baud rate between 5 and 50 MBaud not shown is also available at no extra cost. **©1997 Data Delay Devices**

APPLICATION NOTES

The 3D7502 Manchester Decoder samples the input at precise pre-selected intervals to retrieve the data and to recover the clock from the received data stream. Its architecture comprises finely tuned delay elements and proprietary circuitry which, in conjunction with other circuits, implement the data decoding and clock recovery function.

INPUT SIGNAL CHARACTERISTICS

Encoded data transmitted from a source arrives at its destination corrupted. Such corruption of the received data manifests itself as jitter and/or pulse width distortion at the input to the device. The instantaneous deviations from nominal Baud Rate and/or Pulse Width (high or low) adversely impact the data extraction and clock recovery function if their published limits are exceeded. **See Table 4, Allowed Baud Rate/Duty Cycle.**

The 3D7502 Manchester Decoder Data Input **is TTL compatible. The user should assure himself that** the 1.5 volt TTL threshold is used when referring to all timing, especially the input pulse widths.

FREQUENCY (JITTER) ERRORS

The 3D7502 Manchester Decoder, being a self-timed device, is tolerant of frequency modulation (jitter) present in the input data stream, provided that the input data pulse width variations remain within the allowable ranges.

OUTPUT SIGNAL CHARACTERISTICS

The 3D7502 presents at its outputs the decoded data (inverted) and the recovered clock. The decoded data is **valid at the rising edge of the clock.**

The clock recovery function operates in two modes dictated by the input data stream bit sequence. When a data bit is succeeded by its inverse, the clock recovery circuit is engaged and forces the clock output low for a time equal to **one over twice the baud rate**. Otherwise, the input is presented at the clock output unchanged, shifted in time.

When engaged, the clock recovery circuit generates a low-going pulse of fixed width. Therefore, the clock duty cycle is strongly dependent on the baud rate, as this will affect the clock-high duration.

The clock output falling edge is not operated on by the clock recovery circuitry. It, therefore, preserves more accurately the clock frequency information embedded in the transmitted data. Therefore, it can be used, if it is desired, to retrieve clock frequency information.

POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

CMOS integrated circuitry is strongly dependent on power supply and temperature. The monolithic 3D7502 Manchester Decoder utilizes novel and innovative compensation circuitry to minimize timing variations induced by fluctuations in power supply and/or temperature.

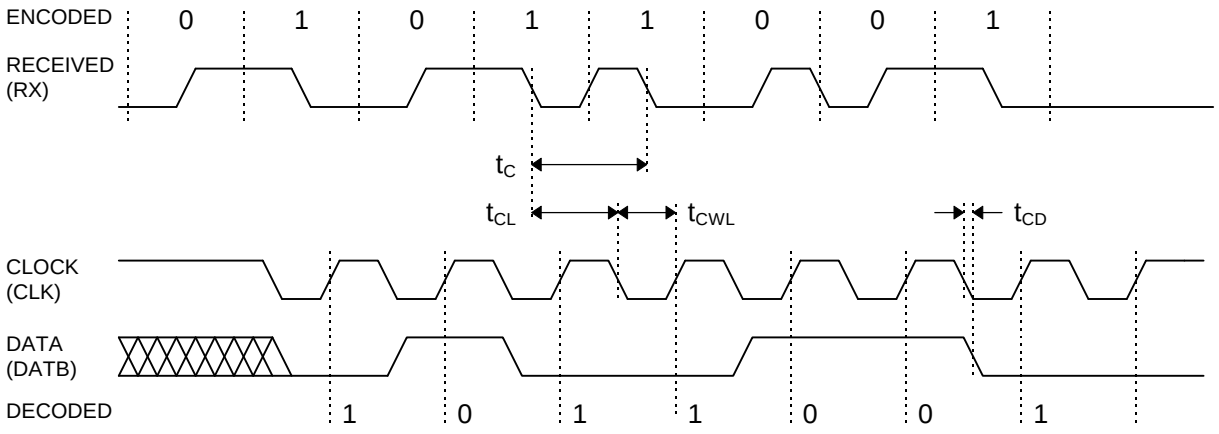


Figure 1: Timing Diagram

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DEVICE SPECIFICATIONS

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-10	10	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 3: DC ELECTRICAL CHARACTERISTICS

(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		40	mA	
High Level Input Voltage	V_{IH}	2.0		V	
Low Level Input Voltage	V_{IL}		0.8	V	
High Level Input Current	I_{IH}		1.0	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}		1.0	µA	$V_{IL} = 0V$
High Level Output Current	I_{OH}	-4.0		mA	$V_{DD} = 4.75V$ $V_{OH} = 2.4V$
Low Level Output Current	I_{OL}	4.0		mA	$V_{DD} = 4.75V$ $V_{OL} = 0.4V$
Output Rise & Fall Time	T_R & T_F		2	ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = 2 * C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/pin (pf)
F = Input frequency (GHz)

Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

TABLE 4: AC ELECTRICAL CHARACTERISTICS

(0C to 70C, 4.75V to 5.25V, except as noted)

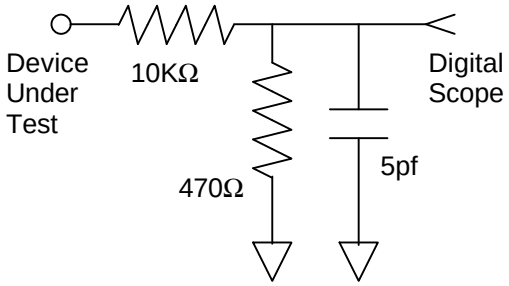
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Nominal Input Baud Rate	f_{BN}	5		50	MBaud	
Allowed Input Baud Rate Deviation	f_B	-0.15 f_{BN}		0.15 f_{BN}	MBaud	25C, 5.00V
Allowed Input Baud Rate Deviation	f_B	-0.05 f_{BN}		0.05 f_{BN}	MBaud	-40C to 85C 4.75V to 5.25V
Allowed Input Baud Rate Deviation	f_B	-0.03 f_{BN}		0.03 f_{BN}	MBaud	-55C to 125C 4.75V to 5.25V
Allowed Input Duty Cycle		42.5	50.0	57.5	%	
Bit Cell Time	tc		1000/f_B		ns	
Input Data Edge to Clock Falling Edge	t_{CL}		0.75 tc		ns	
Clock Width Low	t_{CWL}		500/f_{BN}		ns	±2ns or 5%
Clock Falling Edge to Data Transition	t_{CD}	3.0	4.0	5.0	ns	

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 5.0V ± 0.1V
Input Pulse: High = 3.0V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width: PW_{IN} = 1/(2*BAUD)
Period: PER_{IN} = 1/BAUD

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

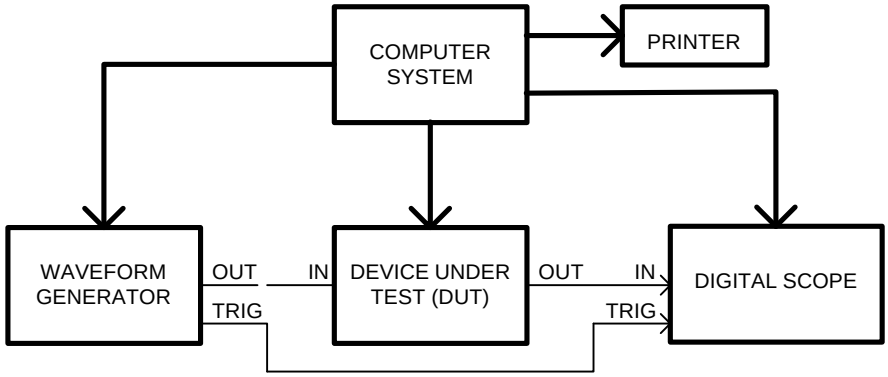


Figure 2: Test Setup

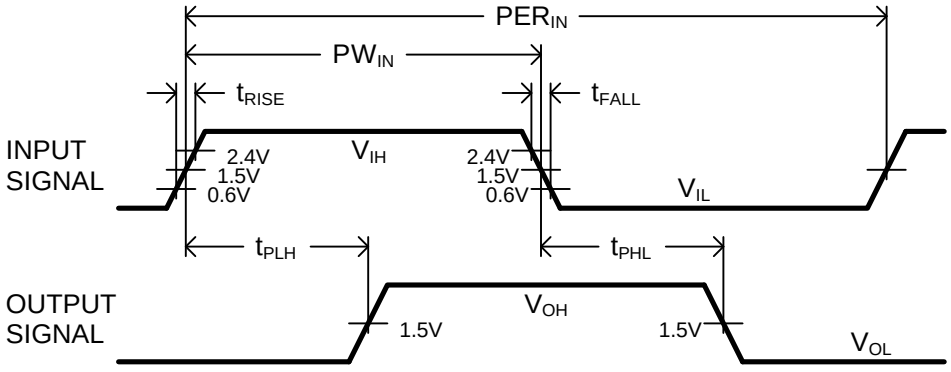


Figure 3: Timing Diagram