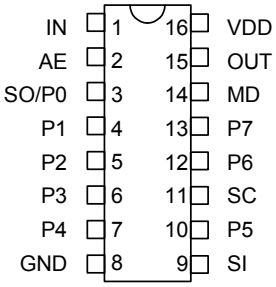
MONOLITHIC 8-BIT PROGRAMMABLE DELAY LINE (SERIES 3D7428 – LOW NOISE)

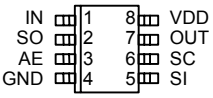
FEATURES

- All-silicon, low-power CMOS technology
- TTL/CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP pkg.)
- Leading- and trailing-edge accuracy
- Programmable via serial or parallel interface
- **Increment range:** 0.25 through 20.0ns
- **Delay tolerance:** 0.5% (See Table 1)
- **Supply current:** 3mA typical
- **Temperature stability:** ±1.5% max (-40C to 85C)
- **Vdd stability:** ±0.5% max (4.75V to 5.25V)

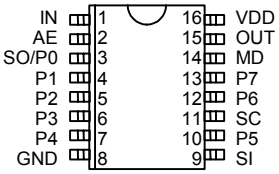
PACKAGES



3D7428-xx DIP



3D7428Z-xx SOIC



3D7428S-xx SOL

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D7428 device is a versatile 8-bit programmable monolithic delay line. The input (IN) is reproduced at the output (OUT) without inversion, shifted in time as per the user selection. Delay values, programmed either via the serial or parallel interface, can be varied over 255 equal steps according to the formula:

$$T_{i,nom} = T_{inh} + i * T_{inc}$$

where i is the programmed address, T_{inc} is the delay increment (equal to the device dash number), and T_{inh} is the inherent (address zero) delay. The device features both rising- and falling-edge accuracy.

PIN DESCRIPTIONS

IN	Signal Input
OUT	Signal Output
MD	Mode Select
AE	Address Enable
P0-P7	Parallel Data Input
SC	Serial Clock
SI	Serial Data Input
SO	Serial Data Output
VDD	+5 Volts
GND	Ground

The all-CMOS 3D7428 integrated circuit has been designed as a reliable, economic alternative to hybrid TTL programmable delay lines. It is offered in a standard 16-pin auto-insertable DIP and a surface mount 16-pin SOL. An 8-pin SOIC package is available for applications where the parallel interface is not needed.

TABLE 1: PART NUMBER SPECIFICATIONS

PART NUMBER	DELAYS AND TOLERANCES			INPUT RESTRICTIONS			
	Inherent Delay (ns)	Delay Range (ns)	Delay Step (ns)	Rec'd Max Frequency	Absolute Max Frequency	Rec'd Min Pulse Width	Absolute Min Pulse Width
3D7428-0.25	10.5 ± 2.0	63.75 ± 0.4	0.25 ± 0.12	6.25 MHz	77 MHz	80.0 ns	6.5 ns
3D7428-0.5	10.5 ± 2.0	127.5 ± 0.5	0.50 ± 0.25	3.12 MHz	45 MHz	160.0 ns	11.0 ns
3D7428-1	10.5 ± 2.0	255.0 ± 1.0	1.00 ± 0.50	1.56 MHz	22 MHz	320.0 ns	22.0 ns
3D7428-1.5	10.5 ± 2.0	382.5 ± 1.5	1.50 ± 0.75	1.04 MHz	15 MHz	480.0 ns	33.0 ns
3D7428-2	10.5 ± 2.0	510.0 ± 2.0	2.00 ± 1.00	781 KHz	11 MHz	640.0 ns	44.0 ns
3D7428-2.5	10.5 ± 2.5	637.5 ± 2.5	2.50 ± 1.25	625 KHz	9.0 MHz	800.0 ns	55.0 ns
3D7428-4	13.0 ± 4.0	1020 ± 3.2	4.00 ± 2.00	390 KHz	5.6 MHz	1280.0 ns	88.0 ns
3D7428-5	15.0 ± 5.0	1275 ± 4.0	5.00 ± 2.50	312 KHz	4.5 MHz	1600.0 ns	110.0 ns
3D7428-7.5	20.0 ± 7.5	1912.5 ± 6.0	7.50 ± 3.75	208 KHz	3.0 MHz	2400.0 ns	165.0 ns
3D7428-10	23.5 ± 10	2550 ± 8.0	10.0 ± 5.00	156 KHz	2.2 MHz	3200.0 ns	220.0 ns
3D7428-15	33.0 ± 15	3825 ± 12	15.0 ± 9.00	104 KHz	1.5 MHz	4800.0 ns	330.0 ns
3D7428-20	42.0 ± 20	5100 ± 16	20.0 ± 12.0	78 KHz	1.1 MHz	6400.0 ns	440.0 ns

NOTES: Any delay increment between 0.25 and 20 ns not shown is also available as standard.
See application notes section for more details

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APPLICATION NOTES

GENERAL INFORMATION

The 8-bit programmable 3D7428 delay line architecture is comprised of a number of delay cells connected in series with their respective outputs multiplexed onto the Delay Out pin (OUT) by the user-selected programming data (the address). Each delay cell produces at its output a replica of the signal present at its input, shifted in time. The change in delay from one address setting to the next is called the *increment*, or LSB. It is nominally equal to the device dash number. The minimum delay, achieved by setting the address to zero, is called the *inherent delay*.

For best performance, it is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred. Also, signal traces should be kept as short as possible.

DELAY ACCURACY

There are a number of ways of characterizing the delay accuracy of a programmable line. The first is the *differential nonlinearity* (DNL), also referred to as the increment error. It is defined as the deviation of the increment at a given address from its nominal value. For most dash numbers, the DNL is within 0.5 LSB at every address (see Table 1: Delay Step).

The *integrated nonlinearity* (INL) is determined by first constructing the least-squares best fit straight line through the delay-versus-address data. The INL is then the deviation of a given delay from this line. For all dash numbers, the INL is within 1.0 LSB at every address.

The *relative error* is defined as follows:

$$e_{rel} = (T_i - T_0) - i * T_{inc}$$

where i is the address, T_i is the measured delay at the i'th address, T_0 is the measured inherent delay, and T_{inc} is the nominal increment. It is very similar to the INL, but simpler to calculate. For most dash numbers, the relative error is less than 1.0 LSB at every address (see Table 1: Delay Range).

The *absolute error* is defined as follows:

$$e_{abs} = T_i - (T_{inh} + i * T_{inc})$$

where T_{inh} is the nominal inherent delay. The absolute error is limited to 1.5 LSB or 3.0 ns, whichever is greater, at every address.

The *inherent delay error* is the deviation of the inherent delay from its nominal value. It is limited to 1.0 LSB or 2.0 ns, whichever is greater.

DELAY STABILITY

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The 3D7428 utilizes novel compensation circuitry to minimize the delay variations induced by fluctuations in power supply and/or temperature.

With regard to stability, the delay of the 3D7428 at a given address, i, can be split into two components: the *inherent delay* (T_0) and the *relative delay* ($T_i - T_0$). These components exhibit very different stability coefficients, both of which must be considered in very critical applications.

The thermal coefficient of the relative delay is limited to ±250 PPM/C, which is equivalent to a variation, over the -40C to 85C operating range, of ±1.5% from the room-temperature delay settings. This holds for all dash numbers. The thermal coefficient of the inherent delay is nominally +10ps/C for dash numbers less than 1, and +15ps/C for all other dash numbers.

The power supply sensitivity of the relative delay is ±0.5% over the 4.75V to 5.25V operating range, with respect to the delay settings at the nominal 5.0V power supply. This holds for all dash numbers. The sensitivity of the inherent delay is nominally –1ps/mV for all dash numbers.

INPUT SIGNAL CHARACTERISTICS

The frequency and/or pulse width (high or low) of operation may adversely impact the specified delay and increment accuracy of the particular device. The reasons for the dependency of the output delay accuracy on the input signal characteristics are varied and complex. Therefore a recommended maximum and an absolute maximum operating input frequency and a recommended minimum and an absolute minimum operating pulse width have been specified.

OPERATING FREQUENCY

The absolute maximum operating frequency specification, tabulated in Table 1, determines the highest frequency of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable duty cycle

APPLICATION NOTES (CONT'D)

distortion. Exceeding this limit will generally result in no signal output.

The recommended maximum operating frequency specification determines the highest frequency of the delay line input signal for which the output delay accuracy is guaranteed. Exceeding this limit (while remaining within the absolute limit) may cause some delays to shift with respect to their values at low frequency. The amount of delay shift will depend on the degree to which the limit is exceeded.

To guarantee (if possible) the Table 1 delay accuracy for input frequencies higher than the recommended maximum frequency, the 3D7428 must be tested at the user operating frequency. In this case, to facilitate production and device identification, the part number will include a custom reference designator identifying the intended frequency of operation. The programmed delay accuracy of the device is guaranteed, therefore, only at the user specified input frequency. Small input frequency variation about the selected frequency will only marginally impact the programmed delay accuracy, if at all. Contact the factory for details.

OPERATING PULSE WIDTH

The absolute minimum operating pulse width (high or low) specification, tabulated in Table 1, determines the smallest pulse width of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable pulse width distortion. Exceeding this limit will generally result in no signal output.

The recommended minimum operating pulse width (high or low) specification determines the smallest pulse width of the delay line input signal for which the output delay accuracy tabulated in Table 1 is guaranteed. Exceeding this limit (while remaining within the absolute limit) may cause some delays to shift with respect to their values at long pulse width. The amount of delay shift will depend on the degree to which the limit is exceeded.

To guarantee the Table 1 delay accuracy for input pulse width smaller than the recommended minimum operating pulse width, the 3D7428 must be tested at the user operating pulse width. In this case, to facilitate production and device identification, the part number will include a custom reference designator identifying the intended frequency and duty cycle of operation. The programmed delay accuracy of the device is guaranteed, therefore, only for the user specified input characteristics. Small input pulse width variation about the selected pulse width will only marginally impact the programmed delay accuracy, if at all.

PROGRAMMED DELAY UPDATE

A delay line is a memory device. It stores information present at the input for a time equal to the delay setting before presenting it at the output with minimal distortion. The 3D7428 8-bit programmable delay line can be represented by 256 serially connected delay elements (individually addressed by the programming data), each capable of storing data for a time equal to the device increment (step time). The delay line memory property, in conjunction with the operational requirement of "instantaneously" connecting the delay element addressed by the programming data to the output, may inject spurious information onto the output data stream. In order to ensure that spurious outputs do not occur, it is essential that the input signal be idle (held high or low) for a short duration prior to updating the programmed delay. This duration is given by the maximum programmable delay. Satisfying this requirement allows the delay line to "clear" itself of spurious edges. When the new address is loaded, the input signal can begin to switch (and the new delay will be valid) after a time given by $\mathbf{t_{PDV}}$ or $\mathbf{t_{EDV}}$ (see section below).

PROGRAMMING INTERFACE

Figure 1 illustrates the main functional blocks of the 3D7428 delay program interface. Since the 3D7428 is a CMOS design, all unused input pins must be returned to well defined logic levels, VDD or Ground.

TRANSPARENT PARALLEL MODE (MD = 1, AE = 1)

The eight program pins P0 - P7 directly control the output delay. A change on one or more of the program pins will be reflected on the output delay after a time $\mathbf{t_{PDV}}$, as shown in Figure 2. A register is required if the programming data is bused.

APPLICATION NOTES (CONT'D)

LATCHED PARALLEL MODE (MD = 1, AE PULSED)

The eight program pins P0 - P7 are loaded by the falling edge of the Enable pulse, as shown in Figure 3. After each change in delay value, a settling time t_{EDV} is required before the input is accurately delayed.

SERIAL MODE (MD = 0)

While observing data setup (t_{DSC}) and data hold (t_{DHC}) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the clock (SC) while the enable (AE) is high, as shown in Figure 4. The falling edge of the enable (AE) activates the new delay value which is reflected at the output after a settling time t_{EDV}. As data is shifted into the serial data input (SI), the previous contents of the 8-bit input register are shifted out of the serial output port pin (SO) in MSB-to-LSB order, thus allowing cascading of multiple devices by connecting the serial output pin (SO) of the preceding device to the serial data input pin (SI) of the succeeding device, as illustrated in Figure 5. The total number of serial data bits in a cascade configuration must be eight times the number of units, and each group of eight bits must be transmitted in MSB-to-LSB order.

To initiate a serial read, enable (AE) is driven high. After a time t_{EQV} , bit 7 (MSB) is valid at the serial output port pin (SO). On the first rising edge of the serial clock (SC), bit 7 is loaded with the value present at the serial data input pin (SI), while bit 6 is presented at the serial output pin (SO). To retrieve the remaining bits seven more rising edges must be generated on the serial clock line. The read operation is destructive. Therefore, if it is desired that the original delay setting remain unchanged, the read data must be written back to the device(s) before the enable (AE) pin is brought low.

The SO pin, if unused, must be allowed to float if the device is configured in the serial programming mode.

The serial mode is the only mode available on the 8-pin version of the 3D7428.

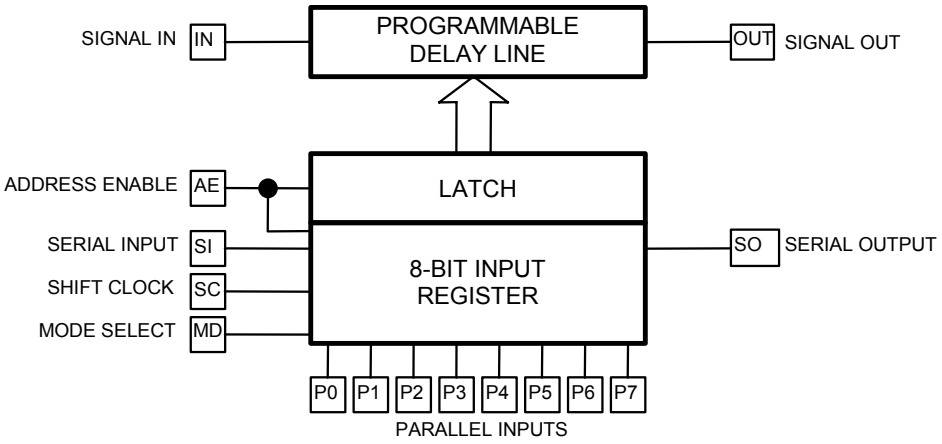


Figure1: Functional block diagram

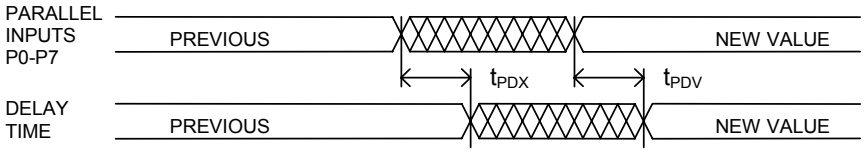


Figure 2: Non-latched parallel mode (MD=1, AE=1)

APPLICATION NOTES (CONT'D)

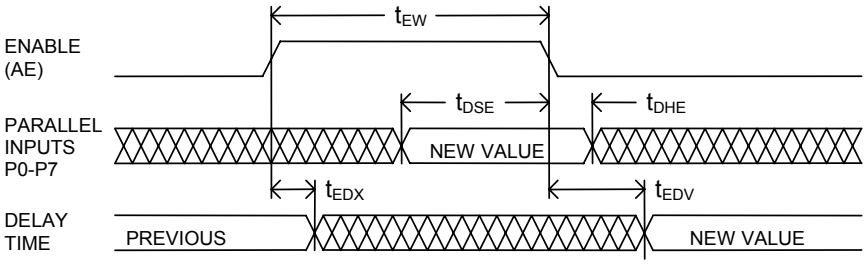


Figure 3: Latched parallel mode (MD=1)

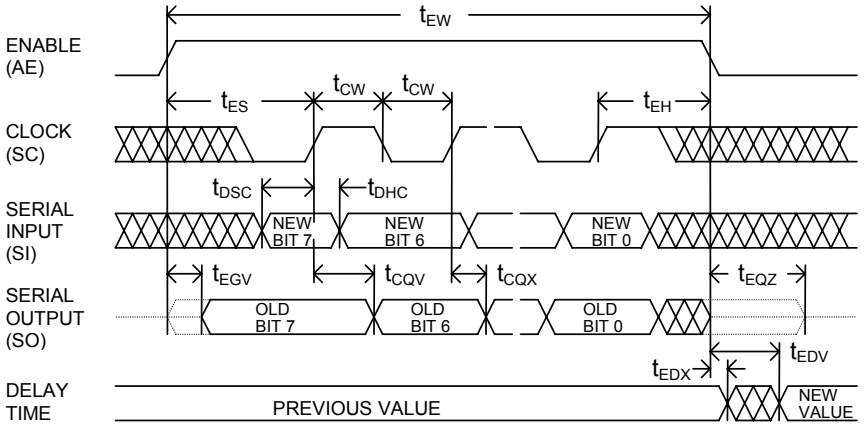


Figure 4: Serial mode (MD=0)

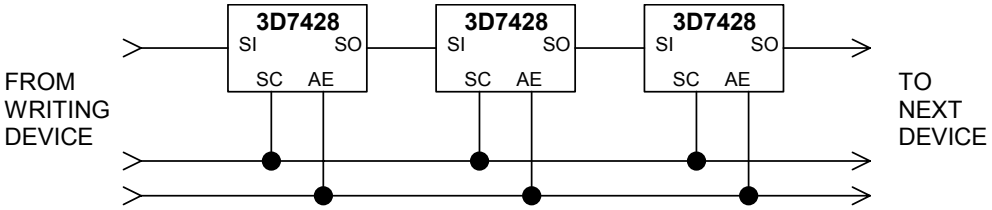


Figure 5: Cascading Multiple Devices

TABLE 2: DELAY VS. PROGRAMMED ADDRESS

	PROGRAMMED ADDRESS								NOMINAL DELAY (NS) PER 3D7428 DASH NUMBER						
PARALLEL	P7	P6	P5	P4	P3	P2	P1	P0							
SERIAL	Msb							Lsb	-0.25	-0.5	-1	-2	-5	-10	-20
STEP 0	0	0	0	0	0	0	0	0	10.50	10.5	10.5	10.5	15	23.5	42
STEP 1	0	0	0	0	0	0	0	1	10.75	11.0	11.5	12.5	20	33.5	62
STEP 2	0	0	0	0	0	0	1	0	11.00	11.5	12.5	14.5	25	43.5	82
STEP 3	0	0	0	0	0	0	1	1	11.25	12.0	13.5	16.5	30	53.5	102
STEP 4	0	0	0	0	0	1	0	0	11.50	12.5	14.5	18.5	35	63.5	122
STEP 5	0	0	0	0	0	1	0	1	11.75	13.0	15.5	20.5	40	73.5	142
STEP 253	1	1	1	1	1	1	0	1	73.75	137.0	263.5	516.5	1280	2553.5	5102
STEP 254	1	1	1	1	1	1	1	0	74.00	137.5	264.5	518.5	1285	2563.5	5122
STEP 255	1	1	1	1	1	1	1	1	74.25	138.0	265.5	520.5	1290	2573.5	5142
CHANGE									63.75	127.5	255.0	510.0	1275	2550.0	5100

DEVICE SPECIFICATIONS

TABLE 3: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-10	10	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 4: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		3.0	5.0	mA	
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}			1.0	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}			1.0	µA	V_{IL} = 0V
High Level Output Current	I_{OH}		-35.0	-4.0	mA	V_{DD} = 4.75V V_{OH} = 2.4V
Low Level Output Current	I_{OL}	4.0	15.0		mA	V_{DD} = 4.75V V_{OL} = 0.4V
Output Rise & Fall Time	T_R & T_F		2.0	2.5	ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/line (pf)
F = Input frequency (GHz)

Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

TABLE 5: AC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_C			80	MHz	
Enable Width	t_{EW}	10			ns	
Clock Width	t_{CW}	10			ns	
Data Setup to Clock	t_{DSC}	10			ns	
Data Hold from Clock	t_{DHC}	3			ns	
Data Setup to Enable	t_{DSE}	10			ns	
Data Hold from Enable	t_{DHE}	3			ns	
Enable to Serial Output Valid	t_{EQV}			20	ns	
Enable to Serial Output High-Z	t_{EQZ}			20	ns	
Clock to Serial Output Valid	t_{CQV}			20	ns	
Clock to Serial Output Invalid	t_{CQX}	10			ns	
Enable Setup to Clock	t_{ES}	10			ns	
Enable Hold from Clock	t_{EH}	10			ns	
Parallel Input Valid to Delay Valid	t_{PDV}		20	40	ns	**1**
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	**1**
Enable to Delay Valid	t_{EDV}		35	45	ns	**1**
Enable to Delay Invalid	t_{EDX}	0			ns	**1**
Input Pulse Width	t_{WI}	8			% of Total Delay	See Table 1
Input Period	Period	20			% of Total Delay	See Table 1
Input to Output Delay	t_{PLH}, t_{PHL}				ns	See Table 2

NOTES: 1 - Refer to **PROGRAMMED DELAY UPDATE** section

SILICON DELAY LINE AUTOMATED TESTING

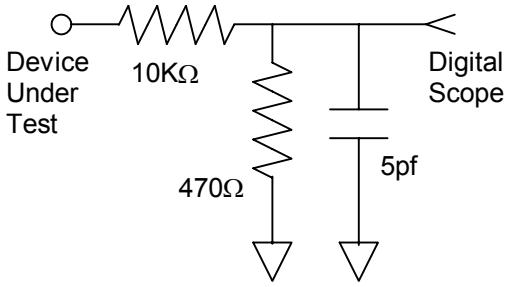
TEST CONDITIONS

INPUT:

Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 5.0V ± 0.1V
Input Pulse: High = 3.0V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width: PW_{IN} = 1.25 x Total Delay
Period: PER_{IN} = 2.5 x Total Delay

OUTPUT:

R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

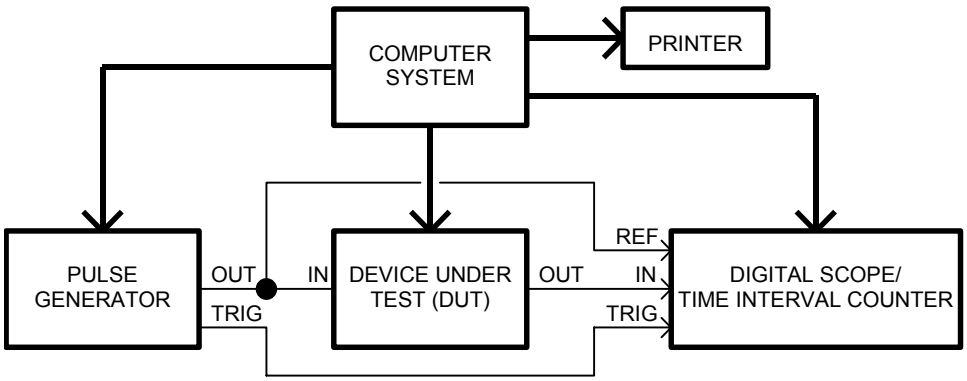


Figure 6: Test Setup

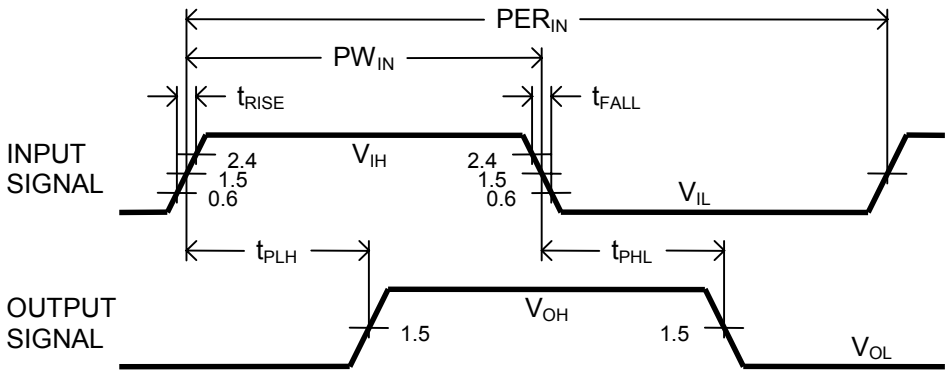


Figure 7: Timing Diagram