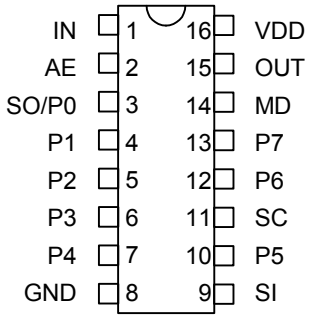
MONOLITHIC 8-BIT PROGRAMMABLE DELAY LINE (SERIES 3D3418 – LOW NOISE)

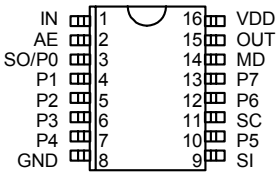
FEATURES

- All-silicon, low-power 3.3V CMOS technology
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP pkg.)
- Low ground bounce noise
- Leading- and trailing-edge accuracy
- **Increment range:** 0.25 through 7.5ns
- **Delay tolerance:** 1% (See Table 1)
- **Temperature stability:** ±3% typical (0C-70C)
- **Vdd stability:** ±1% typical (3.0V-3.6V)
- **Static Idd:** 1.3ma typical
- **Minimum input pulse width:** 10% of total delay
- Programmable via 3-wire serial or 8-bit parallel interface

PACKAGES



3D3418 DIP
3D3418G Gull Wing



3D3418S SOL
(300 Mil)

For mechanical dimensions, click here.

FUNCTIONAL DESCRIPTION

The 3D3418 Programmable 8-Bit Silicon Delay Line product family consists of 8-bit, user-programmable CMOS silicon integrated circuits. Delay values, programmed either via the serial or parallel interface, can be varied over 255 equal steps ranging from 250ps to 7.5ns inclusively. Units have a typical inherent (address 0) delay of 20ns (See Table 1). The input is reproduced at the output without inversion, shifted in time as per user selection. The 3D3418 is CMOS-compatible, and features both rising- and falling-edge accuracy.

The all-CMOS 3D3418 integrated circuit has been designed as a reliable, economic alternative to hybrid TTL programmable delay lines. It is offered in a standard 16-pin auto-insertable DIP and a space saving surface mount 16-pin SOIC.

PIN DESCRIPTIONS

IN	Signal Input
OUT	Signal Output
MD	Mode Select
AE	Address Enable
P0-P7	Parallel Data Input
SC	Serial Clock
SI	Serial Data Input
SO	Serial Data Output
VDD	+3.3 Volts
GND	Ground

TABLE 1: PART NUMBER SPECIFICATIONS

PART NUMBER	DELAYS AND TOLERANCES			INPUT RESTRICTIONS			
	Step 0 Delay (ns)	Step 255 Delay (ns)	Delay Increment (ns)	Max Operating Frequency	Absolute Max Oper Freq	Min Operating P.W.	Absolute Min Oper P.W.
3D3418-0.25	19.5 ± 3.0	83.25 ± 4.0	0.25 ± 0.15	6.25 MHz	90 MHz	80.0 ns	5.5 ns
3D3418-0.5	19.5 ± 3.0	147.0 ± 4.0	0.50 ± 0.25	3.15 MHz	45 MHz	160.0 ns	11.0 ns
3D3418-1	19.5 ± 3.0	274.5 ± 5.0	1.00 ± 0.50	1.56 MHz	22 MHz	320.0 ns	22.0 ns
3D3418-2	20.0 ± 3.5	530.0 ± 6.0	2.00 ± 1.00	0.78 MHz	11 MHz	640.0 ns	44.0 ns
3D3418-3	20.0 ± 3.5	785.0 ± 8.0	3.00 ± 1.50	0.52 MHz	7.5 MHz	960.0 ns	66.0 ns
3D3418-4	20.0 ± 3.5	1040 ± 9.0	4.00 ± 2.00	0.39 MHz	5.5 MHz	1280.0 ns	88.0 ns
3D3418-5	20.0 ± 3.5	1295 ± 10	5.00 ± 2.50	0.31 MHz	4.4 MHz	1600.0 ns	110.0 ns
3D3418-7.5	20.5 ± 3.5	1933 ± 15	7.50 ± 3.75	0.21 MHz	2.9 MHz	2400.0 ns	165.0 ns

NOTES: Any delay increment between 0.25 and 7.5 ns not shown is also available.
All delays referenced to input pin

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APPLICATION NOTES

The 8-bit programmable 3D3418 delay line architecture is comprised of a number of delay cells connected in series with their respective outputs multiplexed onto the Delay Out pin (OUT) by the user-selected programming data. Each delay cell produces at its output a replica of the signal present at its input, shifted in time.

INPUT SIGNAL CHARACTERISTICS

The Frequency and/or Pulse Width (high or low) of operation may adversely impact the specified delay and increment accuracy of the particular device. The reasons for the dependency of the output delay accuracy on the input signal characteristics are varied and complex. Therefore a **Maximum** and an **Absolute Maximum** operating input frequency and a **Minimum** and an **Absolute Minimum** operating pulse width have been specified.

OPERATING FREQUENCY

The **Absolute Maximum Operating Frequency** specification, tabulated in **Table 1**, determines the highest frequency of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable duty cycle distortion.

The **Maximum Operating Frequency** specification determines the highest frequency of the delay line input signal for which the output delay accuracy is guaranteed.

To guarantee the **Table 1** delay accuracy for input frequencies higher than the **Maximum Operating Frequency**, the 3D3418 must be tested at the user operating frequency. Therefore, to facilitate production and device identification, **the part number will include a custom reference designator** identifying the intended frequency of operation. The programmed delay accuracy of the device is guaranteed, therefore, only at the user specified input frequency. Small input frequency variation about the selected frequency will only marginally impact the programmed delay accuracy, if at all. **Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.**

OPERATING PULSE WIDTH

The **Absolute Minimum Operating Pulse Width** (high or low) specification, tabulated in **Table 1**, determines the smallest Pulse Width of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable pulse width distortion.

The **Minimum Operating Pulse Width** (high or low) specification determines the smallest Pulse Width of the delay line input signal for which the output delay accuracy tabulated in **Table 1** is guaranteed.

To guarantee the **Table 1** delay accuracy for input pulse width smaller than the **Minimum Operating Pulse Width**, the 3D3418 must be tested at the user operating pulse width. Therefore, to facilitate production and device identification, the **part number will include a custom reference designator** identifying the intended frequency and duty cycle of operation. The programmed delay accuracy of the device is guaranteed, therefore, only for the user specified input characteristics. Small input pulse width variation about the selected pulse width will only marginally impact the programmed delay accuracy, if at all. **Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.**

SPECIAL HIGH ACCURACY REQUIREMENTS

The **Table 1** delay and increment accuracy specifications are aimed at meeting the requirements of the majority of the applications encountered to date. However, some systems may place tighter restrictions on one accuracy parameter in favor of others. For example, a channel delay equalizing system is concerned in minimizing delay variations among the various channels. Therefore, because the inter channel skew is a delay difference, the programmed delay tolerance may need to be considerably decreased, while the increment and its tolerance are of no consequence. The opposite is true for an under-sampled multi-channel data acquisition system.

APPLICATION NOTES (CONT'D)

The flexible 3D3418 architecture can be exploited to conform to these more demanding user-dictated accuracy constraints. However, to facilitate production and device identification, **the part number will include a custom reference designator** identifying the user requested accuracy specifications and operating conditions. **It is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.**

POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The monolithic 3D3418 programmable delay line utilizes novel and innovative compensation circuitry to minimize the delay variations induced by fluctuations in power supply and/or temperature.

The **thermal coefficient** is reduced to **600 PPM/C**, which is equivalent to a variation, over the 0C-70 C operating range, of **±3%** from the room-temperature delay settings. The **power supply coefficient** is reduced, over the 3.0V-3.6V operating range, to **±1%** of the delay settings at the nominal 3.3VDC power supply and/or **±2ns**, whichever is greater.

It is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred.

PROGRAMMED DELAY (ADDRESS) UPDATE

A delay line is a memory device. It stores information present at the input for a time equal to the delay setting before presenting it at the output with minimal distortion. The 3D3418 8-bit programmable delay line can be represented by 256 serially connected delay elements (individually **addressed** by the programming data), each capable of storing data for a time equal to the device increment (step time). The delay line memory property, in conjunction with the operational requirement of "instantaneously" connecting the delay element addressed by the programming data to the output, may inject spurious information onto the output data stream.

In order to ensure that spurious outputs do not occur, it is essential that the input signal be idle (held high or low) for a short duration prior to updating the programmed delay. This duration is given by the maximum programmable delay. Satisfying this requirement allows the delay line to "clear" itself of spurious edges. When the new address is loaded, the input signal can begin to switch (and the new delay will be valid) after a time given by $\mathbf{t_{PDV}}$ or $\mathbf{t_{EDV}}$ (see section below).

PROGRAMMED DELAY (ADDRESS) INTERFACE

Figure 1 illustrates the main functional blocks of the 3D3418 delay program interface. Since the 3D3418 is a CMOS design, all unused input pins must be returned to well defined logic levels, VCC or Ground.

TRANSPARENT PARALLEL MODE (MD = 1, AE = 1)

The eight program pins P0 - P7 directly control the output delay. A change on one or more of the program
pins will be reflected on the output delay after a time $\mathbf{t_{PDV}}$, as shown in **Figure 2**. A register is required if the programming data is bused.

LATCHED PARALLEL MODE (MD = 1, AE PULSED)

The eight program pins P0 - P7 are loaded by the falling edge of the Enable pulse, as shown in **Figure 3**. After each change in delay value, a settling time $\mathbf{t_{EDV}}$ is required before the input is accurately delayed.

SERIAL MODE (MD = 0)

While observing data setup ($\mathbf{t_{DSC}}$) and data hold ($\mathbf{t_{DHC}}$) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the clock (SC) while the enable (AE) is high, as shown in **Figure 4**. The falling edge of the enable (AE) activates the new delay value which is reflected at the output after a settling time $\mathbf{t_{EDV}}$. As data is shifted into the serial data input (SI), the previous contents of the 8-bit input register are shifted out of the serial output port pin (SO) in MSB-to-LSB order, thus allowing cascading of multiple devices by connecting the serial output pin (SO) of the preceding device to the serial data input

APPLICATION NOTES (CONT'D)

pin (SI) of the succeeding device, as illustrated in **Figure 5**. The total number of serial data bits in a cascade configuration must be eight times the number of units, and each group of eight bits must be transmitted in MSB-to-LSB order.

To initiate a serial read, enable (AE) is driven high. After a time $\mathbf{t_{EQV}}$, bit 7 (MSB) is valid at the serial output port pin (SO). On the first rising edge of the serial clock (SC), bit 7 is loaded with the value present at the serial data input pin (SI), while bit 6 is presented at the serial output pin (SO). To retrieve the remaining bits seven more rising edges must be generated on the serial clock line. The read operation is destructive. Therefore, if it is desired that the original delay setting remain unchanged, the read data must be written back to the device(s) before the enable (AE) pin is brought low.

Pin 3, if unused, **must be allowed to float** if the device is configured in the serial programming mode.

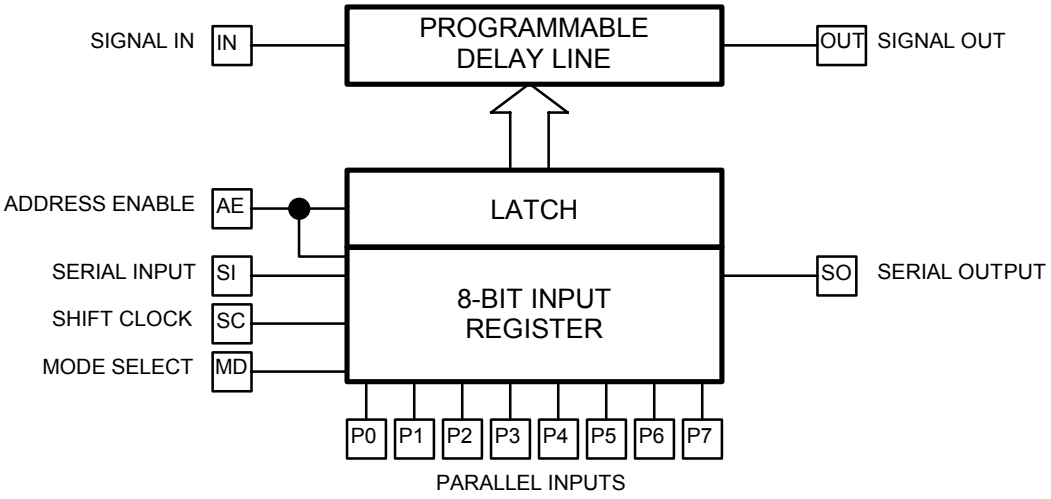


Figure1: Functional block diagram

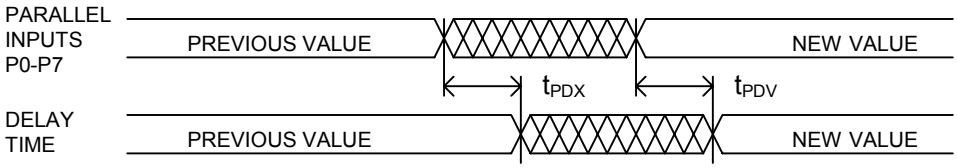


Figure 2: Non-latched parallel mode (MD=1, AE=1)

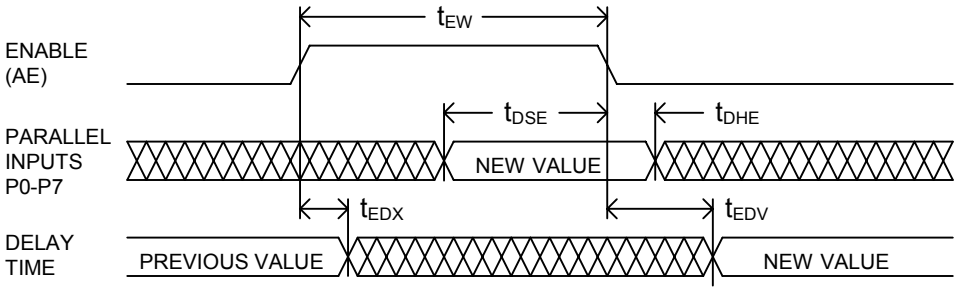


Figure 3: Latched parallel mode (MD=1)

APPLICATION NOTES (CONT'D)

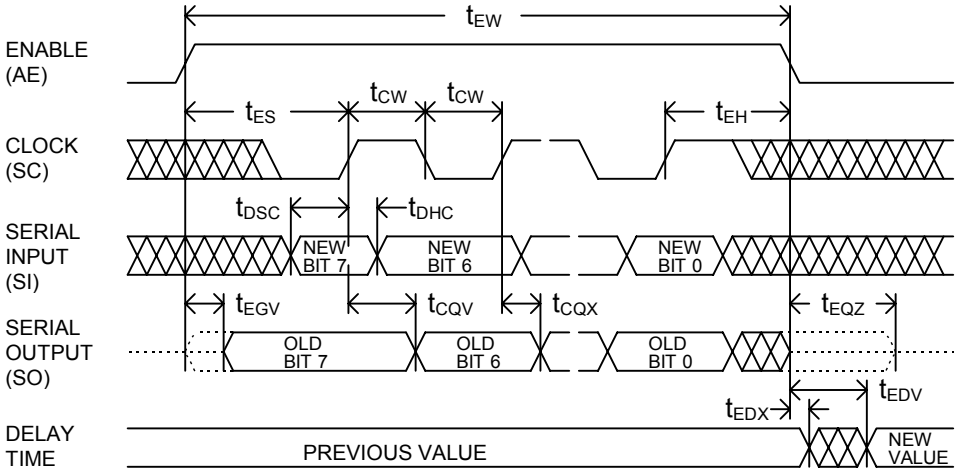


Figure 4: Serial mode (MD=0)

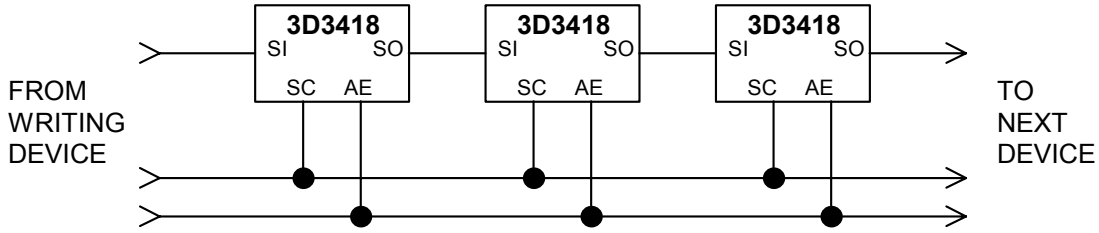


Figure 5: Cascading Multiple Devices

TABLE 2: DELAY VS. PROGRAMMED ADDRESS

	PROGRAMMED ADDRESS								NOMINAL DELAY (NS)				
PARALLEL	P7	P6	P5	P4	P3	P2	P1	P0	3D3418 DASH NUMBER				
SERIAL	Msb							Lsb	-.25	-.5	-1	-2	-5
STEP 0	0	0	0	0	0	0	0	0	19.50	19.5	19.5	20	20
STEP 1	0	0	0	0	0	0	0	1	19.75	20.0	20.5	22	25
STEP 2	0	0	0	0	0	0	1	0	20.00	20.5	21.5	24	30
STEP 3	0	0	0	0	0	0	1	1	20.25	21.0	22.5	26	35
STEP 4	0	0	0	0	0	1	0	0	20.50	21.5	23.5	28	40
STEP 5	0	0	0	0	0	1	0	1	20.75	22.0	24.5	30	45
STEP 253	1	1	1	1	1	1	0	1	82.75	146.0	272.5	526	1285
STEP 254	1	1	1	1	1	1	1	0	83.00	146.5	273.5	528	1290
STEP 255	1	1	1	1	1	1	1	1	83.25	147.0	274.5	530	1295
DELAY CHANGE									63.75	127.5	255	510	1275

DEVICE SPECIFICATIONS

TABLE 3: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-10	10	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 4: DC ELECTRICAL CHARACTERISTICS

(0C to 70C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		1.3	2.0	mA	V_{DD} = 3.6V
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}	-0.1	0.0	0.1	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}	-0.1	0.0	0.1	µA	V_{IL} = 0V
High Level Output Current	I_{OH}		-8.0	-6.0	mA	V_{DD} = 3.0V V_{OH} = 2.4V
Low Level Output Current	I_{OL}	6.0	7.5		mA	V_{DD} = 3.0V V_{OL} = 0.4V
Output Rise & Fall Time	T_R & T_F		2		ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/line (pf)
F = Input frequency (GHz)

Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

TABLE 5: AC ELECTRICAL CHARACTERISTICS

(0C to 70C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_C			80	MHz	
Enable Width	t_{EW}	10			ns	
Clock Width	t_{CW}	10			ns	
Data Setup to Clock	t_{DSC}	10			ns	
Data Hold from Clock	t_{DHC}	3			ns	
Data Setup to Enable	t_{DSE}	10			ns	
Data Hold from Enable	t_{DHE}	3			ns	
Enable to Serial Output Valid	t_{EQV}			20	ns	
Enable to Serial Output High-Z	t_{EQZ}			20	ns	
Clock to Serial Output Valid	t_{CQV}			20	ns	
Clock to Serial Output Invalid	t_{CQX}	10			ns	
Enable Setup to Clock	t_{ES}	10			ns	
Enable Hold from Clock	t_{EH}	10			ns	
Parallel Input Valid to Delay Valid	t_{PDV}		20	40	ns	**1**
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	**1**
Enable to Delay Valid	t_{EDV}		35	45	ns	**1**
Enable to Delay Invalid	t_{EDX}	0			ns	**1**
Input Pulse Width	t_{WI}	8			% of Total Delay	See Table 1
Input Period	Period	20			% of Total Delay	See Table 1
Input to Output Delay	t_{PLH}, t_{PHL}				ns	See Table 2

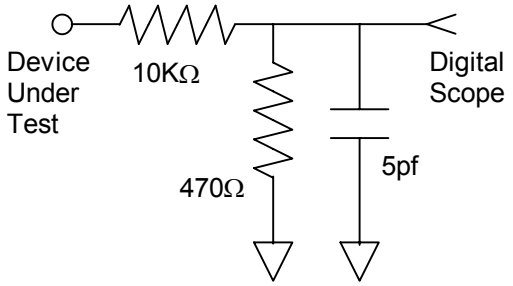
NOTES: 1 - Refer to **PROGRAMMED DELAY (ADDRESS) UPDATE** section

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 3.3V ± 0.1V
Input Pulse: High = 3.3V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V
)
Pulse Width: PW_{IN} = 1.25 x Total Delay
Period: PER_{IN} = 2.5 x Total Delay

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

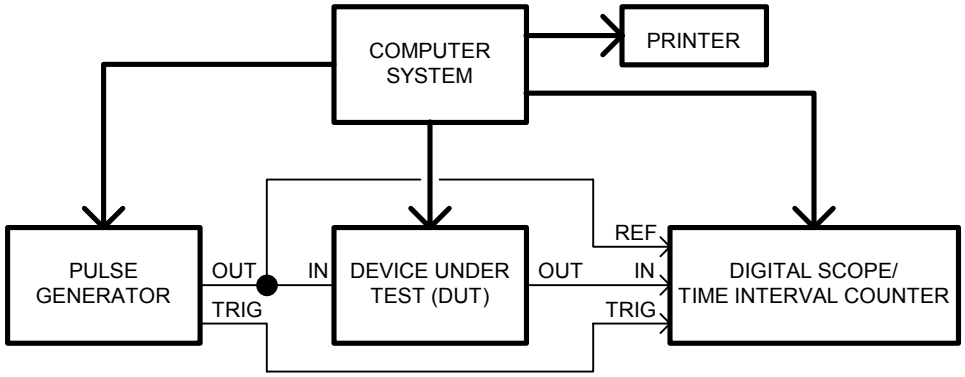


Figure 6: Test Setup

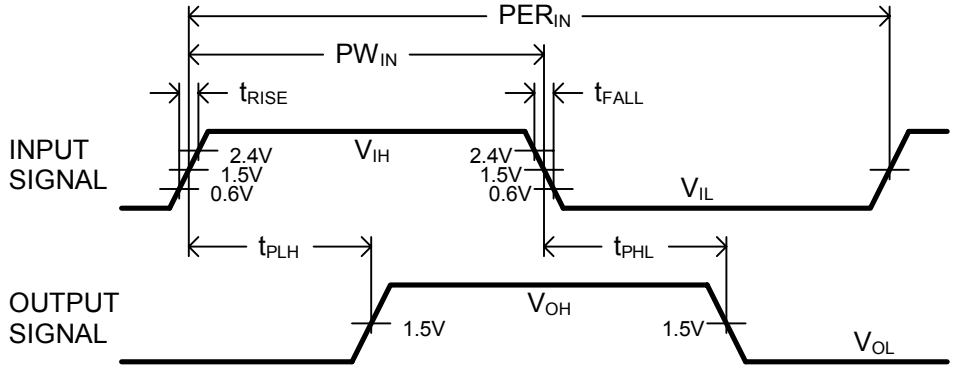


Figure 7: Timing Diagram