CAT34RC02

2-kb I²C Serial EEPROM, Serial Presence Detect

FEATURES

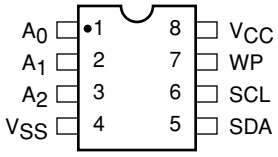
- 400 kHz I²C bus compatible*
- 1.7 to 5.5 volt operation
- 16-byte page write buffer
- Hardware write protection for entire memory
- Permanent and reversible software write protection for lower 128 bytes
- Schmitt trigger on SCL and SDA inputs
- Low power CMOS technology
- 1,000,000 program/erase cycles
- 100 year data retention
- 8-pin DIP, SOIC, TSSOP and TDFN packages
- Industrial and extended temperature ranges

DESCRIPTION

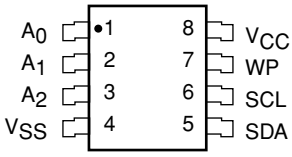
The CAT34RC02 is a 2-kb Serial CMOS EEPROM internally organized as 256 words of 8 bits each. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT34RC02 features a 16-byte page write buffer. The device operates via the I²C bus serial interface and is available in 8-pin DIP, SOIC, TSSOP and TDFN packages.

PIN CONFIGURATION

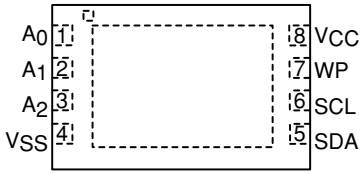
DIP Package (P, L)



SOIC Package (J, W)



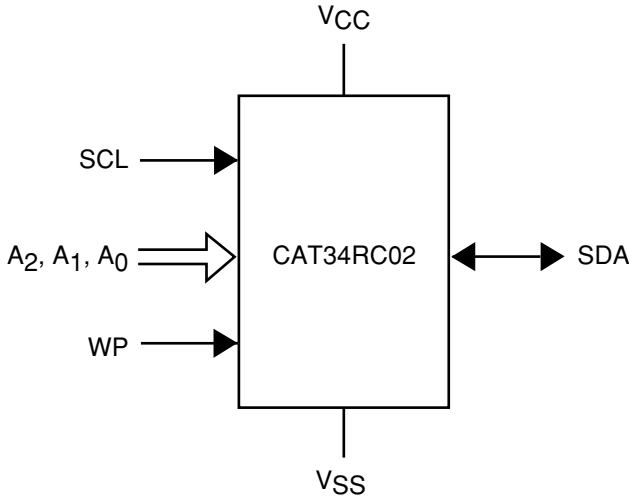
TDFN Package (SP2, VP2)



TSSOP Package (U, Y)



FUNCTIONAL SYMBOL



PIN FUNCTIONS

Pin Name	Function
A_0, A_1, A_2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{CC}	1.7 V to 5.5 V Power Supply
V_{SS}	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

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Doc No. 1052, Rev. K

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... -2.0 V to V_{CC} + 2.0 V

Voltage on A_0 ..... -2.0 V to +12.0 V

V_{CC} with Respect to V_{SS} ..... -2.0 V to +7.0 V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Units
N_{END}(2)(*)	Endurance	MIL-STD-883, Test Method 1033	1,000,000	Program/ Erase Cycles
T_{DR}(2)(*)	Data Retention	MIL-STD-883, Test Method 1008	100	Years
V_{ZAP}(2)(*)	ESD Susceptibility	MIL-STD-883, Test Method 3015	4000	Volts
I_{LTH}(2)(3)	Latch-up	JEDEC Standard 17	100	mA

(*) Page Mode, VCC = 5 V, 25°C

D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.7 V to 5.5 V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current (Read)	f_{SCL} = 100 kHz			1	mA
I_{CC}	Power Supply Current (Write)	f_{SCL} = 100 kHz			3	mA
I_{SB}(4)	Standby Current (V_{CC} = 5.0 V)	V_{IN} = GND or V_{CC}			1	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			1	µA
V_{IL}	Input Low Voltage		–1		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 1.0	V
V_{OL1}	Output Low Voltage (V_{CC} = 3.0 V)	I_{OL} = 3 mA			0.4	V
V_{OL2}	Output Low Voltage (V_{CC} = 1.7 V)	I_{OL} = 1.5 mA			0.5	V
V_{HV}	RSWP Set/Clear Overdrive A_0 High Voltage	V_{HV} - V_{CC} > 4.8 V	7		10	V

CAPACITANCE T_A = 25°C, f = 400 kHz, V_{CC} = 5 V

Symbol	Test	Conditions	Min	Typ	Max	Units
$C_{I/O}$(2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0 V			8	pF
C_{IN}(2)	Input Capacitance (other pins)	V_{IN} = 0 V			6	pF
Z_{WPL}	WP Input Impedance	V_{IN} < 0.5 V	5		70	kΩ
Z_{WPH}	WP Input Impedance	V_{IN} > V_{CC} x 0.7	500			kΩ

Note:

(1) The DC input voltage on any pin should not be lower than -0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -2.0 V or overshoot to no more than VCC + 2.0 V, for periods of less than 20 ns. The maximum DC voltage on address pin A_0 is +12.0 V.

(2) This parameter is tested initially and after a design or process change that affects the parameter.

(3) Latch-up protection is provided for stresses up to 100 mA on I/O pins from -1.0 V to V_{CC} + 1.0 V.

(4) Standby Current, I_{SB} = 10 µA max at extended temperature range.

A.C. CHARACTERISTICS

V_{CC} = 1.7 V to 5.5 V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	1.7 V - 5.5 V		2.5 V - 5.5 V		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
T_I(1)	Noise Suppression Time Constant at SCL, SDA Inputs		100		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		0.9	µs
t_{BUF}(1)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.3		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R(1)	SDA and SCL Rise Time		1		0.3	µs
t_F(1)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns

Power-Up Timing(1)(2)

Symbol	Parameter	Min	Typ	Max	Units
t_{PUR}	Power-up to Read Operation			1	ms
t_{PUW}	Power-up to Write Operation			1	ms

Write Cycle Limits

Symbol	Parameter	Min	Typ	Max	Units
t_{WR}	Write Cycle Time			5	ms

The write cycle time is the time elapsed between the STOP command (following the write instruction) and the completion of the internal write cycle. During the internal write cycle, SDA is released by the Slave and the device does not acknowledge external commands.

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT34RC02 supports the I^2C (2-wire) Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. Data transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT34RC02 operates as a Slave device. Both the Master and Slave devices can operate as either transmitter or receiver, but the Master alone assigns those roles. A maximum of 8 devices may be connected to the bus as determined by the device address inputs A_0, A_1, and A_2.

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input pin is used to clock all data transfers into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer data into and out of the device. This pin is an open drain output in transmit mode.

A_0, A_1, A_2: Device Address Inputs
These inputs set the device address. When left floating, the address pins are internally pulled to ground.

WP: Write Protect

This input, when grounded or left floating, allows write operations to the entire memory. When this pin is tied to V_{CC}, the entire memory is write protected.

Figure 1. Bus Timing

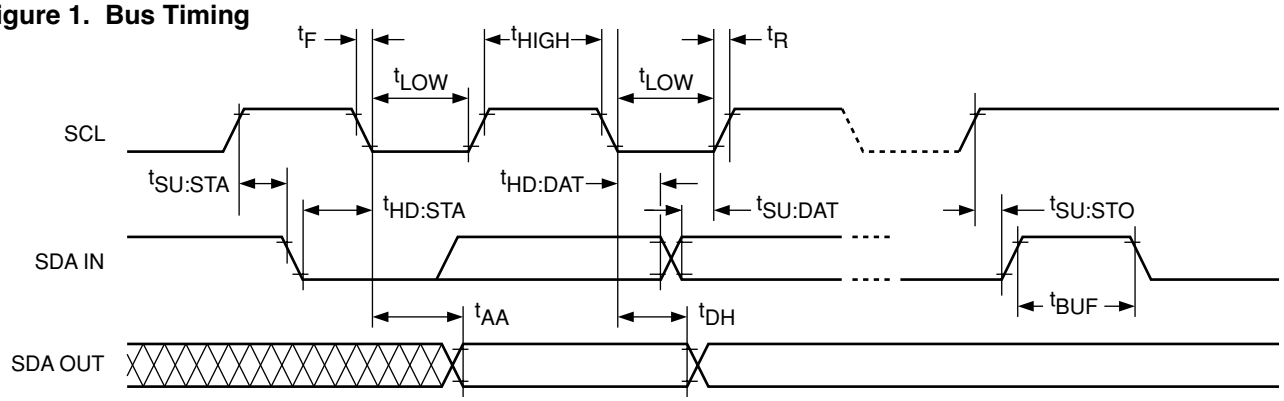


Figure 2. Write Cycle Timing

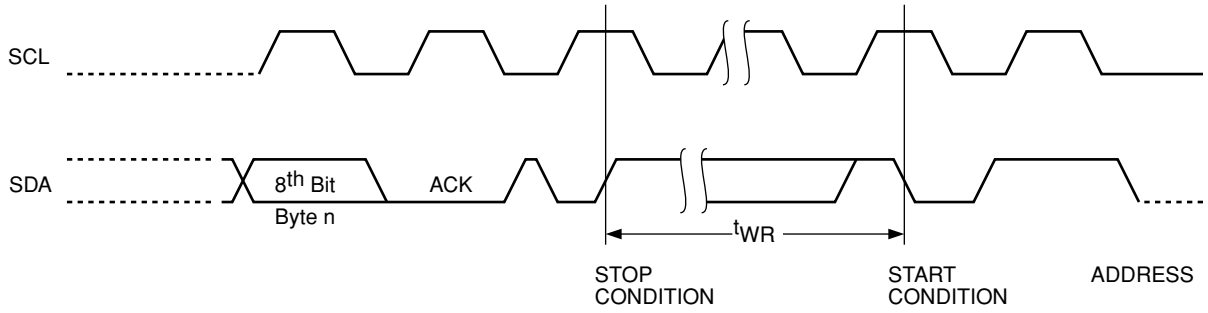
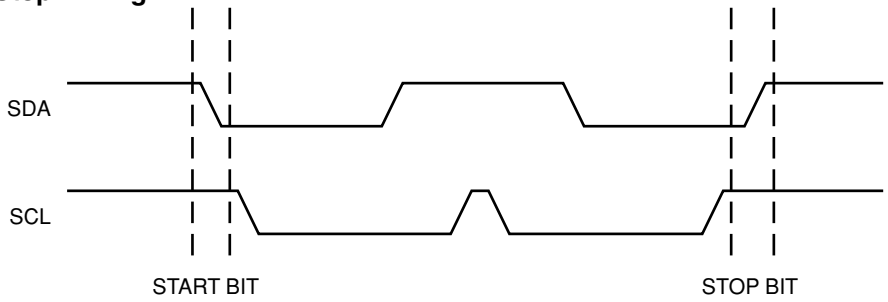


Figure 3. Start/Stop Timing



I²C BUS PROTOCOL

The I²C bus consists of two 'wires', SCL and SDA. The two 'wires' are connected to the supply (V_{CC}) via pull-up resistors. Master and Slave devices connect to the bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

(1) Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

(2) During a data transfer, the data line must remain stable whenever the SCL line is high. An SDA transition while SCL is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START condition acts as a 'wake-up' call for the Slave devices. A Slave will not respond to commands unless the MASTER generates a START condition.

STOP Condition

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP condition starts the internal write cycle, when following a WRITE command and sends the Slave into standby mode, when following a READ command.

Device Addressing

The Master initiates a data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The four most significant bits of the Slave address (the 'preamble') are fixed to 1010 (Ah), for normal read/write operations and 0110 (6h) for Software Write Protect (SWP) operations (Fig. 5). The next three bits, A_2, A_1 and A_0, select one of eight possible Slave devices. The last bit, R/$\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle. The Slave will aslo acknowledge the 8-bit byte address and every data byte presented in WRITE mode. In READ mode the Slave shifts out eight bits of data, and then 'releases' the SDA line durng the 9th clock cycle. If the Master acknowledges in the 9th clock cycle (by pulling down the SDA line), then the Slave continues transmitting. When data transfer is complete, the Master responds with a NoACK (it does not acknowledge the last data byte) and the Slave stops transmitting and waits for a STOP condition.

Figure 4. Acknowledge Timing

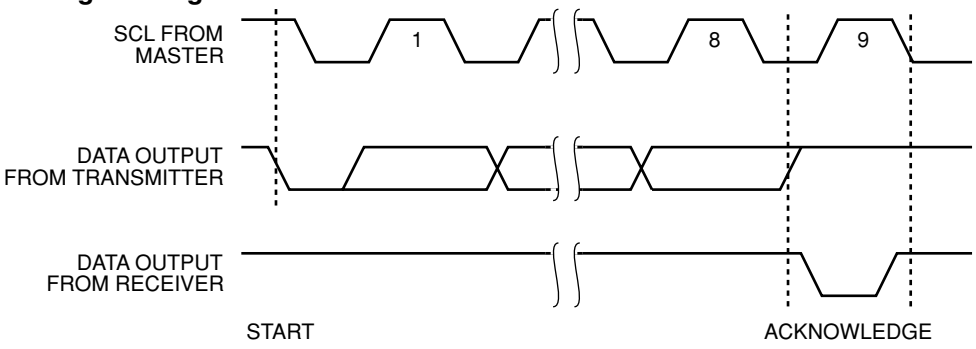
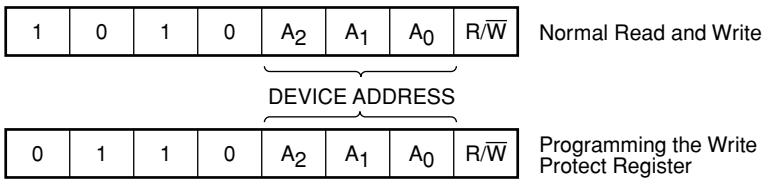


Figure 5. Slave Address Bits



WRITE OPERATIONS

Byte Write

In Byte Write mode the Master creates a START condition, and then broadcasts the Slave address, byte address and data to be written. The Slave acknowledges the three bytes by pulling down the SDA line during the 9th clock cycle following each byte. The Master creates a STOP condition after the last ACK from the Slave, which then starts the internal write operation (Fig. 6). During internal write, the Slave will ignore any read/write request from the Master.

Page Write

The CAT34RC02 contains 256 bytes of data, arranged in 16 pages of 16 bytes each. The page is selected by the four most significant bits of the address byte presented to the device after the Slave address, while the four least significant bits point to the byte within the page. By 'loading' more than one data byte into the device, up to an entire page can be written in one write cycle (Fig. 7). The internal byte address counter will increment after each data byte. If the Master transmits more than 16 data bytes, then earlier bytes will be overwritten by later bytes in a 'wrap-around' fashion within the selected page. The internal write cycle is started following the STOP condition created by the Master.

Acknowledge Polling

Acknowledge polling can be used to determine if the CAT34RC02 is busy writing or is ready to accept commands. Polling is implemented by sending a 'Selective Read' command (described under READ OPERATIONS) to the device. The CAT34RC02 will not acknowledge the Slave address, as long as internal write is in progress.

WRITE PROTECTION

Hardware Write Protection

With the WP pin held HIGH, the entire memory, as well as the SWP flags are protected against WRITE operations (Fig. 9). If the WP pin is left floating or is grounded. then it has no impact on the operation of the CAT34RC02.

Software Write Protection

The lower half of memory (first 128 bytes) can be protected against WRITE operations by setting one of two Software Write Protection (SWP) flags/switches. The PSWP (Permanent Software Write Protection) flag can be set but not cleared by the user. The RSWP (Reversible Software Write Protection) flag can be set and cleared by the user. Whereas the PSWP flag can be set 'in-system', the RSWP flag is meant to be used during testing. RSWP commands require the presence of a very high voltage (higher than VCC) on address pin A_0 and fixed logic levels for the other two address pins.

The CAT34RC02 is shipped 'unprotected'. The state of the SWP flags can be read by issuing an 'Immediate Address Read' command, with the Slave address 'preamble' set to 0110 (6h) instead of the 'normal' 1010 (Ah). A SWP READ will return the complemented versions of the two flags in the last two slots of the resulting data byte; the other six more significant bits in the data byte have no meaning to the user (Fig. 11).

Figure 6. Byte Write Timing

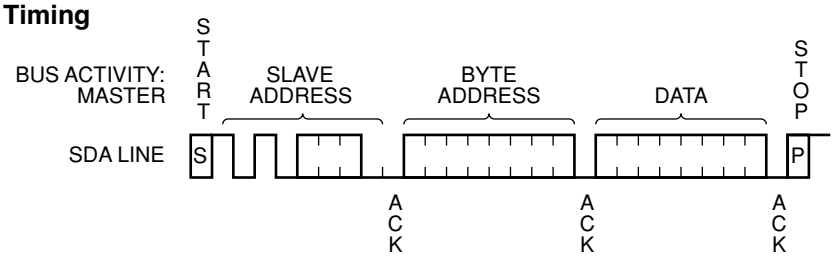
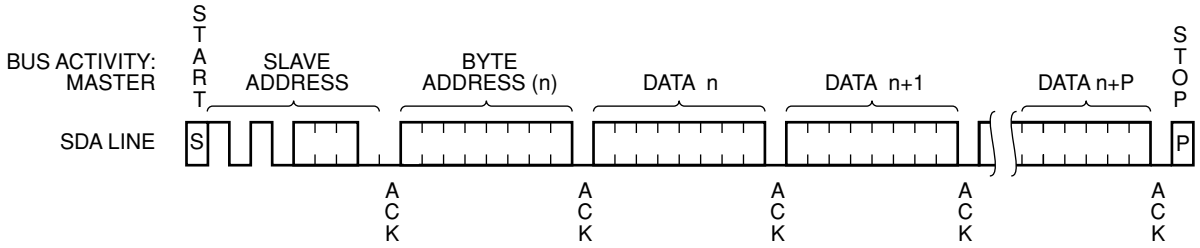


Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

The PSWP flag can be set (forever) by issuing a 'Byte Write' command, with the Slave address preamble set to '6h', followed by a 'don't care' address, followed by 'don't care' data and a STOP condition. The CAT34RC02 will acknowledge the Slave address, dummy byte address and dummy data (Fig. 10). The PSWP flag will be permanently set (after the internal write cycle is completed).

The SWP commands are shown in Table 1.

Table 1. SWP Commands

				Slave Address							
	PIN			Preamble				Device Address			R/$\overline{W}$
Command	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
SWP READ	A2	A1	A0	0	1	1	0	A2	A1	A0	1
RSWP SET	0	0	VHV	0	1	1	0	0	0	1	0
RSWP CLEAR	0	1	VHV	0	1	1	0	0	1	1	0
PSWP SET	A2	A1	A0	0	1	1	0	A2	A1	A0	0

The CAT34RC02 will not acknowledge RSWP or PSWP commands, once the PSWP flag is set. If the PSWP flag is not set, but the WP pin is HIGH, then the CAT34RC02 will react to RSWP or PSWP commands as follows: if the command attempts to 'flip' one of the two SWP switches, then the CAT34RC02 will respond the same way the regular memory would, i.e. the command and address (in this case dummy) are acknowledged, but the data (in this case dummy) will not be acknowledged; if the command attempts to 'reaffirm' one of the two switches, then the CAT34RC02 will not acknowledge the command itself. In addition, the CAT34RC02 will not acknowledge a 'reaffirming' SWP command, even if the WP pin is LOW.

Power-On Reset (POR)

The CAT34RC02 incorporates Power-On Reset (POR) circuitry which protects the device against malfunctioning while V_{CC} is lower than the recommended operating voltage.

The device will power up into a read-only state and will power-down into a reset state when V_{CC} crosses the POR level of ~1.3V.

READ OPERATIONS

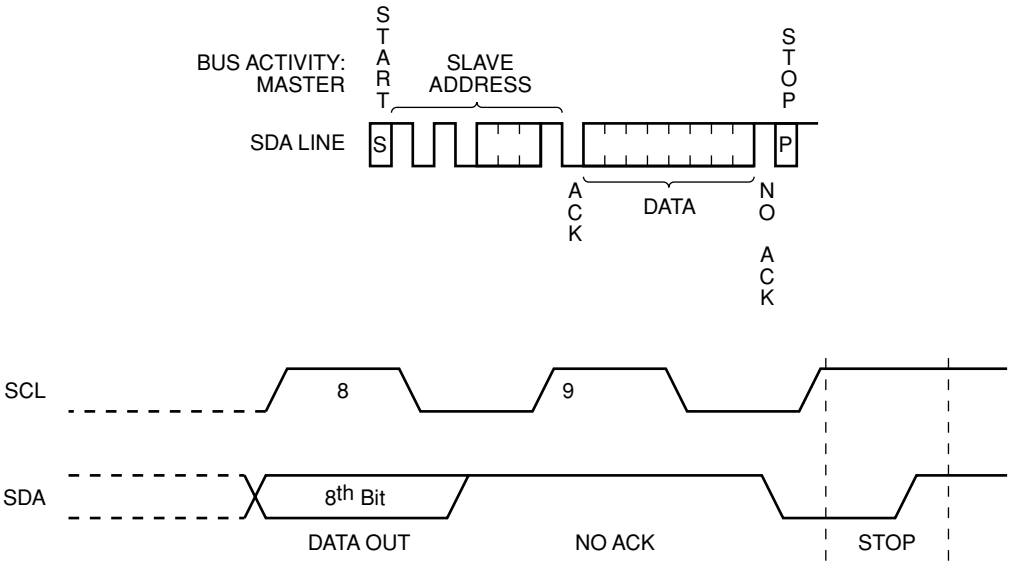
Immediate Address Read

In standby mode, the CAT34RC02 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If the 'previous' byte was the last byte in memory, then the address counter will point to the first memory byte, etc. If the CAT34RC02 decodes a Slave address with a '1' in the R/$\overline{W}$ bit position (Fig. 8), it will issue an ACK in the 9th clock cycle, and will then transmit the data byte being pointed at by the address counter. The Master can then stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read

The READ operation can also be started at an address different from the one stored in the address counter. The

Figure 8. Immediate Address Read Timing



address counter can be 'initialized' by performing a 'dummy' WRITE operation (Fig. 12). The START condition is followed by the Slave address (with the R/$\overline{W}$ bit set to '0') and the desired byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the 'Immediate Address Read' sequence, as described earlier.

Sequential Read

If the Master acknowledges the 1st data byte transmitted by the CAT34RC02, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Fig. 13). If the end of memory is reached during sequential READ, the address counter will 'wrap-around' to the beginning of memory, etc. Sequential READ works with either 'Immediate Address Read' or 'Selective Read', the only difference being the starting byte address.

Figure 9. Memory Array

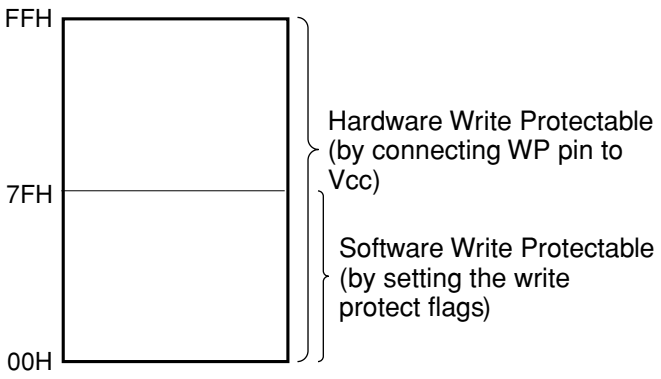
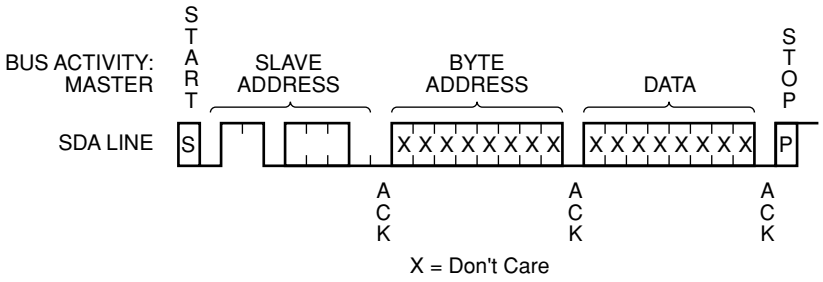


Figure 10. Software Write Protect (Write)



* For PSWP A_0 is at normal CMOS levels and for RSWP, A_0 is at V_{HV} which must be held high beyond the end of the STOP condition (approximately 1μs of "overlap" is sufficient).

Figure 11. Software Write Protect (Read)

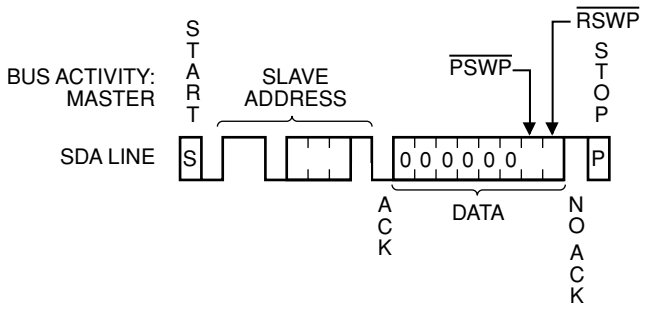


Figure 12. Selective Read Timing

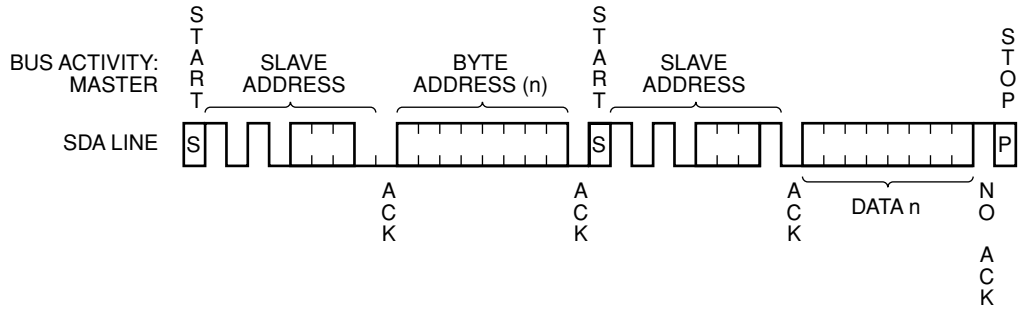
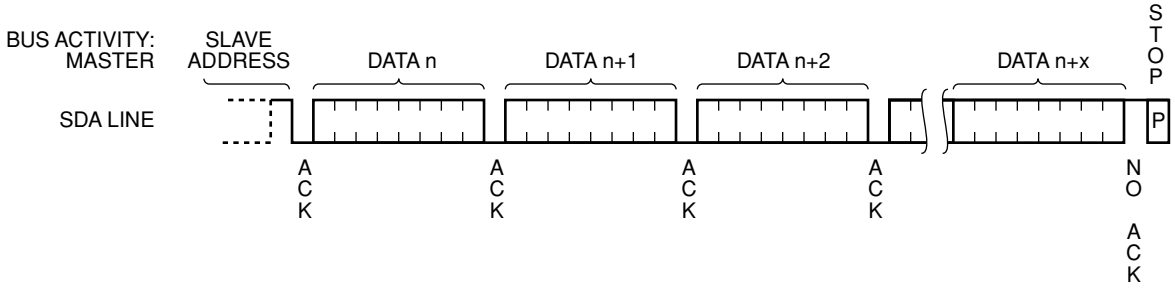
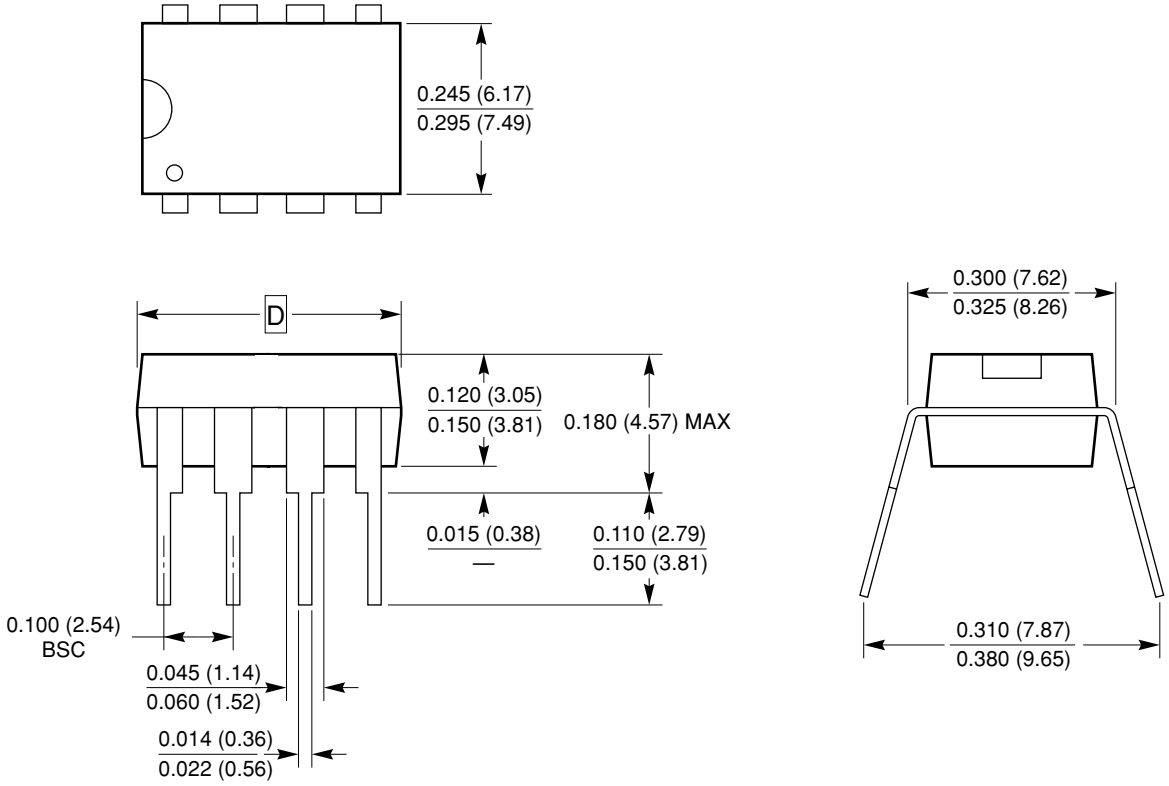


Figure 13. Sequential Read Timing



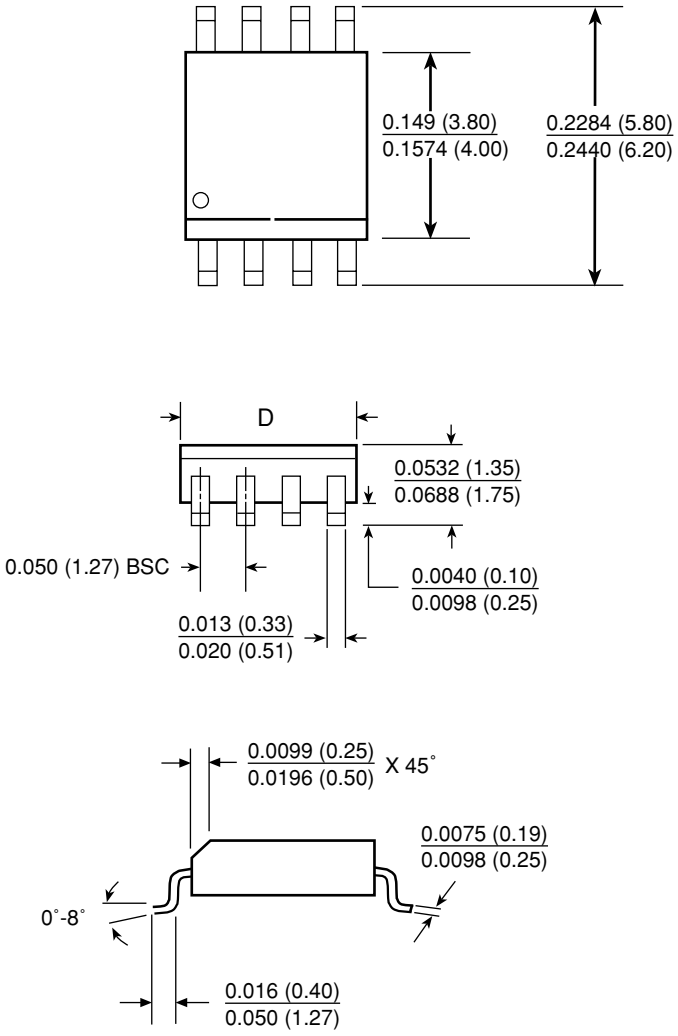
8–22-LEAD 300 MIL WIDE PLASTIC DIP (P, L)



Dimension D		
Pkg	**Min**	**Max**
8L	0.355 (9.02)	0.400 (10.16)

Notes:
1. Complies with JEDEC Publication 95 MS001 dimensions; however, some of the dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

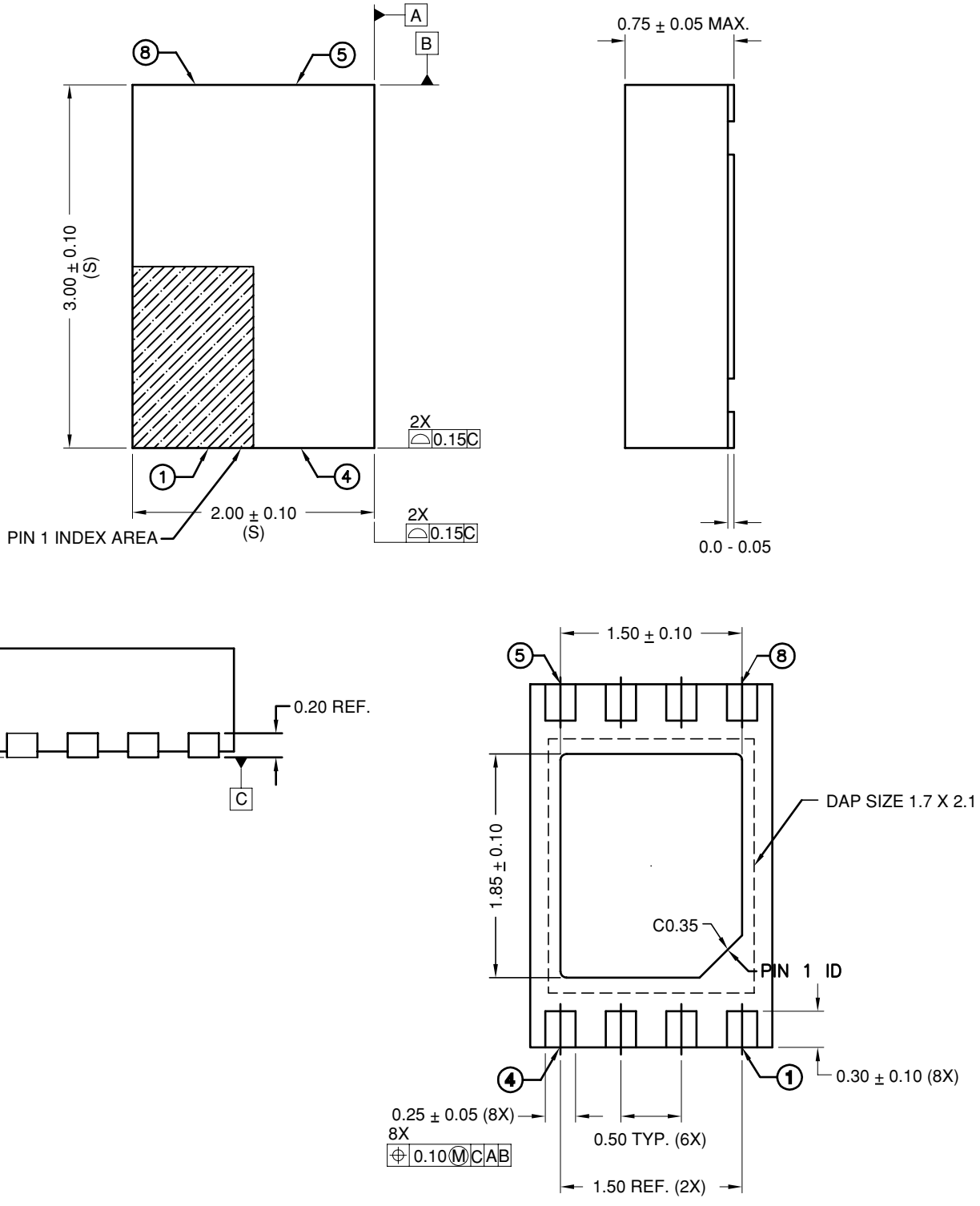
8-LEAD 150 MIL WIDE SOIC (J, W)



Dimension D		
Pkg	**Min**	**Max**
8L	0.1890(4.80)	0.1968(5.00)

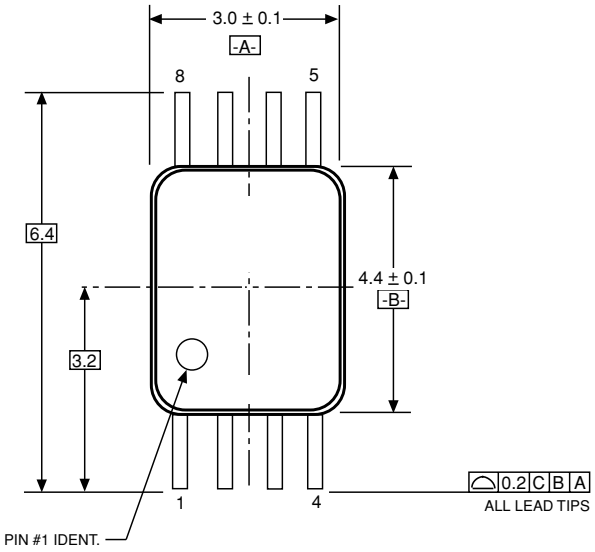
Notes:
1. Complies with JEDEC publication 95 MS-012 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.
3. Lead coplanarity is 0.004" (0.102mm) maximum.

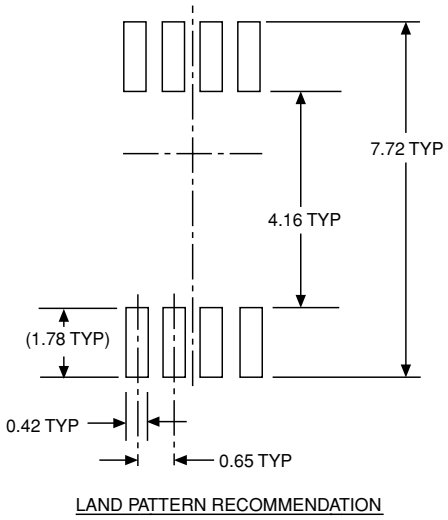
8-PAD TDFN 2X3 PACKAGE (VP2, SP2)



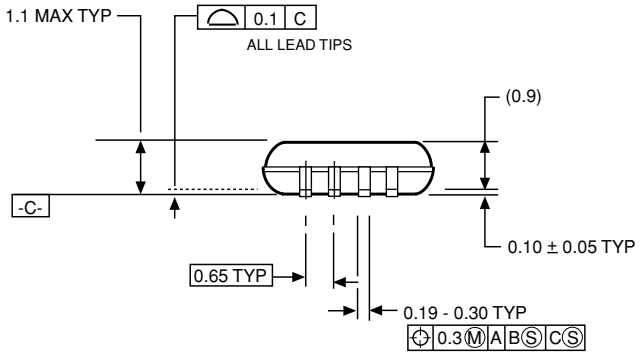
NOTE:
1. ALL DIMENSIONS IN MM. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMNALS. COPLANARITY SHALL NOT EXCEED 0.08 MM.
3. WARPAGE SHALL NOT EXCEED 0.10 MM.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE NOT CONSIDERED AS SPECIAL CHARACTERISTIC.

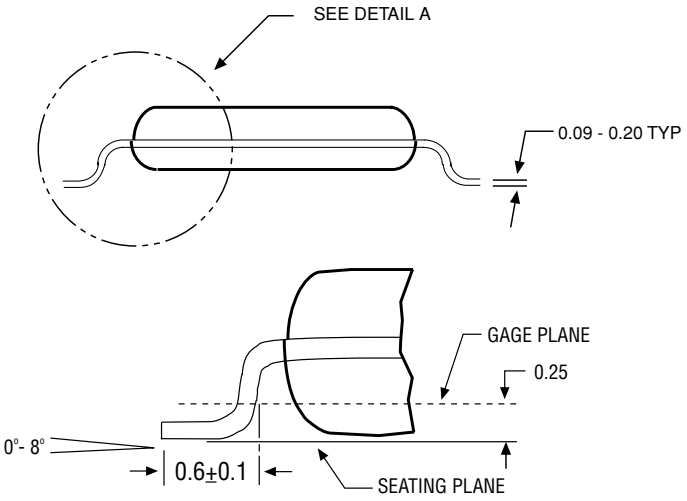
8-LEAD TSSOP (U, Y)





LAND PATTERN RECOMMENDATION

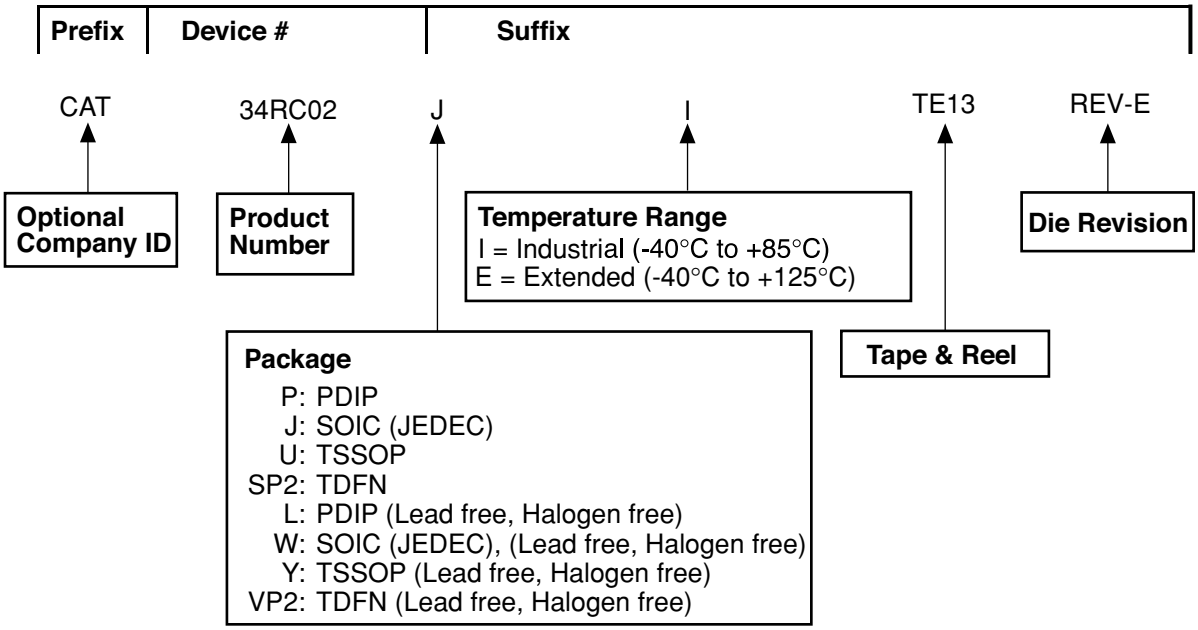




DETAIL A

Notes:
1. Lead coplanarity is 0.004" (0.102mm) maximum.

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a 34RC02JI-TE13 (SOIC, Industrial Temperature, 1.7 Volt to 5.5 Volt Operating Voltage, Tape & Reel)

REVISION HISTORY

Date	Revision	Comments
09/22/03	A	Initial Issue
12/09/03	B	Removed Automotive temperature range Changed Industrial Temp to " I" from " Blank" in ordering information
01/12/04	C	Updated Features Replaced Block Diagram with Functional Symbol Updated Notes for Reliability Characteristics, D.C. Operating Characteristics and Capacitance Updated TDFN package Updated packaging information to reflect new TDFN package
02/20/04	D	Re-labeled TDFN package to A0, A1, A2 instead of A1, A2, A3
03/22/04	E	Updated Absolute Max. Ratings Updated DC Operating Characteristics Updated Table 1 (SWP Commands) Updated Fig 11 Added mechanical package drawings Corrected TDFN drawing
03/31/04	F	Corrected table 1 SWP Commands
05/16/04	G	Update D.C. Operating Characteristics Update Write Cycle Limits Update Revision History Update Rev Number
06/03/04	H	Update Die Revision in Ordering Information Eliminate data sheet designation Updated DC Operating Characteristics
06/07/04	I	Updated Write Cycle Limits
9/27/04	J	Added Power-On Reset (POR) description Added V_{HV} and deleted ΔV_{HV} in DC Operating Characteristics
10/18/04	K	Updated DC Operating Characteristics & notes (removed Note 5)

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