34AA02/34LC02

2K I²C™ Serial EEPROM Software Write-Protect

Features:

- Permanent and Resettable Software Write-Protect for Lower Half of the Array (00h-7Fh)
- Single Supply with Operation Down to 1.7V
- Low-Power CMOS Technology:
  - Read current 1 mA, typical
  - Standby current, 100 nA, typical
- 2-Wire Serial Interface Bus, I²C™ Compatible
- Cascadable up to Eight Devices
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Compatibility
- 1 MHz Clock for LC Versions
- Page Write Time 3 ms, typical
- Self-Timed Erase/Write Cycle
- 16-Byte Page Write Buffer
- ESD Protection > 4,000V
- Software Write Protection for Lower 128 Bytes
- Hardware Write Protection for Entire Array
- More than 1 Million Erase/Write Cycles
- Data Retention > 200 Years
- 8-Lead PDIP, SOIC, TSSOP, MSOP and TDFN packages
- 6-Lead SOT-23 Package
- Pb-free and RoHS Compliant
- Available for Extended Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

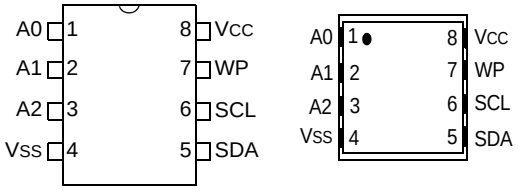
Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp Ranges
34AA02	1.7-5.5	400 kHz(1)	I,E
34LC02	2.2-5.5	1 MHz	I,E

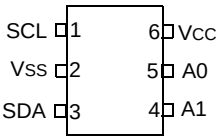
Note 1: 100 kHz for VCC <1.8V

Package Types

PDIP/SOIC/TSSOP/MSOP/TDFN



SOT-23



Description:

The Microchip Technology Inc. 34AA02/34LC02 (34XX02*) is a 2 Kbit Electrically Erasable PROM capable of operation across a broad voltage range (1.7V to 5.5V). This device has two software write-protect features for the lower half of the array, as well as an external pin that can be used to write-protect the entire array. This allows the system designer to protect none, half, or all of the array, depending on the application. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.7V, with standby and active currents of only 100 nA and 1 mA, respectively. The 34XX02 also has a page write capability for up to 16 bytes of data. The 34XX02 is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP, MSOP and TDFN packages. The 34XX02 is also available in the 6-lead, SOT-23 package.

*34XX02 is used in this document as a generic part number for the 34AA02/34LC02 devices.

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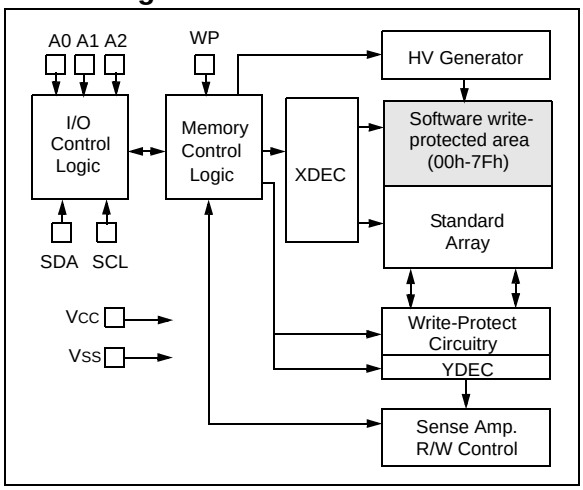
Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.3V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC SPECIFICATIONS

DC CHARACTERISTICS			VCC = +1.7V to +5.5V Industrial (I): TA = -40°C to +85°C Automotive (E):TA = -40°C to +125°C				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
	—	**A0, A1, A2, SCL, SDA and WP pins**	—	—	—	—	—
D1	VIH	High-level input voltage	0.7 VCC	—	—	V	—
D2	VIL	Low-level input voltage	—	—	0.3 VCC	V	0.2 VCC for VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger inputs	0.05 VCC	—	—	V	**(Note)**
D4	VOL	Low-level output voltage	—	—	0.40	V	IOL = 3.0 mA, VCC = 2.5V
D5	VHV	High-Voltage Detect	7	—	10	V	A0 Pin only, VCC < 2.2V
			VCC + 4.8	—	10	V	A0 Pin only, VCC ≥ 2.2V
			10	—	VCC + 4.8	V	A0 Pin only, VCC > 5.2V
D6	ILI	Input leakage current	—	—	±1	µA	VIN = VSS or VCC
D7	ILO	Output leakage current	—	—	±1	µA	VOUT = VSS or VCC
D8	CIN, COUT	Pin capacitance (all inputs/outputs)	—	—	10	pF	VCC = 5.5V **(Note)** TA = 25°C, FCLK = 1 MHz
D9	ICC write	Operating current	—	0.1	3	mA	VCC = 5.5V, SCL = 1 MHz
D10	ICC read		—	0.05	1	mA	—
D11	ICCS	Standby current	— —	0.01 —	1 5	µA µA	Industrial Automotive SDA = SCL = VCC A0, A1, A2, WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC SPECIFICATIONS

AC CHARACTERISTICS			V_{CC} = +1.7V to +5.5V Industrial (I): T_A = -40°C to +85°C Automotive (E): T_A = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	F_{CLK}	Clock frequency	— — —	100 400 1000	kHz	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
2	T_{HIGH}	Clock high time	4000 600 500	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
3	T_{LOW}	Clock low time	4700 1300 500	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
4	T_R	SDA and SCL rise time **(Note 1)**	— — —	1000 300 300	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
5	T_F	SDA and SCL fall time **(Note 1)**	— — —	1000 300 300	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
6	$T_{HD:STA}$	Start condition hold time	4000 600 250	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
7	$T_{SU:STA}$	Start condition setup time	4700 600 250	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
8	$T_{HD:DAT}$	Data input hold time	0	—	ns	**(Note 2)**
9	$T_{SU:DAT}$	Data input setup time	250 100 100	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
10	$T_{SU:STO}$	Stop condition setup time	4000 600 250	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
11	$T_{SU:WP}$	WP setup time	4000 600 600	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
12	$T_{HD:WP}$	WP hold time	4700 600 600	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
13	T_{AA}	Output valid from clock **(Note 2)**	— — —	3500 900 400	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
14	T_{BUF}	Bus free time: Time the bus must be free before a new transmission can start	1300 4700	— — —	ns	1.7V ≤ V_{CC} < 1.8V 1.8V ≤ V_{CC} ≤ 5.5V 2.5V ≤ V_{CC} ≤ 5.5V (34LC02)
16	T_{SP}	Input filter spike suppression (SDA and SCL pins)	—	50	ns	All except 34LC02 **(Note 1 and Note 3)**
17	T_{WC}	Write cycle time (byte or page)	—	5	ms	—
18	—	Endurance	1M	—	cycles	25°C, V_{CC} = 5.5V, Block mode **(Note 4)**

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a T_I specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

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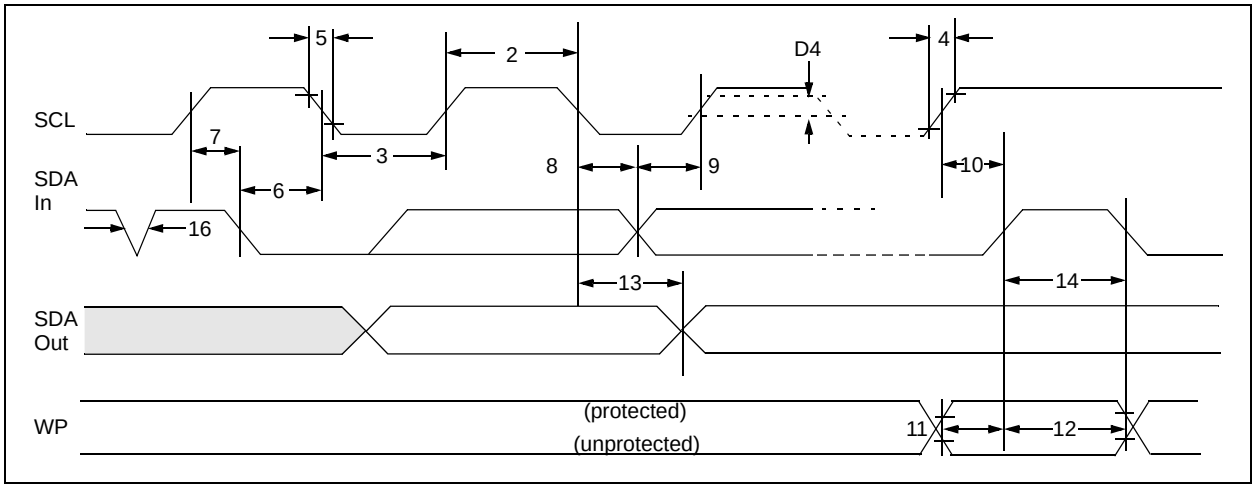
FIGURE 1-1: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 34XX02 has two Software Write-Protect features that allow you to protect half of the array from being written (Addresses 00h-7Fh). One command, Software Write-Protect (SWP) will prevent writes to half of the array and is resettable by using the Clear Software Write-Protect (CSWP) command. The other command is Permanent Software Write-Protect (PSWP), which is not resettable and will permanently lock half the array from being written to. The device still has an external pin (WP) that allows you to protect the entire array if so desired.

The 34XX02 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data, as a receiver. The bus has to be controlled by a master device, which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 34XX02 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus Not Busy (A)

Both data and clock lines remain high.

3.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between the Start and Stop conditions is determined by the master device and is, theoretically, unlimited; although only the last sixteen will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first-in, first-out (FIFO) fashion.

3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. Exceptions to this rule relating to software write protection are described in **Section 7.0 “Write Protection”**. The master device must generate an extra clock pulse, which is associated with this Acknowledge bit.

Note:	The 34XX02 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end-of-data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (34XX02) will leave the data line high to enable the master to generate the Stop condition.

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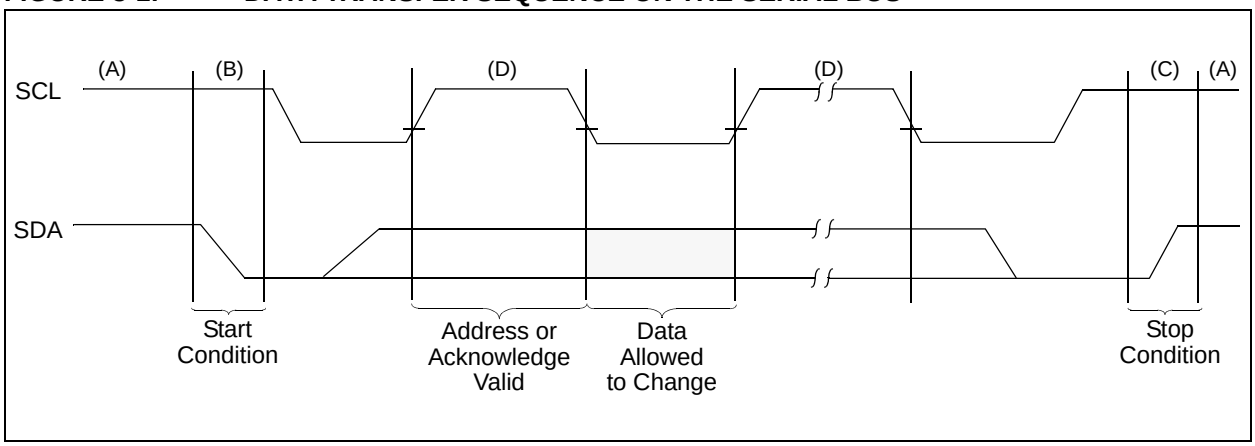
FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



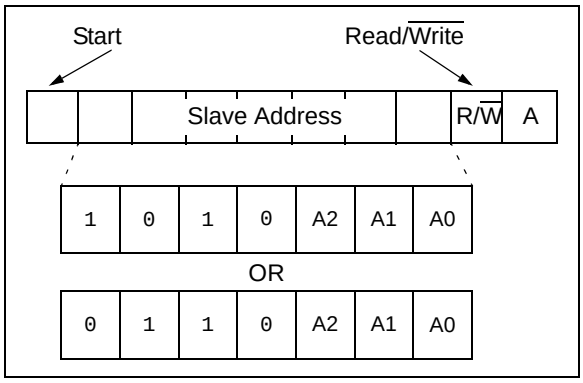
3.6 Device Addressing

A control byte is the first byte received following the Start condition from the master device. The first part of the control byte consists of a 4-bit control code which is set to '1010' for normal read and write operations and '0110' for writing to the write-protect register. The control byte is followed by three Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 34XX02 devices on the same bus and are used to determine which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond.

The eighth bit of slave address determines if the master device wants to read or write to the 34XX02 (Figure 3-2). When set to a one, a read operation is selected. When set to a zero, a write operation is selected.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	A2 A1 A0	1
Write	1010	A2 A1 A0	0
Write-Protect Register	0110	A2 A1 A0	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATIONS

4.1 Byte Write

Following the Start signal from the master, the device code (4 bits), the Chip Select bits (3 bits) and the R/$\overline{W}$ bit, which is a logic low, are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow, once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the Address Pointer of the 34XX02.

After receiving another Acknowledge signal from the 34XX02, the master device will transmit the data word to be written into the addressed memory location. The 34XX02 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, which means that during this time, the 34XX02 will not generate Acknowledge signals (Figure 4-1). If an attempt is made to write to the array when the software or hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if the write protection is enabled.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 34XX02 in the same way as in a byte write. Instead of generating a Stop condition, the master transmits up to 15 additional data bytes to the 34XX02, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a Stop condition. Upon receipt of each word, the four lower order Address Pointer bits are internally incremented by one. The higher order four bits of the word address remain constant. If the master should transmit more than 16 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an

internal write cycle will begin (Figure 4-2). If an attempt is made to write to the array when the hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if the write protection is enabled.

Note:	Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 4-1: BYTE WRITE

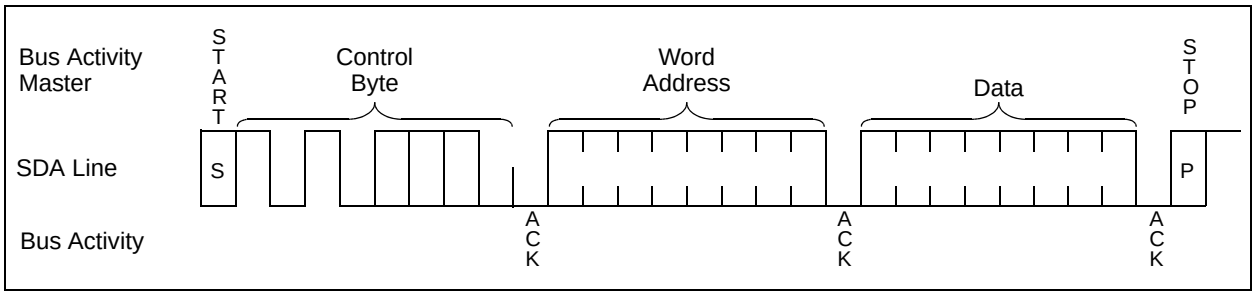
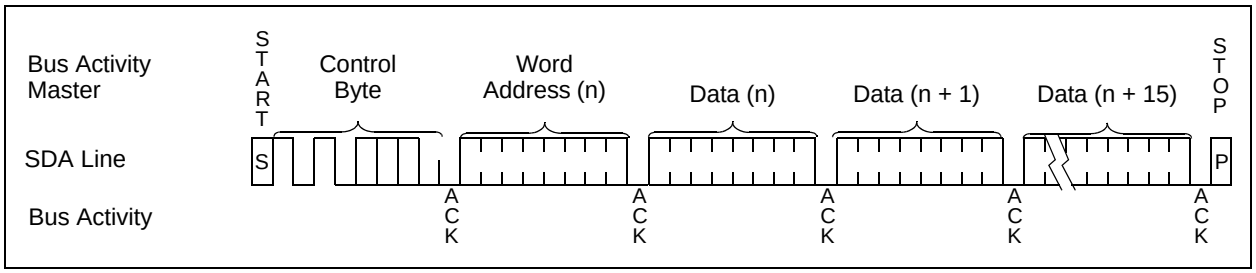


FIGURE 4-2: PAGE WRITE



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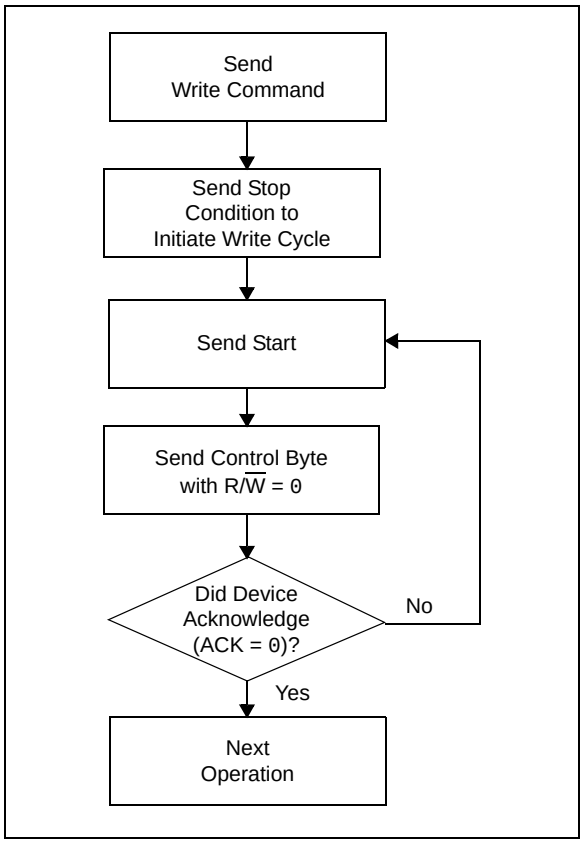
5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

6.1 Current Address Read

The 34XX02 contains an address counter that maintains the address of the last word accessed, internally incremented by '1'. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ bit set to '1', the 34XX02 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 34XX02 discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 34XX02 as part of a write operation. Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 34XX02 then issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 34XX02 discontinues transmission (Figure 6-2).

6.3 Sequential Read

Sequential reads are initiated in the same way as a random read, with the exception that after the 34XX02 transmits the first data byte, the master issues acknowledge, as opposed to a Stop condition in a random read. This directs the 34XX02 to transmit the next sequentially addressed 8-bit word (Figure 6-3).

To provide sequential reads, the 34XX02 contains an internal Address Pointer, which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

6.4 Contiguous Addressing Across Multiple Devices

The Chip Select bits (A2, A1, A0) can be used to expand the contiguous address space for up to 16K bits by adding up to eight 34XX02 devices on the same bus. In this case, software can use A0 of the control byte as address bit A8; A1 as address bit A9, and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

6.5 Noise Protection and Brown-Out

The 34XX02 employs a V_{CC} threshold detector circuit which disables the internal erase/write logic if the V_{CC} is below 1.35V at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation, even on a noisy bus.

FIGURE 6-1: CURRENT ADDRESS READ

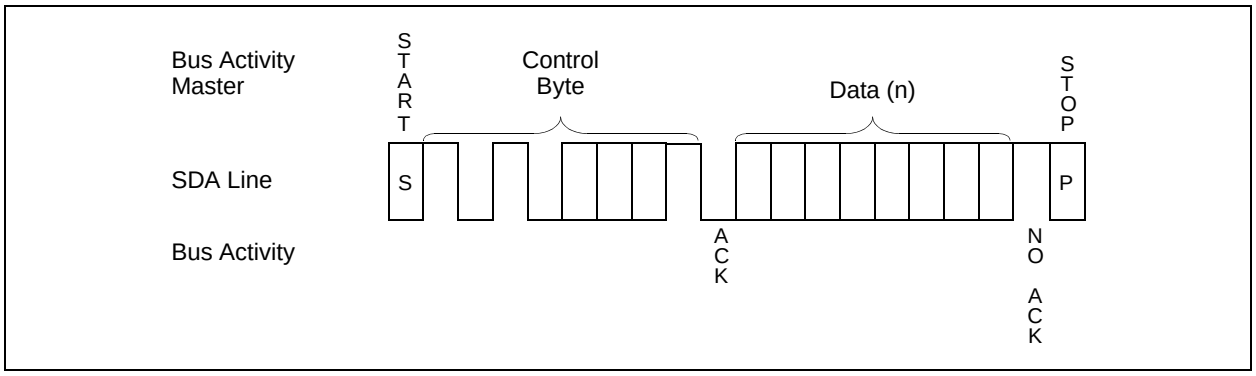


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FIGURE 6-2: RANDOM READ

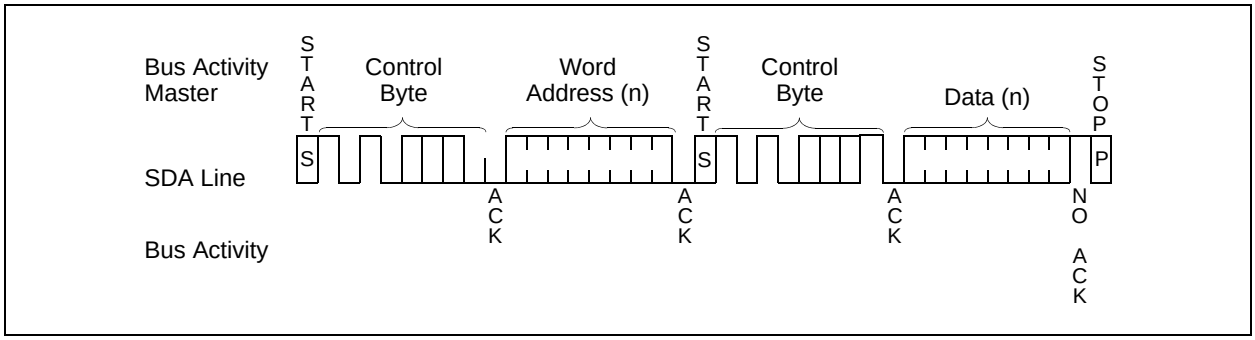
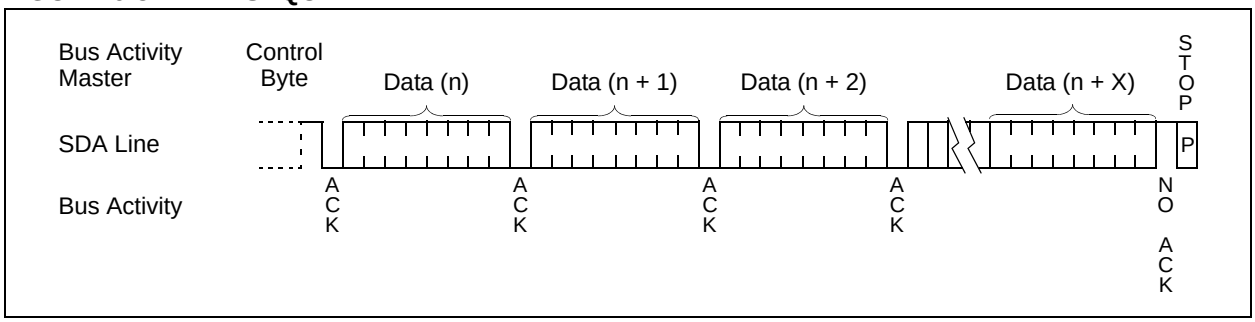


FIGURE 6-3: SEQUENTIAL READ



7.0 WRITE PROTECTION

The 34XX02 has two software write-protect features (SWP and PSWP) that allows the lower half of the array (addresses 00h-7Fh) to be write-protected, as well as a WP pin that can be used to protect the entire array. The permanent software write-protect feature is enabled by sending the device a special command. Once this feature has been enabled, it cannot be reversed. The resettable software write-protect feature is also enabled by sending the device a special command but can be reset by issuing another special command. In addition to the software protect features, there is a WP pin that can be used to write-protect the entire array, regardless of whether the software write-protect register has been written or not.

Table 7-2 and Table 7-3 describe how the 34XX02 will acknowledge specific commands under various circumstances.

7.1 Hardware Write Protection

The WP pin allows the user to write-protect the entire array (00-FF) when the pin is tied to VCC. If the pin is tied to VSS the write protection is disabled.

7.2 Software Write Protection (SWP) and Clear Software Write Protection (CSWP)

In addition to hardware write-protect the 34XX02 has an additional software write-protect feature that, when set, protects the first 128 bytes (00-7Fh) of the array from being written.

Setting the software write protection is done by sending the SWP instruction. SWP can also then be cleared by issuing a CSWP instruction (see Figure 7-1).

These two instructions follow the same format as the BYTE WRITE instruction with the exception of the Device Type Identifier, (typically '1010', instead changes to '0110'). Once this identifier is recognized by the device, the rest of the Byte Write command, address and data, are "don't cares". In addition to the identifier, high voltage must be applied to the A0 pin of the device and specific levels must be present on A1 and A2. See Table 7-1 for the available commands.

7.3 Permanent Software Write-Protect (PSWP)

The Permanent software write protection, or PSWP is another instruction that may be used to permanently protect the first 128 byte of the array. Once this command is issued, the user will no longer have the ability to clear this feature regardless of instruction, power cycling, or state of the WP pin. Also, once this instruction has been executed, the device will no longer acknowledge the device identifier '0110'.

FIGURE 7-1: SOFTWARE WRITE PROTECTION FOR SWP, CSWP, PSWP, OR CPSWP

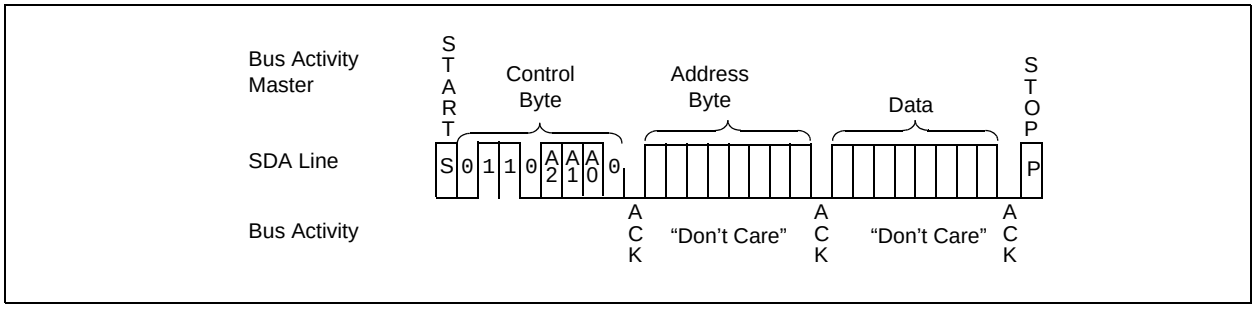


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TABLE 7-1: SOFTWARE WRITE PROTECTION INSTRUCTION SET WP = 0

	Address Pins			Device Type Identifier				Chip Select Bits			R/$\overline{W}$
	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
SWP	VSS	VSS	VHV	0	1	1	0	0	0	1	0
CSWP	VSS	VCC	VHV	0	1	1	0	0	1	1	0
PSWP	A2	A1	A0	0	1	1	0	A2	A1	A0	0
Read SWP	VSS	VSS	VHV	0	1	1	0	0	0	1	1
Read CSWP	VSS	VCC	VHV	0	1	1	0	0	1	1	1
Read PSWP	A2	A1	A0	0	1	1	0	A2	A1	A0	1

1. A0 is used to detect VHV for the SWP and CSWP commands.
2. B3, B2 and B1 are compared to the A2, A1 and A0 external pins, respectively on the 34XX02.

TABLE 7-2: ACKNOWLEDGE TABLE FOR WRITE OR WRITE PROTECTION WITH R/$\overline{W}$ = 0

Status	Write-Protect	Instruction	ACK	Address	ACK	Data Byte	ACK	Write Cycle
Permanently Protected	x	PSWP, SWP, CSWP	No Ack	Don't Care	No Ack	Don't Care	No Ack	No
		PAGE or BYTE WRITE in lower 128 bytes	Ack	Address	Ack	Data	No Ack	No
Protected with SWP	0	SWP	No Ack	Don't Care	No Ack	Don't Care	No Ack	No
		CSWP	Ack	Don't Care	Ack	Don't Care	Ack	Yes
		PSWP	Ack	Don't Care	Ack	Don't Care	Ack	Yes
		PAGE or BYTE WRITE in lower 128 bytes	Ack	Address	Ack	Data	No Ack	No
	1	SWP	No Ack	Don't Care	No Ack	Don't Care	No Ack	No
		CSWP	Ack	Don't Care	Ack	Don't Care	No Ack	No
		PSWP	Ack	Don't Care	Ack	Don't Care	No Ack	No
		PAGE or BYTE WRITE	Ack	Address	Ack	Data	No Ack	No
Not Protected	0	PSWP, SWP, or CSWP	Ack	Don't Care	Ack	Don't Care	Ack	Yes
		PAGE or BYTE WRITE	Ack	Address	Ack	Data	Ack	Yes
	1	PSWP, SWP, or CSWP	Ack	Don't Care	Ack	Don't Care	No Ack	No
		PAGE or BYTE WRITE	Ack	Address	Ack	Address	No Ack	No

TABLE 7-3: ACKNOWLEDGE TABLE FOR WRITE OR WRITE PROTECTION WITH R/$\overline{W}$ = 1

Status	Instruction	ACK
Permanently Protected	PSWP, SWP, CSWP	No Ack
Protected with SWP	SWP	No Ack
	CSWP	Ack
	PSWP	Ack
Not protected	PSWP, SWP, CSWP	Ack

8.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 8-1.

TABLE 8-1: PIN FUNCTION TABLE

Symbol	PDIP	SOIC	TSSOP	MSOP	TDFN	SOT-23	Description
A0	1	1	1	1	1	5	Chip Address Input
A1	2	2	2	2	2	4	Chip Address Input
A2	3	3	3	3	3	NC	Chip Address Input
VSS	4	4	4	4	4	2	Ground
SDA	5	5	5	5	5	3	Serial Address/Data I/O
SCL	6	6	6	6	6	1	Serial Clock
WP	7	7	7	7	7	NC	Write-Protect Input
VCC	8	8	8	8	8	6	+1.7V to 5.5V Power Supply

8.1 A0, A1, A2

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 34XX02 devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VSS or VCC.

The A0 pin is also used to detect VHV.

8.2 Serial Address/Data Input/Output (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

8.3 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

8.4 Write-Protect (WP)

This is the hardware write-protect pin. It can be tied to VCC or VSS. If tied to VCC, the hardware write protection is enabled. If the WP pin is tied to VSS, the hardware write protection is disabled.

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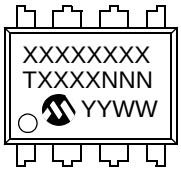
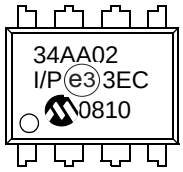
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

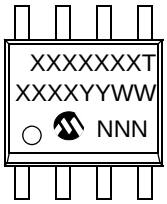
8-Lead PDIP (300 mil)



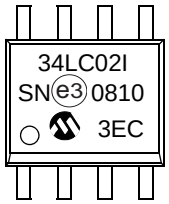
Example:



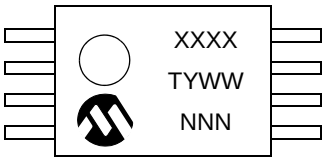
8-Lead SOIC (3.90 mm)



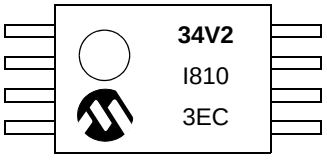
Example:



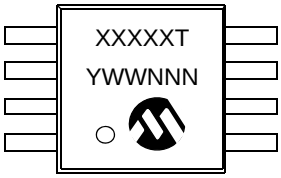
8-Lead TSSOP



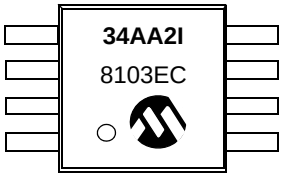
Example:



8-Lead MSOP



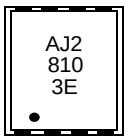
Example:



8-Lead 2x3 TDFN

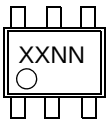


Example:



Part Number	1st Line Marking Codes		
	TSSOP	MSOP	TDFN
34AA02	34A2	34AA2T	2J2
34LC02	34L2	34VL2T	2J5

6-Lead SOT-23



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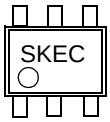

SOT-23 Marking Codes		
Device	I-temp	E-temp
34AA02	STNN	SVNN
34LC02	SKNN	SLNN
Pb-free topside mark is same; Pb-free noted only on carton label.		

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

*****Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

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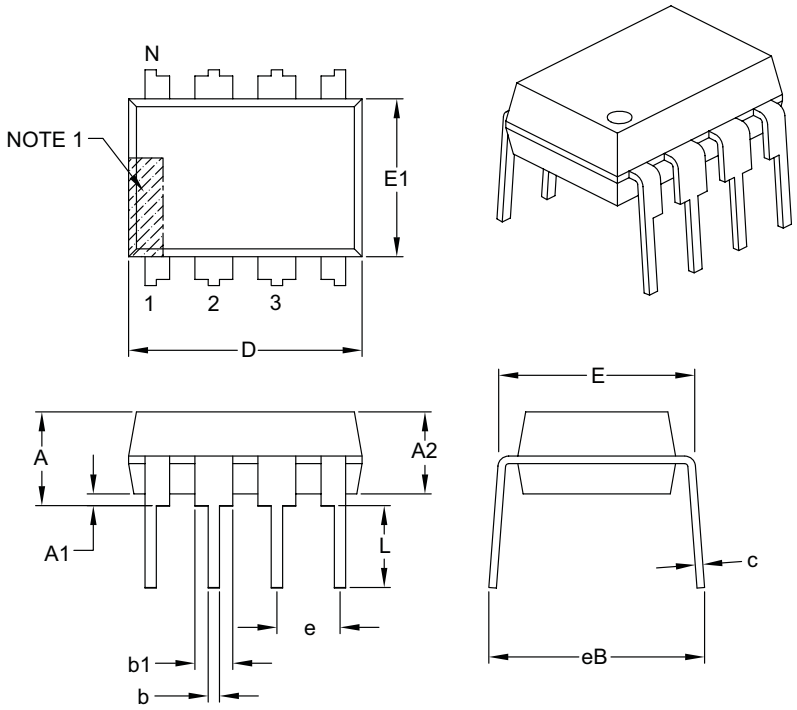
8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

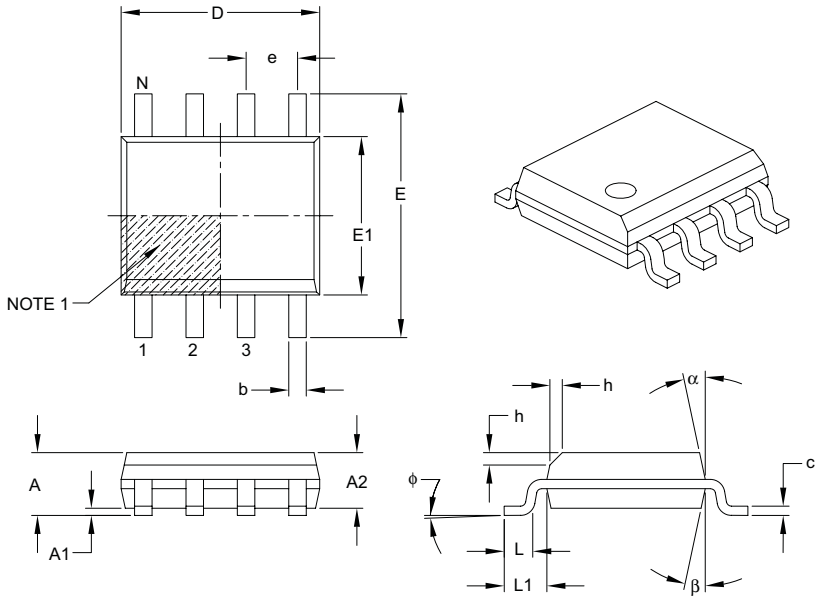
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

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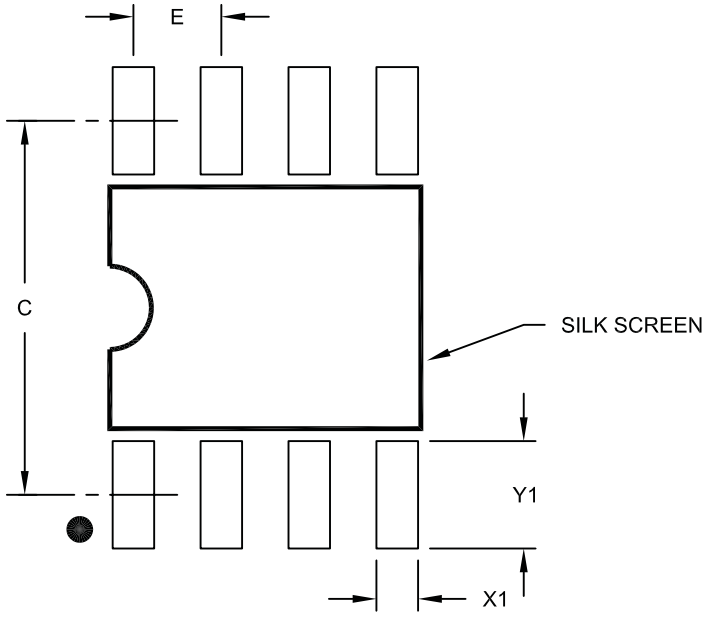

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

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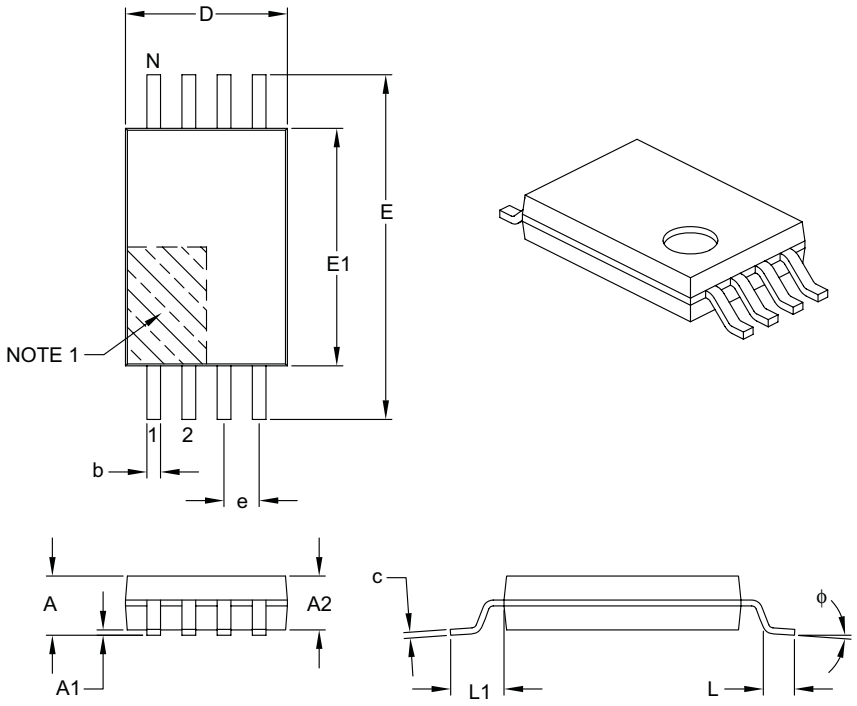

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

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8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

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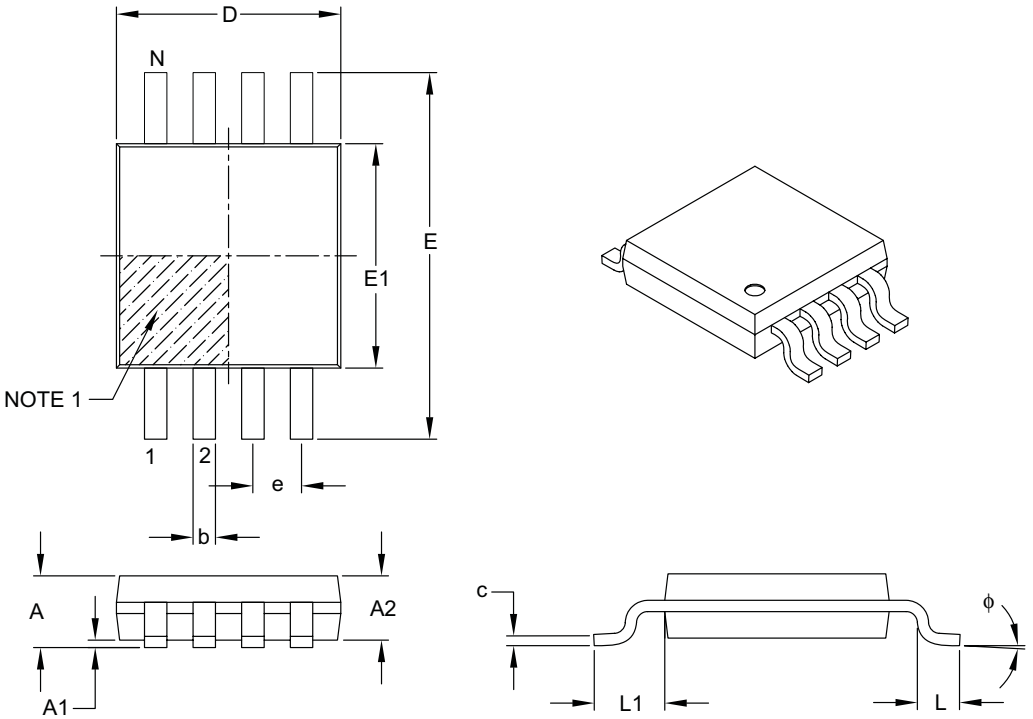


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

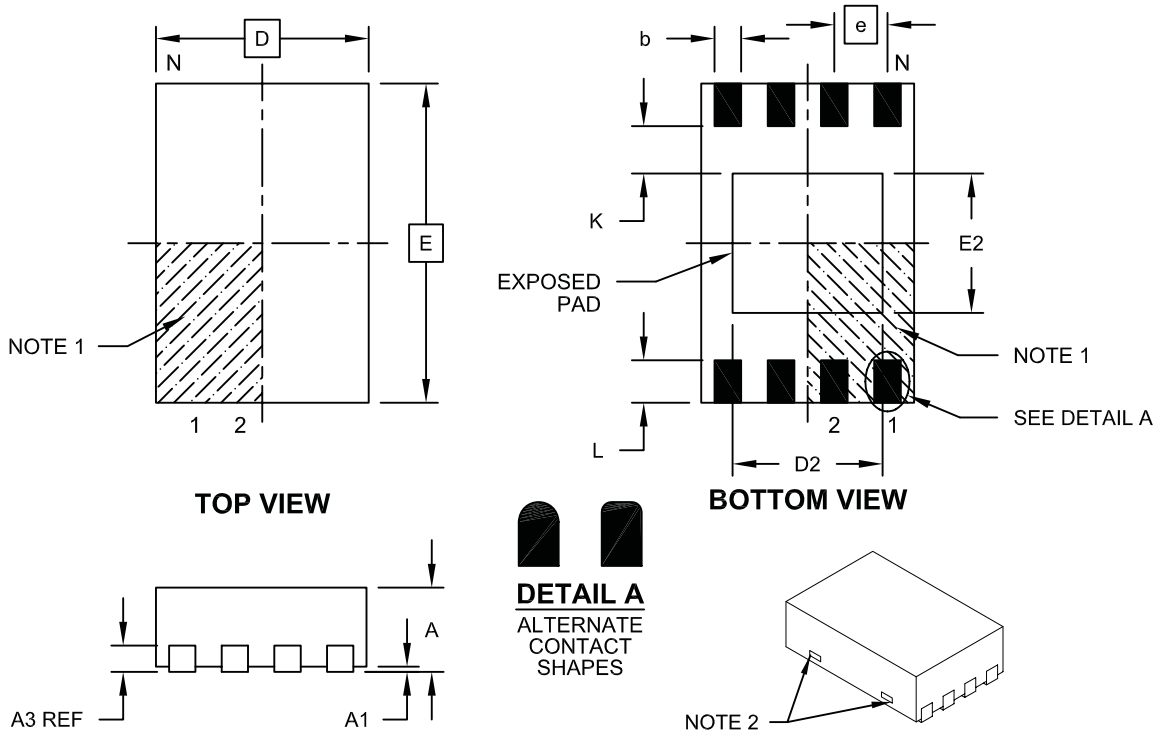
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129B

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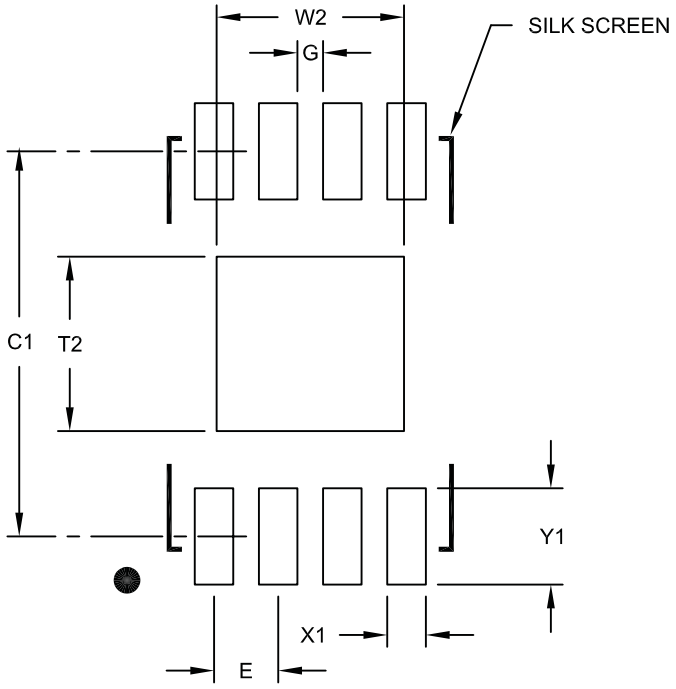
8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

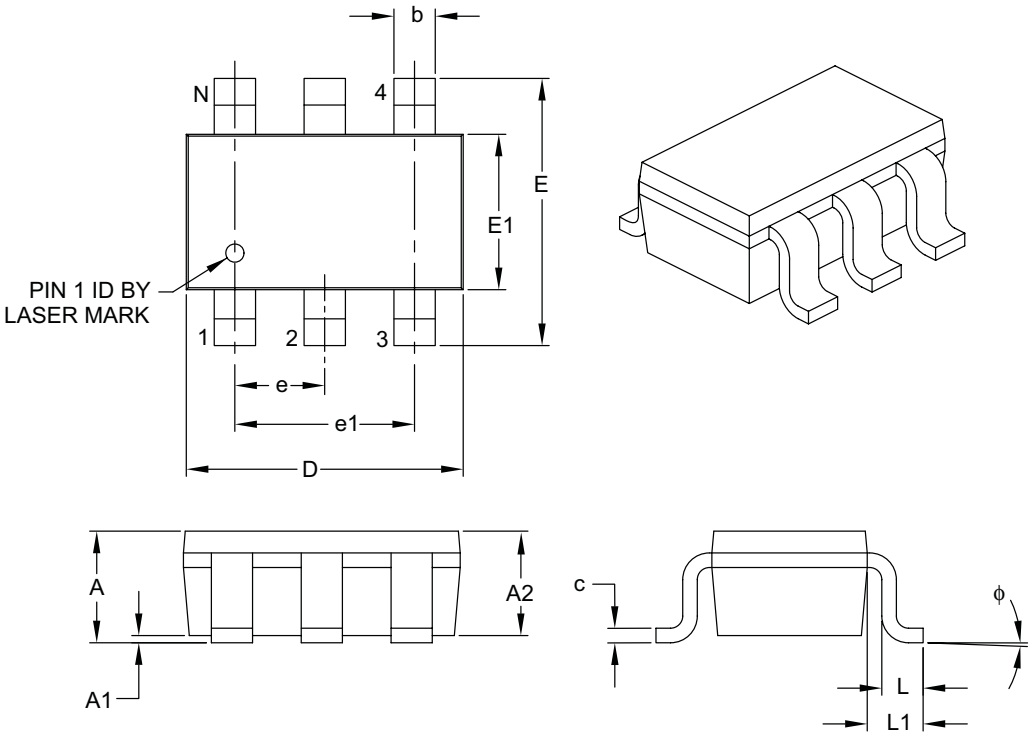
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

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APPENDIX A: REVISION HISTORY

Revision A (1/2007)

Original release of this document.

Revision B (2/2007)

Replaced Package Drawings.

Revision C (2/2008)

Added TDFN and SOT-23 Package info; Removed "VL" Part.

Revision D (4/2008)

Updated Product Identification System table, example (e).

NOTES:

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- Technical Support
- Development Systems Information Line

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4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	34AA02:	=	1.7V, 2 Kbit I^2C Serial EEPROM
	34AA02T:	=	1.7V, 2 Kbit I^2C Serial EEPROM (Tape and Reel)
	34LC02:	=	2.2V, 2 Kbit I^2C Serial EEPROM
	34LC02T:	=	2.2V, 2 Kbit I^2C Serial EEPROM (Tape and Reel)
Temperature Range:	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Package:	OT	=	Plastic Small Outline (SOT-23), 6-lead
	P	=	Plastic DIP (300 mil body), 8-lead
	SN	=	Plastic SOIC (3.90 mm body), 8-lead
	ST	=	Plastic TSSOP (4.4 mm), 8-lead
	MS	=	Plastic Micro Small Outline (MSOP), 8-lead
	MNY*	=	Plastic Dual Flat, no lead package (2x3 mm body), 8-lead

Note 1: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.

Examples:

a) 34AA02-I/P: Industrial Temperature, 1.7V, PDIP package

b) 34AA02-I/SN: Industrial Temperature, 1.7V, SOIC package

c) 34AA02T-E/MS: Tape and Reel, Automotive Temperature, 1.7V, MSOP package

d) 34LC02-I/P: Industrial Temperature, 2.2V, PDIP package

e) 34LC02-I/MNY: Industrial Temperature, 2.2V, DFN package

f) 34LC02T-E/MS: Tape and Reel, Automotive Temperature, 2.2V, MSOP package

NOTES:

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