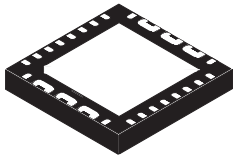
Document Number: MC34716
Rev. 3.0, 5/2007

RoHS

1.0 MHz Dual Switch-Mode DDR Power Supply

34716

DUAL SWITCH-MODE DDR POWER SUPPLY



EP SUFFIX
98ASA10728D
26-PIN QFN

The 34716 is a highly integrated, space-efficient, low cost, dual synchronous buck switching regulator with integrated N-channel power MOSFETs. It is a high performance point-of-load (PoL) power supply with its second output having the ability to track an external reference voltage. it provides a full power supply solution for Double-Data-Rate (DDR) Memories.

Channel one provides a source only 5.0 A drive capability, while channel two can sink and source up to 3.0 A. Both channels are highly efficient with tight output regulation. With its high current drive capability, channel one can be used to supply the V_{DDQ} to the memory chipset. The second channel's ability to track a reference voltage makes it ideal to provide the termination voltage (V_{TT}) for modern data buses. The 34716 also provides a buffered output reference voltage (V_{REFOUT}) to the memory chipset

The 34716 offers the designer the flexibility of many control, supervisory, and protection functions to allow for easy implementation of complex designs. It is housed in a Pb-Free, thermally enhanced, and space efficient 26-Pin Exposed Pad QFN.

Features

- 50 mΩ Integrated N-Channel Power MOSFETs
- Input Voltage Operating Range from 3.0 V to 6.0 V
- ±1 % Accurate Output Voltages, Ranging from 0.7 V to 3.6 V
- The second output Tracks 1/2 an External Reference Voltage
- ±1 % Accurate Buffered Reference Output Voltage
- Programmable Switching Frequency Range from 200 kHz to 1.0 MHz
- Programmable Soft Start Timing for Channel One
- Over Current Limit and Short Circuit Protection on Both Channels
- Thermal Shutdown
- Output Overvoltage and Undervoltage Detection
- Active Low Power Good Output Signal
- Active Low Standby and Shutdown Inputs
- Pb-Free Packaging Designated by Suffix Code EP.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC34716EP/R2	-40 to 85°C	26 QFN

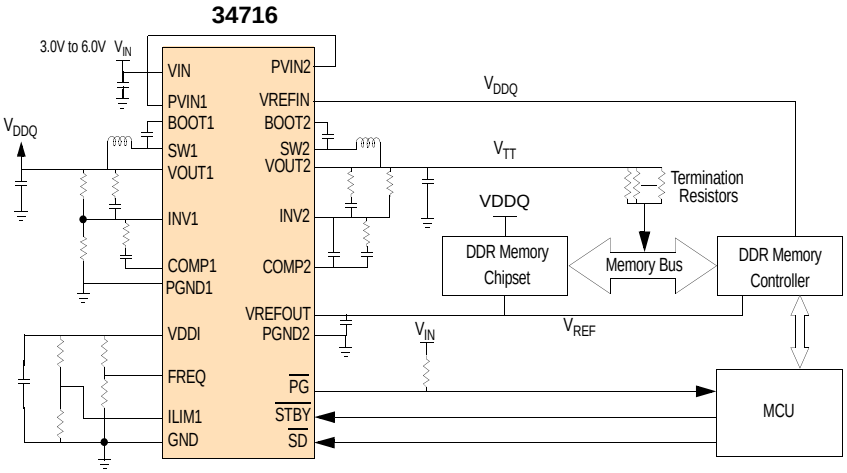


Figure 1. 34716 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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INTERNAL BLOCK DIAGRAM

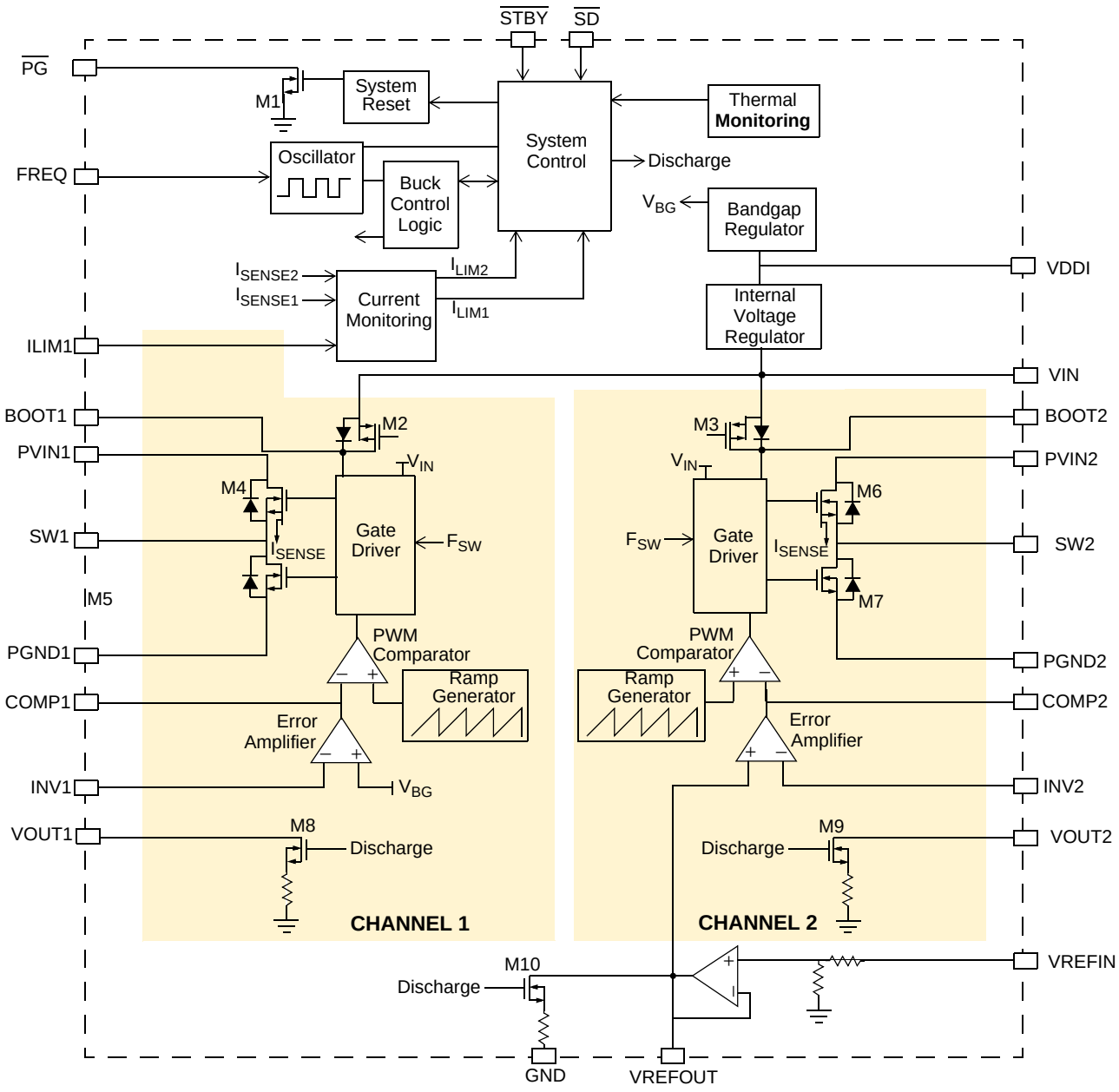


Figure 2. 34716 Simplified Internal Block Diagram

PIN CONNECTIONS

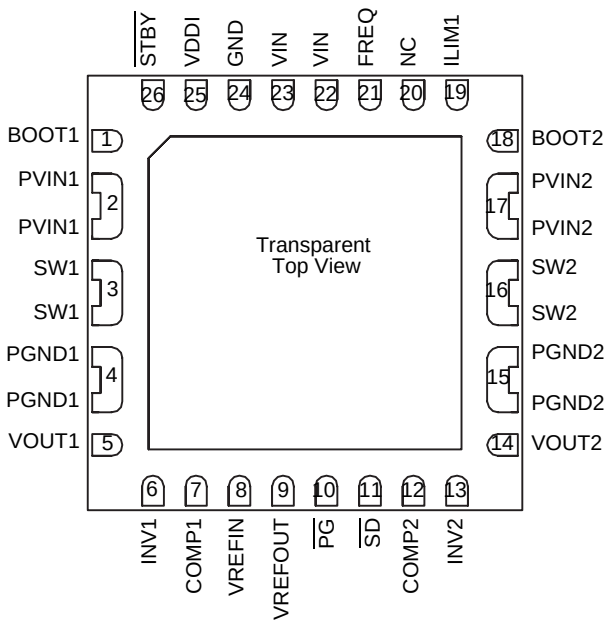


Figure 3. 34716 Pin Connections

Table 1. 34716 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 11.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	BOOT1	Passive	Bootstrap	Channel 1 Bootstrap capacitor input pin
2	PVIN1	Supply	Power Input Voltage	Channel 1 Buck converter power input
3	SW1	Input/Output	Switching Node	Channel 1 Buck converter switching node
4	PGND1	Ground	Power Ground	Channel 1 Buck converter and discharge MOSFETs power ground
5	VOUT1	Input	Output Voltage Discharge Path	Channel 1 Buck converter output voltage discharge pin
6	INV1	Input	Error Amplifier Inverting Input	Channel 1 Buck converter error amplifier inverting input
7	COMP1	Input	Buck Convertor Compensation Input	Channel 1 Buck converter external compensation network input
8	VREFIN	Input	Reference Voltage Input	Voltage tracking reference voltage input
9	VREFOUT	Output	Reference Voltage Output	This is a buffered reference voltage output
10	$\overline{PG}$	Output	Power Good Output Signal	It is an active low open drain power good status reporting output
11	$\overline{SD}$	Input	Shutdown Input	Shutdown mode input control pin
12	COMP2	Input	Buck Convertor Compensation Input	Channel 2 Buck converter external compensation network input
13	INV2	Input	Error Amplifier Inverting Input	Channel 2 Buck converter error amplifier inverting input

Table 1. 34716 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 11.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
14	VOUT2	Output	Output Voltage Discharge Path	Channel 2 Buck converter output voltage discharge pin
15	PGND2	Ground	Power Ground	Channel 2 Buck converter and discharge MOSFETs power ground
16	SW2	Input/Output	Switching Node	Channel 2 Buck converter switching node
17	PVIN2	Power	Power Input Voltage	Channel 2 Buck converter power input
18	BOOT2	Input	Bootstrap Input	Channel 2 Bootstrap capacitor input pin
19	ILIM1	Input	Soft Start Adjustment Input	Channel 1 soft start adjustment
20	NC	None	No Connect	No internal connections to this pin
21	FREQ	Input	Frequency Adjustment Input	The buck converters switching frequency adjustment input
22,23	VIN	Power	Input Supply Voltage	Power supply voltage of the IC
24	GND	Ground	Signal Ground	Analog ground of the IC
25	VDDI	Output	Internal Supply Voltage	Internal Supply Voltage Output
26	$\overline{\text{STBY}}$	Input	Standby Input	Standby mode input control pin

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Input Supply Voltage (VIN) Pin	V_{IN}	-0.3 to 7.0	V
High-Side MOSFET Drain Voltage (PVIN1, PVIN2) Pins	P_{VIN}	-0.3 to 7.0	V
Switching Node (SW1, SW2) Pins	V_{SW}	-0.3 to 7.5	V
BOOT1, BOOT2 Pins (Referenced to SW1, SW2 Pins Respectively)	V_{BOOT} - V_{SW}	-0.3 to 7.5	V
$\overline{PG}$, VOUT1, VOUT2, $\overline{SD}$, and $\overline{STBY}$ Pins	-	-0.3 to 7.0	V
VDDI, FREQ, ILIM1, INV1, INV2, COMP1, COMP2, VREFIN, and VREFOUT Pins	-	-0.3 to 3.0	V
Channel 1 Continuous Output Current (1)	I_{OUT1}	+5.0	A
Channel 2 Continuous Output Current (1)	I_{OUT2}	±3.0	A
ESD Voltage (2)			V
Human Body Model (3)	V_{ESD1}	±2000	
Charge Device Model	V_{ESD3}	±750	
THERMAL RATINGS			
Operating Ambient Temperature (4)	T_A	-40 to 85	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Peak Package Reflow Temperature During Reflow (5), (6)	T_{PPRT}	Note 6	°C
Maximum Junction Temperature	$T_{J(MAX)}$	+150	°C
Power Dissipation (T_A = 85 °C) (7)	P_D	2.03	W

Notes

1. Continuous output current capability so long as T_J is ≤ $T_{J(MAX)}$.
2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model (CDM).
3. SW1 pin complies with ±1000V Human Body Model.
4. The limiting factor is junction temperature, taking into account power dissipation, thermal resistance, and heatsinking.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
   Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
7. Maximum power dissipation at indicated ambient temperature.

Table 2. Maximum Ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RESISTANCE [8]			
Thermal Resistance, Junction to Ambient, Single-Layer Board (1s) [9]	$R_{\theta JA}$	93	°C/W
Thermal Resistance, Junction to Ambient, Four-Layer Board (2s2p) [10]	$R_{\theta JMA}$	32	°C/W
Thermal Resistance, Junction to Board [11]	R_{QJB}	13.6	°C/W

Notes

8. The PVIN, SW, and PGND pins comprise the main heat conduction paths.
9. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
10. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal. There are thermal vias connecting the package to the two planes in the board. (per JESD51-5)
11. Thermal resistance between the device and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40°C ≤ T_A ≤ 85°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
IC INPUT SUPPLY VOLTAGE (VIN)					
Input Supply Voltage Operating Range	V_{IN}	3.0	-	6.0	V
Input DC Supply Current (12) (Normal Mode: $\overline{SD}$ = 1 & $\overline{STBY}$ = 1, Unloaded Outputs)	I_{IN}	-	-	35	mA
Input DC Supply Current (12) (Standby Mode, $\overline{SD}$ = 1 & $\overline{STBY}$ = 0)	I_{INQ}	-	-	25	mA
Input DC Supply Current (12) (Shutdown Mode, $\overline{SD}$ = 0 & $\overline{STBY}$ = X)	I_{INOFF}	-	-	100	µA
INTERNAL SUPPLY VOLTAGE OUTPUT (VDDI)					
Internal Supply Voltage Range	V_{DDI}	2.35	2.5	2.65	V
CHANNEL 1 BUCK CONVERTER (PVIN1, SW1, PGND1, BOOT1, INV1, COMP1, ILIM1)					
CH 1 High-side MOSFET Drain Voltage Range	P_{VIN}	2.5	-	6.0	V
Output Voltage Adjustment Range (13)	V_{OUTHI1}	0.7	-	3.6	V
Output Voltage Accuracy (13), (14), (15)	-	-1.0	-	1.0	%
Line Regulation (13) (Normal Operation, V_{IN} = 3.0 V to 6.0 V, I_{OUT1} = +5.0 A)	REG_{LN1}	-1.0	-	1.0	%
Load Regulation (13) (Normal Operation, I_{OUT1} = 0.0 A to 5.0 A)	REG_{LD1}	-1.0	-	1.0	%
Error Amplifier Reference Voltage (13)	V_{REF1}	-	0.7	-	V
Output Undervoltage Threshold	V_{UVR1}	-1.5	-	-8.0	%
Output Overvoltage Threshold	V_{OVR1}	1.5	-	8.0	%
Continuous Output Current	I_{OUT1}	-	-	5.0	A
Over Current Limit	I_{LIM1}	-	6.5	-	A
Soft Start Adjusting Reference Voltage Range	V_{ILIM1}	1.25	-	V_{DDI}	V
Short Circuit Current Limit	I_{SHORT1}	-	8.5	-	A
High-Side N-CH Power MOSFET (M4) $R_{DS(ON)}$ (13) (I_{OUT1} = 1.0 A, V_{BOOT1} - V_{SW1}= 3.3 V)	$R_{DS(ON)HS1}$	15	-	50	mΩ

Notes

12. Section “MODES OF OPERATION”, page 15 has a detailed description of the different operating modes of the 34716
13. Design information only, this parameter is not production tested.
14. Overall output accuracy is directly affected by the accuracy of the external feedback network, 1% feedback resistors are recommended.
15. ±1% is assured at room temperature.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40°C ≤ T_A ≤ 85°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Side N-CH Power MOSFET (M5) $R_{DS(ON)}$ (16) (I_{OUT1} = 1.0 A, V_{IN} = 3.3 V)	$R_{DS(ON)LS1}$	15	-	50	mΩ
M2 $R_{DS(ON)}$ (V_{IN} = 3.3 V, M2 is on)	$R_{DS(ON)M2}$	2.0	-	4.0	Ω
PVIN1 Pin Leakage Current (Shutdown Mode)	I_{PVIN1}	-10	-	10	µA
INV1 Pin Leakage Current	I_{INV1}	-1.0	-	1.0	µA
Thermal Shutdown Threshold (16)	T_{SDFET1}	-	170	-	°C
Thermal Shutdown Hysteresis (16)	$T_{SDHYFET1}$	-	25	-	°C
CHANNEL 2 BUCK CONVERTER (PVIN2, SW2, PGND2, BOOT2, INV2, COMP2)					
CH 2 High-side MOSFET Drain Voltage Range	P_{VIN}	2.5	-	6.0	V
Output Voltage Adjustment Range (16)	V_{OUTHI2}	0.7	-	1.35	V
Output Voltage Accuracy (16), (17), (18)	-	-1.0	-	1.0	%
Line Regulation (16) (Normal Operation, V_{IN} = 3.0 V to 6.0 V, I_{OUT2} = ±3.0 A)	REG_{LN2}	-1.0	-	1.0	%
Load Regulation (16) (Normal Operation, I_{OUT2} = -3.0 A to 3.0 A)	REG_{LD2}	-1.0	-	1.0	%
Error Amplifier Common Mode Voltage Range (16), (19)	V_{REF2}	0.0	-	1.35	V
Output Undervoltage Threshold	V_{UVR2}	-1.5	-	-8.0	%
Output Overvoltage Threshold	V_{OVR2}	1.5	-	8.0	%
Continuous Output Current	I_{OUT2}	-3.0	-	3.0	A
Over Current Limit (Sinking and Sourcing)	I_{LIM2}	-	4.0	-	A
Short Circuit Current Limit (Sinking and Sourcing)	I_{SHORT2}	-	6.5	-	A
High-Side N-CH Power MOSFET (M6) $R_{DS(ON)}$ (16) (I_{OUT2} = 1.0 A, V_{BOOT2} - V_{SW2}= 3.3 V)	$R_{DS(ON)HS2}$	15	-	50	mΩ
Low-Side N-CH Power MOSFET (M7) $R_{DS(ON)}$ (16) (I_{OUT2} = 1.0 A, V_{IN} = 3.3 V)	$R_{DS(ON)LS2}$	15	-	50	mΩ
M3 $R_{DS(ON)}$ (V_{IN} = 3.3 V, M3 is on)	$R_{DS(ON)M3}$	2.0	-	4.0	Ω
PVIN2 Pin Leakage Current (Standby and Shutdown Modes)	I_{PVIN2}	-10	-	10	µA

Notes
16. Design information only, this parameter is not production tested.
17. Overall output accuracy is directly affected by the accuracy of the external feedback network, 1% feedback resistors are recommended
18. ±1% is assured at room temperature
19. The 1 % output voltage regulation is only guaranteed for a common mode voltage range greater than or equal to 0.7V

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40°C ≤ T_A ≤ 85°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INV2 Pin Leakage Current	I_{INV2}	-1.0	-	1.0	µA
Thermal Shutdown Threshold (20)	T_{SDFET2}	-	170	-	°C
Thermal Shutdown Hysteresis (20)	$T_{SDHYFET2}$	-	25	-	°C
OSCILLATOR (FREQ)					
Oscillator Frequency Adjusting Reference Voltage Range	V_{FREQ}	0.0	-	V_{DDI}	V
TRACKING (VREFIN, VREFOUT, VOUT1, VOUT2)					
VREFIN External Reference Voltage Range (20)	V_{REFIN}	0.0	-	2.7	V
VREFOUT Buffered Reference Voltage Range	V_{REFOUT}	0.0	-	1.35	V
VREFOUT Buffered Reference Voltage Accuracy (21)	-	-1.0	-	1.0	%
VREFOUT Buffered Reference Voltage Current Capability	I_{REFOUT}	0.0	-	8.0	mA
VREFOUT Buffered Reference Voltage Over Current Limit	$I_{REFOUTLIM}$	-	11	-	mA
VREFOUT Total Discharge Resistance (20)	$R_{TDR(M10)}$	-	50	-	Ω
VOUT1 Total Discharge Resistance (20)	$R_{TDR(M8)}$	-	50	-	Ω
VOUT2 Total Discharge Resistance (20)	$R_{TDR(M9)}$	-	50	-	Ω
VOUT2 Pin Leakage Current (Standby Mode, V_{OUT2} = 3.6 V)	$I_{VOUTLKG2}$	-1.0	-	1.0	µA
CONTROL AND SUPERVISORY ($\overline{\text{STBY}}$, $\overline{\text{SD}}$, $\overline{\text{PG}}$)					
$\overline{\text{STBY}}$ High Level Input Voltage	V_{STBYHI}	2.0	-	-	V
$\overline{\text{STBY}}$ Low Level Input Voltage	V_{STBYLO}	-	-	0.4	V
$\overline{\text{STBY}}$ Pin Internal Pull Up Resistor	R_{STBYUP}	1.0	-	2.0	MΩ
$\overline{\text{SD}}$ High Level Input Voltage	V_{SDHI}	2.0	-	-	V
$\overline{\text{SD}}$ Low Level Input Voltage	V_{SDLO}	-	-	0.4	V
$\overline{\text{SD}}$ Pin Internal Pull Up Resistor	R_{SDUP}	1.0	-	2.0	MΩ
$\overline{\text{PG}}$ Low Level Output Voltage (I_{PG} = 3.0 mA)	V_{PGLO}	-	-	0.4	V
$\overline{\text{PG}}$ Pin Leakage Current (M1 is off, Pulled up to VIN)	I_{PGLKG}	-	-	1.0	µA

Notes

20. Design information only, this parameter is not production tested.
21. The 1 % accuracy is only guaranteed for V_{REFOUT} greater than or equal to 0.7 V at room temperature.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40°C ≤ T_A ≤ 85°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CHANNEL 1 BUCK CONVERTER (PVIN1, SW1, PGND1, BOOT1, INV1, COMP1, ILIM1)					
Switching Node (SW1) Rise Time (22) (P_{VIN} = 3.3 V, IOUT1 = 5.0 A)	t_{RISE1}	-	8.0	-	ns
Switching Node (SW1) Fall Time (22) (P_{VIN} = 3.3 V, IOUT1 = 5.0 A)	t_{FALL1}	-	5.0	-	ns
Soft Start Duration (Normal Mode)	t_{SS1}				ms
ILIM1: 1.25V to 1.49V		-	3.2	-	
1.5V to 1.81V		-	1.6	-	
1.82V to 2.13V		-	0.8	-	
2.14V to 2.5V		-	0.4	-	
Over Current Limit Timer	t_{LIM1}	-	10	-	ms
Over Current Limit Retry Time-out Period	$t_{TIMEOUT1}$	80	-	120	ms
Output Undervoltage/Overvoltage Filter Delay Timer	$t_{FILTER1}$	5.0	-	25	µs
CHANNEL 2 BUCK CONVERTER (PVIN2, SW2, PGND2, BOOT2, INV2, COMP2)					
Switching Node (SW2) Rise Time (22) (P_{VIN} = 3.3 V, I_{OUT2} = ±3.0 A)	t_{RISE2}	-	28	-	ns
Switching Node (SW2) Fall Time (22) (P_{VIN} = 3.3 V, I_{OUT2} = ±3.0 A)	t_{FALL2}	-	12.0	-	ns
Soft Start Duration (Normal Mode)	t_{SS2}	-	1.6	-	ms
Over Current Limit Timer	t_{LIM2}	-	10	-	ms
Over Current Limit Retry Time-out Period	$t_{TIMEOUT2}$	80	-	120	ms
Output Undervoltage/Overvoltage Filter Delay Timer	$t_{FILTER2}$	5.0	-	25	µs
OSCILLATOR (FREQ) (23)					
Oscillator Default Switching Frequency (FREQ = GND)	f_{SW}	-	1.0	-	MHz
Oscillator Switching Frequency Range	f_{SW}	200	-	1000	kHz
CONTROL AND SUPERVISORY ($\overline{STBY}$, $\overline{SD}$, $\overline{PG}$)					
$\overline{PG}$ Reset Delay	$t_{PGRESET}$	8.0	-	12	ms
Thermal Shutdown Retry Time-out Period (22)	$t_{TIMEOUT}$	80	-	120	ms

Notes
22. Design information only, this parameter is not production tested.
23. Oscillator Frequency tolerance is ±10%.

FUNCTIONAL DESCRIPTION

INTRODUCTION

In modern microprocessor/memory applications, address commands and control lines require system level termination to a voltage (V_{TT}) equal to 1/2 the memory supply voltage (V_{DDQ}). Having the termination voltage at midpoint, the power supply insures symmetry for switching times. Also, a reference voltage (V_{REF}) that is free of any noise or voltage variations is needed for the DDR SDRAM input receiver, V_{REF} is also equal to 1/2 V_{DDQ}. Varying the V_{REF} voltage will effect the setup and hold time of the memory. To comply with DDR requirements and to obtain best performance, V_{TT} and V_{REF} need to be tightly regulated to track 1/2 V_{DDQ} across voltage, temperature, and noise margins. V_{TT} should track any variations in the DC V_{REF} value (V_{TT} = V_{REF} +/- 40 mV), (See Figure 4) for a DDR system level diagram.

The 34716 supplies the V_{DDQ}, V_{TT} and a buffered V_{REF} output. To ensure compliance with DDR specifications, the V_{DDQ} line is applied to the VREFIN pin and divided by 2 internally through a precision resistor divider. This internal voltage is then used as the reference voltage for the V_{TT} output. The same internal voltage is also buffered to give the V_{REF} voltage at the VREFOUT pin for the application to use without the need for an external resistor divider. The 34716 provides the tight voltage regulation and power sequencing/ tracking required along with handling the DDR peak transient current requirements. It gives the user a complete DDR power supply solution with optimum performance. Buffering the V_{REF} output helps its immunity against noise and load changes.

The 34716 utilizes a voltage mode synchronous buck switching converter topology with integrated low $R_{DS(ON)}$ (50 mΩ) N-channel power MOSFETs to provide an output voltage with an accuracy of less than ±2.0 % output voltage. It has a programmable switching frequency that allows for flexibility and optimization over the operating conditions and can operate at up to 1.0 MHz to significantly reduce the external components size and cost. The 34716 can supply up to 5.0 A from one output and sink and source up to 3.0 A of continuous current from the other output. It provides protection against output overcurrent, overvoltage, undervoltage, and overtemperature conditions. It also protects the system from short circuit events. It incorporates a power good output signal to alert the host when a fault occurs.

For boards that support the Suspend-To-RAM (S3) and the Suspend-To-Disk (S5) states, the 34716 offers the $\overline{\text{STBY}}$ and the $\overline{\text{SD}}$ pins respectively. Pulling any of these pins low, puts the IC in the corresponding state.

By integrating the control/supervisory circuitry along with the Power MOSFET switches for the buck converter into a space-efficient package, the 34716 offers a complete, small-size, cost-effective, and simple solution to satisfy the needs of DDR memory applications.

Besides DDR memory termination, the 34716 can be used to supply termination for other active buses and graphics card memory. It can be used in Netcom/Telecom applications like servers. It can also be used in desktop motherboards, game consoles, set top boxes, and high end high definition TVs.

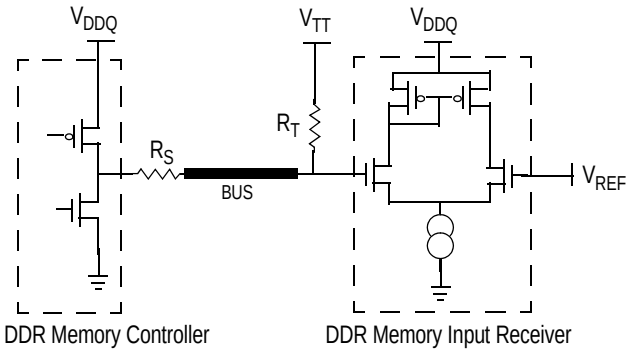


Figure 4. DDR System Level Diagram

FUNCTIONAL PIN DESCRIPTION

BOOTSTRAP INPUT (BOOT1, BOOT2)

Bootstrap capacitor input pin. Connect a capacitor (as discussed in Bootstrap capacitor on page 20) between this pin and the SW pin of the respective channel to enhance the gate of the high-side Power MOSFET during switching.

POWER INPUT VOLTAGE (PVIN1, PVIN2)

Buck converter power input voltage. This is the drain of the buck converter high-side power MOSFET.

SWITCHING NODE (SW1, SW2)

Buck converter switching node. This pin is connected to the output inductor.

POWER GROUND (PGND1, PGND2)

Buck converter and discharge MOSFETs power ground. It is the source of the buck converter low-side power MOSFET.

COMPENSATION INPUT (COMP1, COMP2)

Buck converter external compensation network connects to this pin. Use a type III compensation network.

ERROR AMPLIFIER INVERTING INPUT (INV1, INV2)

Buck converter error amplifier inverting input. Connect the V_{DDQ} voltage (channel 1) to INV1 pin through a resistor divider and connect the V_{TT} voltage (channel 2) directly to INV2 pin.

OUTPUT VOLTAGE DISCHARGE PATH (VOUT1, VOUT2)

Buck converters output voltage are connected to these pins. It only serves as the output discharge path once the $\overline{SD}$ signal is asserted.

INTERNAL SUPPLY VOLTAGE OUTPUT (VDDI)

This is the output of the internal bias voltage regulator. Connect a 1.0 µF, 6 V low ESR ceramic filter capacitor between this pin and the GND pin. Filtering any spikes on this output is essential to the internal circuitry stable operation.

SIGNAL GROUND (GND)

Analog ground of the IC. Internal analog signals are referenced to this pin voltage.

INPUT SUPPLY VOLTAGE (VIN)

IC power supply input voltage. Input filtering is required for the device to operate properly.

POWER GOOD OUTPUT SIGNAL ($\overline{PG}$)

This is an active low open drain output that is used to report the status of the device to a host. This output activates after a successful power up sequence and stays active as long as the device is in normal operation and is not experiencing any faults. This output activates after a 10 ms delay and must be pulled up by an external resistor to a supply voltage like V_{IN}.

STANDBY INPUT ($\overline{STBY}$)

If this pin is tied to the GND pin, the device will be in Standby Mode. If left unconnected or tied to the VIN pin, the device will be in Normal Mode. The pin has an internal pull up of 1.5 MΩ. This input accepts the S3 (Suspend-To-RAM) control signal.

SHUTDOWN INPUT ($\overline{SD}$)

If this pin is tied to the GND pin, the device will be in Shutdown Mode. If left unconnected or tied to the VIN pin, the device will be in Normal Mode. The pin has an internal pull up of 1.5 MΩ. This input accepts the S5 (Suspend-To-Disk) control signal.

REFERENCE VOLTAGE OUTPUT (VREFOUT)

This is a buffered reference voltage output that is equal to 1/2 V_{REFIN}. It has a 10.0 mA current drive capability. This output is used as the V_{REF} voltage rail and should be filtered against any noise. Connect a 0.1 µF, 6 V low ESR ceramic filter capacitor between this pin and the GND pin and between this pin and V_{DDQ} rail. V_{REFOUT} is also used as the reference voltage for the buck converter error amplifier.

REFERENCE VOLTAGE INPUT (VREFIN)

The output of channel two will track 1/2 the voltage applied at this pin.

FREQUENCY ADJUSTMENT INPUT (FREQ)

The buck converters switching frequency can be adjusted by connecting this pin to an external resistor divider between VDDI and GND pins. The default switching frequency (FREQ pin connected to ground, GND) is set at 1.0 MHz.

CHANNEL 1 SOFT START ADJUSTMENT INPUT (ILIM1)

Channel one Soft Start can be adjusted by applying a voltage between 1.25V and V_{DDI}.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

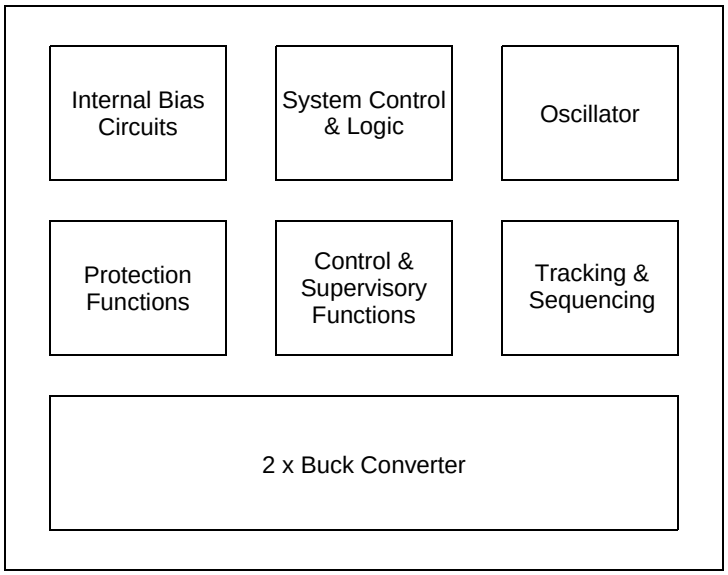


Figure 5. Block Illustration

INTERNAL BIAS CIRCUITS

This block contains all circuits that provide the necessary supply voltages and bias currents for the internal circuitry. It consists of:

- Internal Voltage Supply Regulator: This regulator supplies the V_{DDI} voltage that is used to drive the digital/analog internal circuits. It is equipped with a Power-On-Reset (POR) circuit that watches for the right regulation levels. External filtering is needed on the VDDI pin. This block will turn off during the shutdown mode.
- Internal Bandgap Reference Voltage: This supplies the reference voltage to some of the internal circuitry.
- Bias Circuit: This block generates the bias currents necessary to run all of the blocks in the IC.

SYSTEM CONTROL AND LOGIC

This block is the brain of the IC where the device processes data and reacts to it. Based on the status of the $\overline{\text{STBY}}$ and $\overline{\text{SD}}$ pins, the system control reacts accordingly and orders the device into the right status. It also takes inputs from all of the monitoring/protection circuits and initiates power up or power down commands. It communicates with the buck converter to manage the switching operation and protects it against any faults.

OSCILLATOR

This block generates the clock cycles necessary to run the IC digital blocks. It also generates the buck converters switching frequency. The switching frequency can be programmed by connecting a resistor divider to the FREQ pin, between VDDI and GND pins (See Figure 1, page 1).

PROTECTION FUNCTIONS

This block contains the following circuits:

- Over Current Limit and Short Circuit Detection: This block monitors the output of the buck converters for over current conditions and short circuit events and alerts the system control for further command.
- Thermal Limit Detection: This block monitors the temperature of the device for overheating events. If the temperature rises above the thermal shutdown threshold, this block will alert the system control for further commands.
- Output Overvoltage and Undervoltage Monitoring: This block monitors the buck converters output voltages to ensure they are within regulation boundaries. If not, this block alerts the system control for further commands.

CONTROL AND SUPERVISORY FUNCTIONS

This block is used to interface with an outside host. It contains the following circuits:

- Standby Control Input: An outside host can put the 34716 device into standby mode (S3 or Suspend-To-RAM mode) by sending a logic “0” to the $\overline{\text{STBY}}$ pin.
- Shutdown Control Input: An outside host can put the 34716 device into shutdown mode (S5 or Suspend-To-Disk mode) by sending a logic “0” to the $\overline{\text{SD}}$ pin.
- Power Good Output Signal: The 34716 can communicate to an outside host that a fault has occurred by pulling the voltage on the $\overline{\text{PG}}$ pin high through a pull up resistor.

TRACKING AND SEQUENCING

This block allows the output of channel 2 of the 34716 to track 1/2 the voltage applied at the VREFIN pin. This allows the V_{REF} and V_{TT} voltages to track 1/2 V_{DDQ} and assures that none of them will be higher than V_{DDQ} at any point during normal operating conditions. For power down during a shutdown (S5) mode, the 34716 uses internal discharge MOSFETs (M8, M9, and M10 on Figure 2, page 2) to discharge V_{DDQ}, V_{TT}, and V_{REF} respectively. These discharge MOSFETs are only active during shutdown mode. Using this block along with controlling the $\overline{SD}$ and $\overline{STBY}$ pins can offer the user the device for power sequencing by controlling when to turn the 34716 outputs on or off.

BUCK CONVERTER

This block provides the main function of the 34716: DC to DC conversion from an un-regulated input voltage to a regulated output voltage used by the loads for reliable operation. The buck converter is a high performance, fixed frequency (externally adjustable), Syncronous buck PWM voltage-mode control with a minimum on time of 100ns. It drives integrated 50 mΩ N-channel power MOSFETs saving board space and enhancing efficiency. The switching regulator output voltage is adjustable with an accuracy of less than ±2 % to meet DDR requirements. The regulator's voltage control loop is compensated using a type III compensation network, with external components to allow for optimizing the loop compensation, for a wide range of operating conditions. A typical Bootstrap circuit with an internal PMOS switch is used to provide the voltage necessary to properly enhance the high-side MOSFET gate.

The 34716 is designed to address DDR memory power supplies. The integrated converter has the ability to supply up to 5.0 A out of channel 1 and sink and source up to 3.0 A of continuous current from channel 2, providing a full power supply solution for DDR applications.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

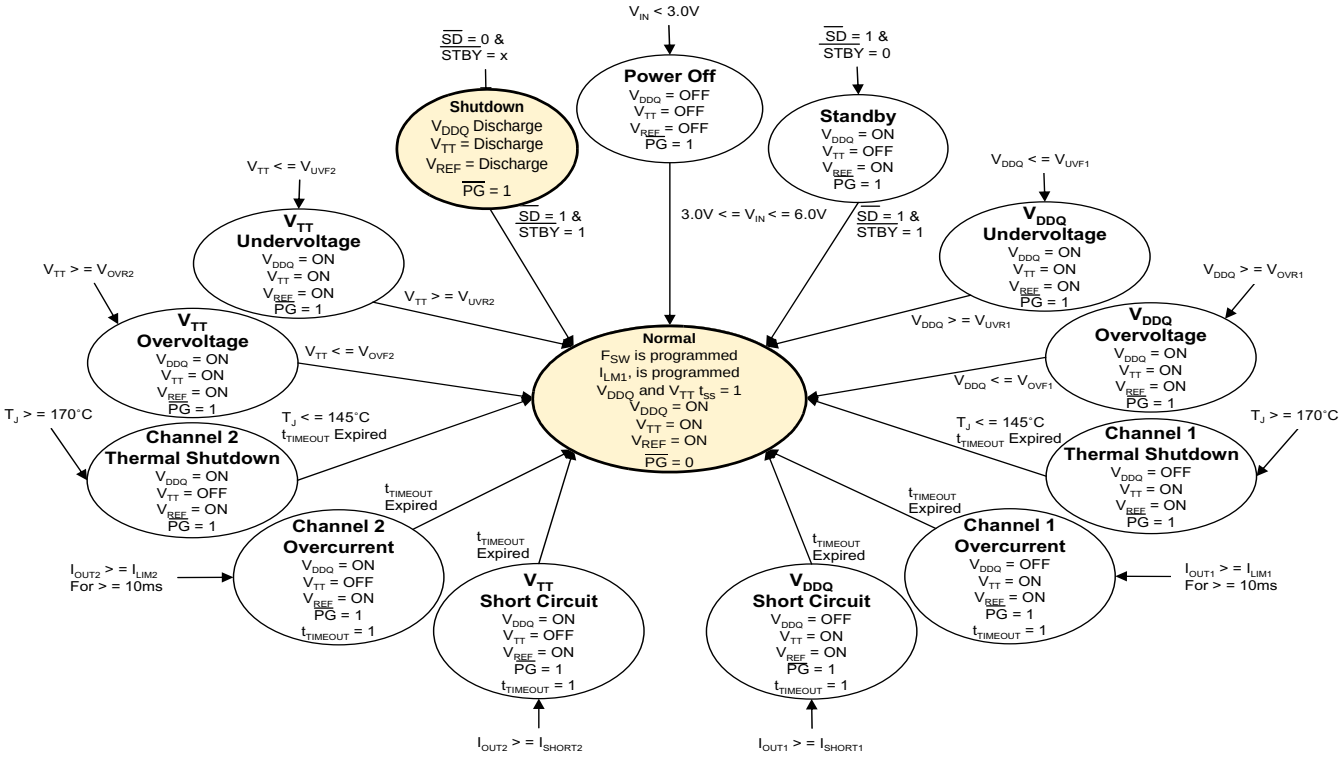


Figure 6. Operation Modes Diagram

MODES OF OPERATION

The 34716 has three primary modes of operation:

Normal Mode

In normal mode, all functions and outputs are fully operational. To be in this mode, the V_{IN} needs to be within its operating range, both Shutdown and Standby inputs are high, and no faults are present. This mode consumes the most amount of power.

Standby Mode

This mode is predominantly used in Desktop memory solutions where the DDR supply is desired to be ACPI compliant (Advanced Configuration and Power Interface). When this mode is activated by pulling the $\overline{STBY}$ pin low, V_{TT} is put in High Z state, I_{OUT2} = 0 A while V_{DDQ} and V_{REF} stay active. This is the S3 state Suspend-To-Ram or Self Refresh mode and it is the lowest DRAM power state. In this mode, the DRAM will preserve the data. While in this mode, the 34716 consumes less power than in the normal mode, because the buck converter and most of the internal blocks are disabled.

Shutdown Mode

In this mode, activated by pulling the $\overline{SD}$ pin low, the chip is in a shutdown state and the outputs are all disabled and discharged. This is the S4/S5 power state or Suspend-To-Disk state, where the DRAM will loose all of its data content (no power supplied to the DRAM). The reason to discharge the V_{TT} and V_{REF} lines is to ensure upon exiting, the Shutdown Mode that V_{TT} and V_{REF} are lower than V_{DDQ}, otherwise V_{TT} can remain floating high, and be higher than V_{DDQ} upon powering up. In this mode, the 34716 consumes the least amount of power since almost all of the internal blocks are disabled.

START-UP SEQUENCE

When power is first applied, the 34716 checks the status of the $\overline{SD}$ and $\overline{STBY}$ pins. If the device is in a shutdown mode, no block will power up and the output will not attempt to ramp. If the device is in a standby mode, only the V_{DDI} internal supply voltage and the bias currents are established and no further activities will occur. Once the $\overline{SD}$ and $\overline{STBY}$ pins are released to enable the device, the internal V_{DDI} POR signal is also released. The rest of the internal blocks will be enabled, and the buck converters switching frequency and the V_{DDQ} Soft start values are determined by reading the FREQ and

ILIM1 pins respectively. A soft start cycle is then initiated to ramp up the outputs. While channel 1 buck converter uses an internal reference, channel 2 converter error amplifier uses the voltage on the VREFOUT pin (V_{REF}) as its reference voltage. V_{REF} is equal to 1/2 V_{DDQ}, where V_{DDQ} is applied to the VREFIN pin. This way, the 34716 assures that V_{REF} and V_{TT} voltages track 1/2 V_{DDQ} to meet DDR requirements.

Soft start is used to prevent the output voltage from overshooting during startup. At initial startup, the output capacitor is at zero volts; V_{OUT} = 0 V. Therefore, the voltage across the inductor will be PV_{IN} during the capacitor charge phase which will create a very sharp di/dt ramp. Allowing the inductor current to rise too high can result in a large difference between the charging current and the actual load current that can result in an undesired voltage spike once the capacitor is fully charged. The soft start is active each time the IC goes out of standby or shutdown mode, power is recycled, or after a fault retry.

To fully take advantage of soft starting, it is recommended not to enable the V_{TT} output before introducing VDDQ on the VREFIN pin. If this happens after a soft start cycle expires and the VREFIN voltage has a high dv/dt, the output will naturally track it immediately and ramp up with a fast dv/dt itself and that will defeat the purpose of soft starting. For reliable operation, it is best to have the VDDQ voltage available before enabling the V_{TT} output.

After a successful start-up cycle where the device is enabled, no faults have occurred, and the output voltages have reached their regulation point, the 34716 pulls the power good output signal low after a 10 ms reset delay, to indicate to the host that the device is in normal operation.

PROTECTION FUNCTIONS

The 34716 monitors the application for several fault conditions to protect the load from overstress. The reaction of the IC to these faults ranges from turning off the outputs to just alerting the host that something is wrong. In the following paragraphs, each fault condition is explained:

Output Overvoltage

An overvoltage condition occurs once the output voltage goes higher than the rising overvoltage threshold (V_{OVR}). In this case, the power good output signal is pulled high, alerting the host that a fault is present, but the outputs will stay active. To avoid erroneous overvoltage conditions, a 20 µs filter is implemented. The buck converter will use its feedback loop to attempt to correct the fault. Once the output voltage falls below the falling overvoltage threshold (V_{OVF}), the fault is cleared and the power good output signal is pulled low, the device is back in normal operation. The condition is the same for both outputs.

Output Undervoltage

An undervoltage condition occurs once the output voltage falls below the falling undervoltage threshold (V_{UVF}). In this case, the power good output signal is pulled high, alerting the host that a fault is present, but the outputs will stay active. To avoid erroneous undervoltage conditions, a 20 µs filter is implemented. The buck converter will use its feedback loop to attempt to correct the fault. Once the output voltage rises above the rising undervoltage threshold (V_{UVR}), the fault is cleared and the power good output signal is pulled low, the device is back in normal operation. The condition is the same for both outputs.

Output Over Current

This block detects over current in the Power MOSFETs of the buck converter. It is comprised of a sense MOSFET and a comparator for each channel. The sense MOSFET acts as a current detecting device by sampling a ratio of the load current. That sample is compared via the comparator with an internal reference to determine if the output is in over current or not. If the peak current in the output inductor reaches the over current limit (I_{LIM}), the converter will start a cycle-by-cycle operation to limit the current, and a 10 ms over current limit timer (t_{LIM}) starts. The converter will stay in this mode of operation until one of the following occurs:

- The current is reduced back to the normal level before t_{LIM} expires, and in this case normal operation is regained.
- t_{LIM} expires without regaining normal operation, at which point the device turns off the output and the power good output signal is pulled high. At the end of a time-out period of 100 ms ($t_{TIMEOUT}$), the device will attempt another soft start cycle.
- The device reaches the thermal shutdown limit (T_{SDFET}) and turns off the output. The power good ($\overline{PG}$) output signal is pulled high.
- The output current keeps increasing until it reaches the short circuit current limit (I_{SHORT}). See below for more details.

Short Circuit Current Limit

This block uses the same current detection mechanism as the over current limit detection block. If the load current reaches the I_{SHORT} value, the device reacts by shutting down the output immediately. This is necessary to prevent damage in case of a permanent short circuit. Then, at the end of a time-out period of 100 ms ($t_{TIMEOUT}$), the device will attempt another soft start cycle.

Thermal Shutdown

Each channel has its own thermal shutdown block. Thermal limit detection block monitors the temperature of the device and protects against excessive heating. If the temperature reaches the thermal shutdown threshold (T_{SDFET}), the converter output switches off and the power good output signal indicates a fault by pulling high. The device will stay in this state until the temperature has decreased by the hysteresis value and then After a time-out period ($T_{TIMEOUT}$) of 100 ms, the device will retry automatically and the output will go through a soft start cycle. If successful normal operation is regained, the power good output signal is asserted low to indicate that.

TYPICAL APPLICATIONS

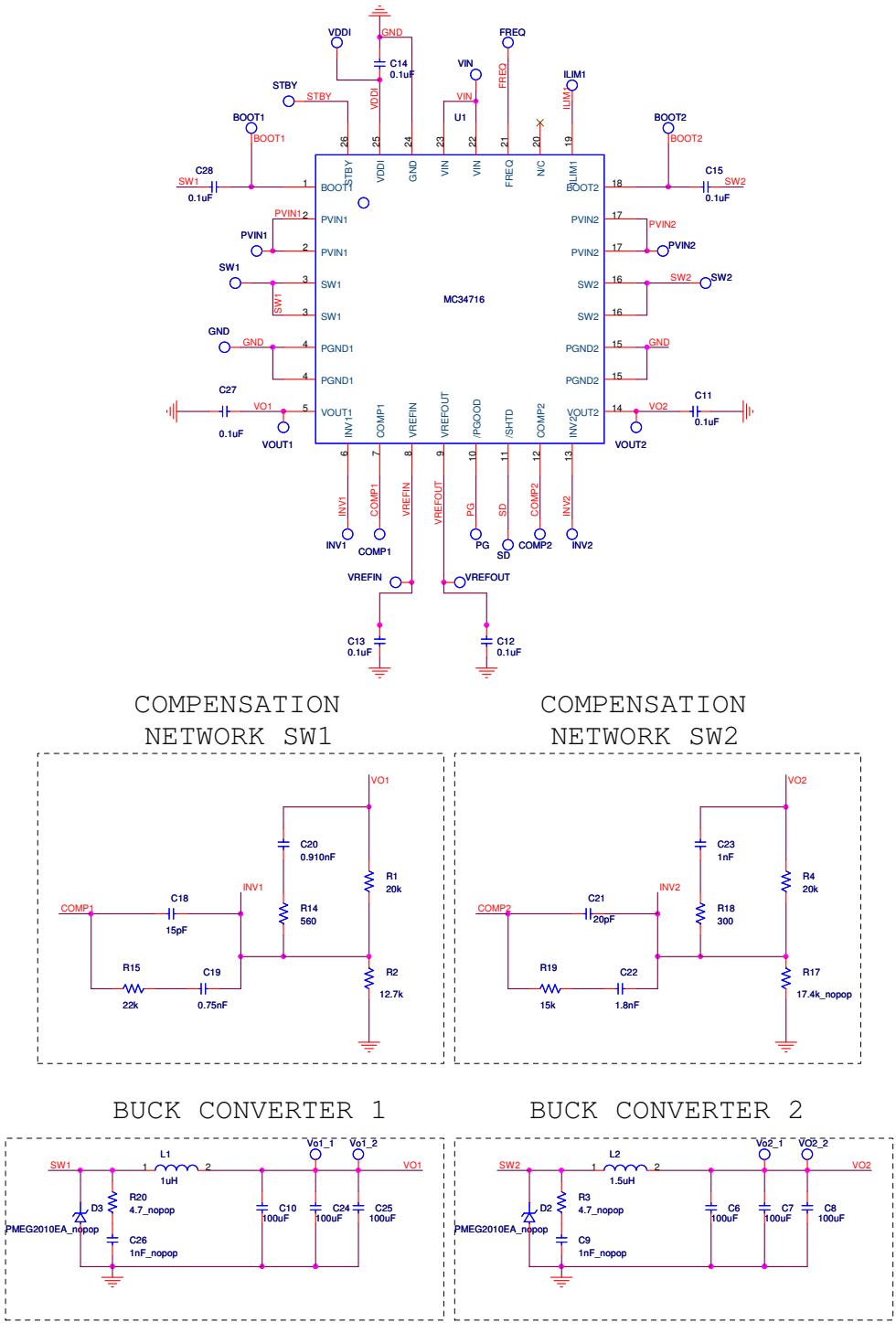


Figure 7. 34716 Typical Application

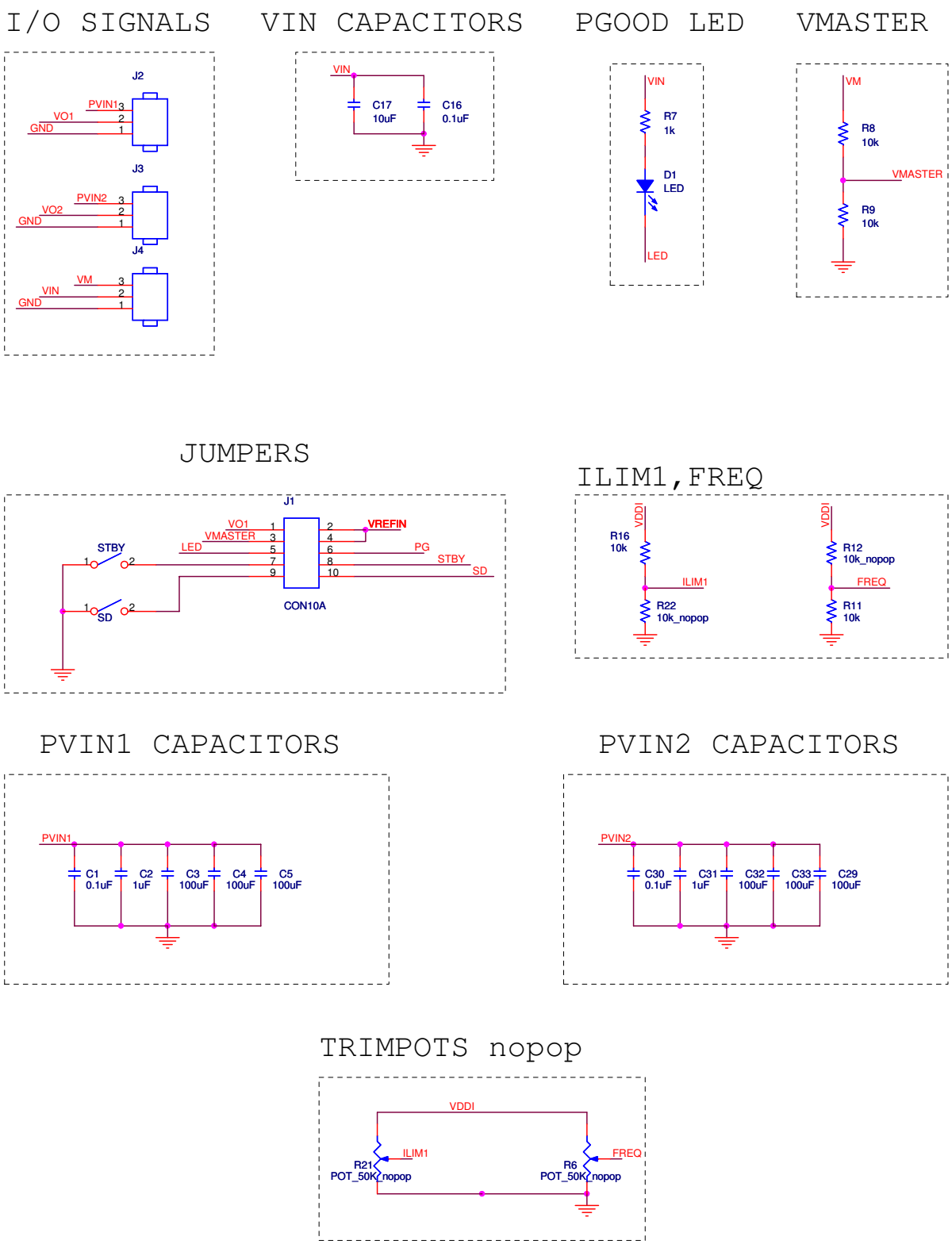


Figure 8. 34716 Typical Application

CONFIGURING THE OUTPUT VOLTAGE:

Channel 1 of the 34716 is a general purpose DC-DC converter, the resistor divider to the -INV1 node is responsible for setting the output voltage, according to the following equation:

$$V_{OUT} = V_{REF}\left(\frac{R1}{R2}+1\right)$$

Where V_{REF} is the internal V_{BG}=0.7V.

Channel 2 is a DDR specific voltage power supply, and the output voltage is given by the equation:

$$V_{TT} = \frac{V_{REFIN}}{2}$$

Where V_{REFIN} is equal to V_{DDQ}.

SWITCHING FREQUENCY CONFIGURATION

The switching frequency will have a value of 1.0 MHz by connecting the FREQ terminal to the GND. If the smallest frequency value of 200 KHz is desired, then connect the FREQ terminal to VDDI. To program the switching frequency to another value, an external resistor divider will be connected to the FREQ terminal to achieve the voltages given by Table 5.

FREQUENCY	VOLTAGE APPLIED TO PIN FREQ
200	2.341 – 2.500
253	2.185 - 2.340
307	2.029 - 2.184
360	1.873 - 2.028
413	1.717 – 1.872
466	1.561 – 1.716
520	1.405 - 1.560
573	1.249 - 1.404
627	1.093 - 1.248
680	0.936 - 1.092
733	0.781 - 0.936
787	0.625 - 0.780
840	0.469 - 0.624
893	0.313 - 0.468
947	0.157 - 0.312
1000	0.000 - 0.156

Table 5. Frequency Selection Table

SOFT START ADJUSTMENT

Table 6 shows the voltage that should be applied to the ILIM1 terminal to get the desired desired sort start timing on channel 1 only.

SOFT START [MS]	VOLTAGE APPLIED TO ILIM
3.2	1.19 - 1.49V
1.6	1.50 - 1.81V
0.8	1.82 - 2.13V
0.4	2.14 - 2.50V

Table 6. Soft Start Configurations

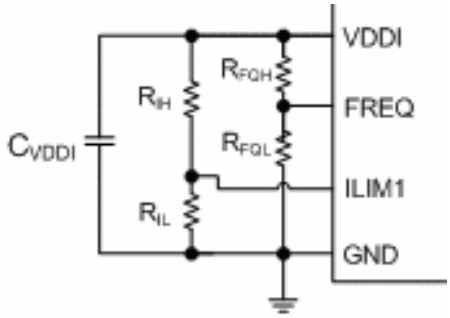


Figure 9. Resistor divider for Frequency and Soft Start adjustment

SELECTING INDUCTOR

Inductor calculation process is the same for both Channels. The equation is the following:

$$L = D'_{MAX} * T * \frac{(V_{out} + I_{out} * (Rds(on)_ls + r_w))}{\Delta I_{out}}$$

$D'_{MAX} = 1 - \frac{V_{out}}{Vin_\max}$ Maximum Off Time Percentage

T Switching Period

$Rds(on)_ls$ Drain – to – Source Resistance of FET

r_w Winding Resistance of Inductor

$\Delta I_{OUT} = 0.4 * I_{OUT}$ Output Current Ripple

If channel 1 will be serving as power supply for channel 2, it is necessary to locate the LC poles at different frequencies in order to ensure that the input impedance of the second converter is always higher than the output impedance of the first converter, and thus, ensure system stability. This can be achieved by selecting different values for L1 and L2 slightly higher than the calculated value.

SELECTING THE OUTPUT FILTER CAPACITOR

For the output capacitor, the following considerations are most important and not the actual Farad value: the physical size, the ESR of the capacitor, and the voltage rating.

Calculate the minimum output capacitor using the following formula:

$$Co = \frac{I_{OUT} * dt_I_rise}{TR_V_dip}$$

Transient Response percentage:
TR_%

Maximum Transient Voltage:
TR_V_dip = V_{OUT}*TR_%

Maximum Current Step:

$$\Delta Iout_step = \frac{(Vin_\min - Vout) * D_\max}{Fsw * L}$$

Inductor Current Rise Time:

$$dt_I_rise = \frac{T * I_{OUT}}{\Delta I_{OUT}_step}$$

The following formula will be helpful to find the maximum allowed ESR.

$$ESR_{\max} = \frac{\Delta V_{OUT} * Fsw * L}{V_{OUT}(1 - D\min)}$$

The effects of the ESR is often neglected by the designers and may present a hidden danger to the ultimate supply stability. Poor quality capacitors have widely disparate ESR value, which can make the closed loop response inconsistent.

BOOTSTRAP CAPACITOR

The bootstrap capacitor is needed to supply the gate voltage for the high side MOSFET. This N-Channel MOSFET needs a voltage difference between its gate and source to be able to turn on. The high side MOSFET source is the SW node, so it is not at ground and it is floating and shifting in voltage. We cannot just apply a voltage directly to the gate of the high side that is referenced to ground. We need a voltage referenced to the SW node. This is why the bootstrap capacitor is needed. This capacitor charges during the high-side off time. Since the low side will be on during that time, the SW node and the bottom of the bootstrap capacitor will be connected to ground, and the top of the capacitor will be connected to a voltage source. The capacitor will charge up to that voltage source (for example 5V). Now when the low side MOSFET switches off and the high side MOSFET switches on, the SW nodes rise to V_{IN}, and the voltage on the boot pin will be $V_{CAP} + V_{IN}$. The gate of the high side will have V_{CAP} across it and it will be able to stay enhanced. **A 0.1μF capacitor is a good value for this bootstrap element.**

TYPE III COMPENSATION NETWORK

Power supplies are desired to offer accurate and tight regulation output voltages. A high DC gain is required to accomplish this, but with high gain comes the possibility of instability. The purpose of adding compensation to the internal error amplifier is to counteract some of the gains and phases contained in the control-to-output transfer function that could jeopardized the stability of the power supply. The Type III compensation network used for 34716 is comprised of two poles (one integrator and one high frequency, to cancel the zero generated from the ESR of the output capacitor) and two zeros to cancel the two poles generated from the LC filter as shown in Figure 10.

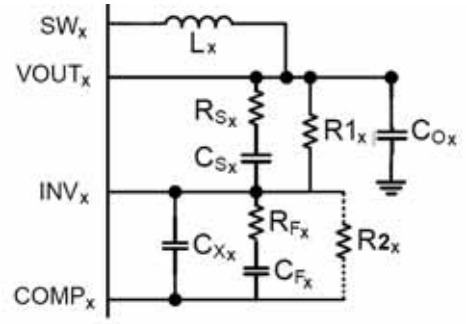


Figure 10. Type III compensation network

1. Choose a value for R1 (R2only applies to Channel 1)
2. Consider a Crossover frequency of one tenth of the switching frequency, set the Zero pole frequency to Fcross/10

$$F_{P0} = \frac{1}{10} F_{CROSS} = \frac{1}{2\pi * R_1 C_F}$$

$$C_F = \frac{1}{2\pi * R_1 F_{PO}}$$

3. Knowing the LC frequency, the Frequency of Zero 1 and Zero 2 in the compensation network is equal to F_{LC}

$$F_{LC} = \frac{1}{2\pi\sqrt{L_X C_{OX}}} = F_{Z1} = F_{Z2}$$

$$F_{Z1} = \frac{1}{2\pi * R_F C_F} \qquad F_{Z2} = \frac{1}{2\pi * R_1 C_S}$$

This gives the result

$$R_F = \frac{1}{2\pi * C_F F_{Z1}} \qquad C_S = \frac{1}{2\pi * R_1 F_{Z2}}$$

4. Calculate R_S by placing the first pole at the ESR zero frequency

$$F_{ESR} = \frac{1}{2\pi * Co_X * ESR} = F_{P1}$$

$$F_{P1} = \frac{1}{2\pi * R_S C_S} \rightarrow R_S = \frac{1}{2\pi * F_{P1} C_S}$$

5. Equating pole 2 at the Crossover Frequency to achieve a faster response and a proper phase margin

$$F_{CROSS} = F_{P2} = \frac{1}{2\pi * R_F \dfrac{C_F Cx}{C_F + C_x}} \rightarrow$$

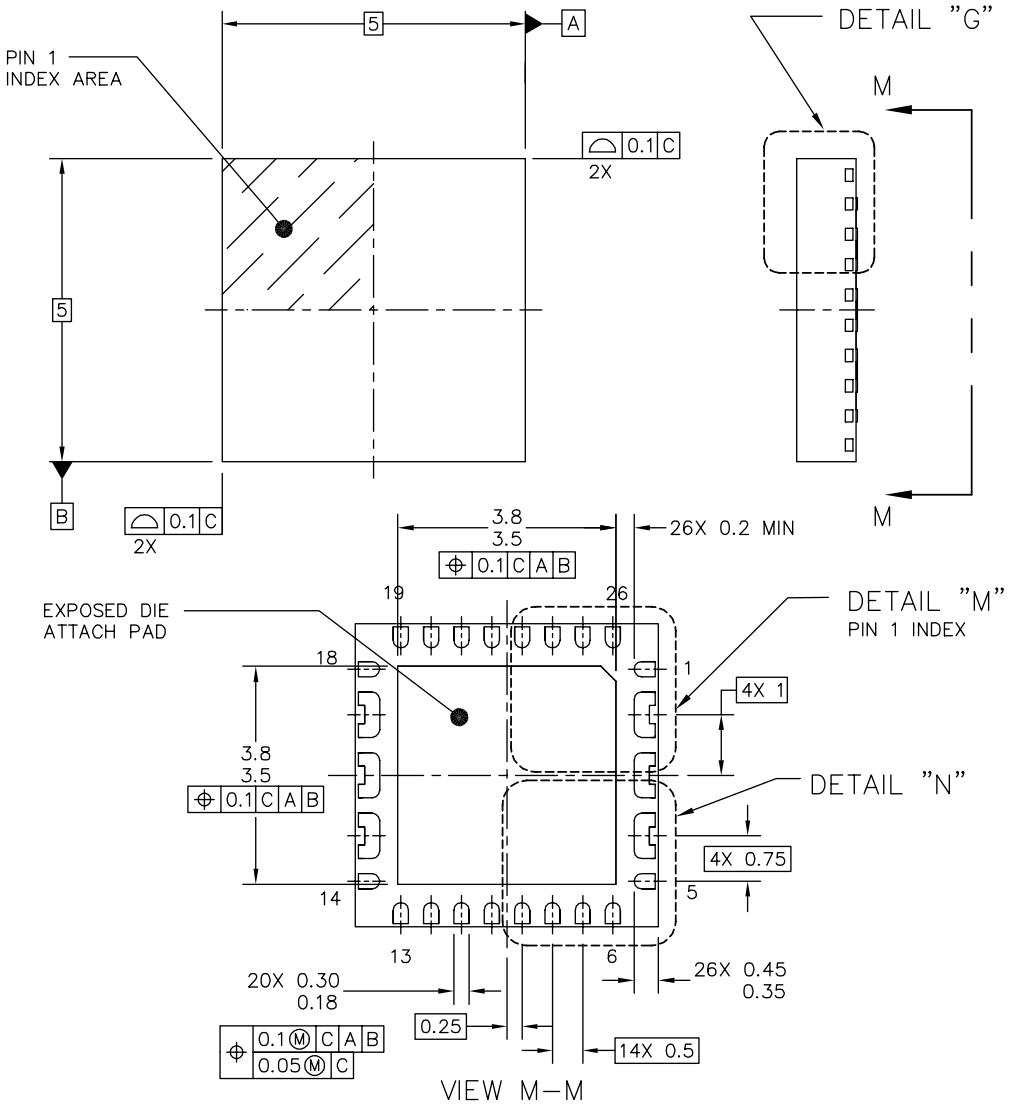
$$C_X = \frac{C_F}{2\pi * R_F C_F F_{P2} - 1}$$

TRACKING CONFIGURATIONS

The 34716 allows default Ratiometric tracking on channel 2 by connecting VDDQ to the VREFIN terminal. It has an internal resistor divider that allows an output of VDDQ/2.

PACKAGING

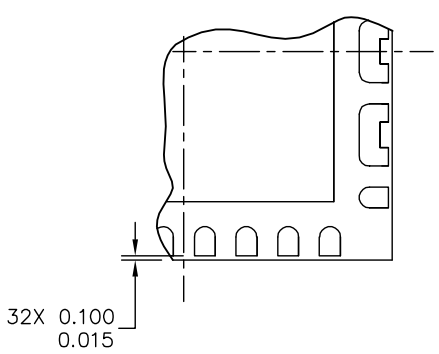
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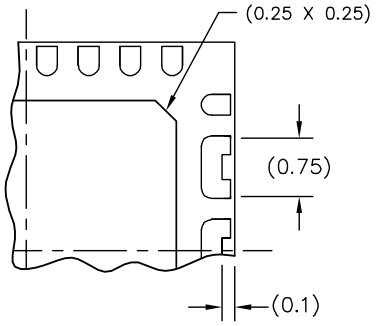
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	CASE NUMBER: 1851–01	25 APR 2006
	STANDARD: NON–JEDEC	

EP SUFFIX
26-PIN
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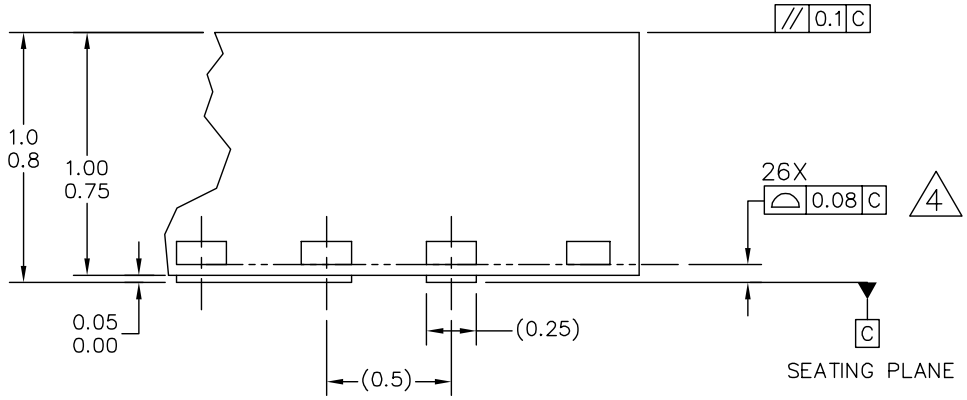
34716



DETAIL "N"
CORNER CONFIGURATION



DETAIL "M"
BACKSIDE PIN 1 INDEX



DETAIL "G"
VIEW ROTATED 90° CW

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	STANDARD: NON–JEDEC	

EP SUFFIX
26-PIN
98ASA10728D
ISSUE 0

34716

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	2/2006	• Pre-release version • Implemented Revision History page
2.0	2/2007	• Initial release • Converted format from Market Assessment to Product Preview • Major updates to the data, form, and style
3.0	5/2007	• Changed Feature fom 2% to 1%, relabeled to include soft start • Change references for 45 mΩ Integrated N-Channel Power MOSFETs to 50 mΩ • Removed Machine Model in Maximum Ratings • Changed Input DC Supply Current (12) , Input DC Supply Current (12), and Input DC Supply Current (12) • Added CH 1 High-side MOSFET Drain Voltage Range • Changed Output Voltage Accuracy (13), (14), (15) • Changed Soft Start Adjusting Reference Voltage Range and Short Circuit Current Limit • Changed High-Side N-CH Power MOSFET (M4) RDS(ON) (13) and Low-Side N-CH Power MOSFET (M5) RDS(ON) (16) • Changed M2 RDS(ON) and PVIN1 Pin Leakage Current • Added CH 2 High-side MOSFET Drain Voltage Range • Changed Output Voltage Accuracy (16), (17), (18) • Changed Short Circuit Current Limit (Sinking and Sourcing) • Changed High-Side N-CH Power MOSFET (M6) RDS(ON) (16) and Low-Side N-CH Power MOSFET (M7) RDS(ON) (16) • Changed M3 RDS(ON) and PVIN2 Pin Leakage Current • Changed VREFOUT Buffered Reference Voltage Accuracy (21), VREFOUT Buffered Reference Voltage Current Capability, and VREFOUT Buffered Reference Voltage Over Current Limit • Changed STBY Pin Internal Pull Up Resistor and SD Pin Internal Pull Up Resistor • Changed Soft Start Duration (Normal Mode) • Changed Over Current Limit Retry Time-out Period and Output Undervoltage/Overvoltage Filter Delay Timer • Changed Oscillator Default Switching Frequency, PG Reset Delay, and Thermal Shutdown Retry Time-out Period (22) • Changed definition for Channel 1 Soft Start ADJUStment input (ILIM1) • Changed drawings in 34716 Typical Application • Changed table for Soft Start Adjustment • Removed PC34716EP/R2 from the ordering information and added MC34716EP/R2 • Changed data sheet status to Advance Information

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