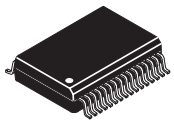
Document Number: MC33730
Rev. 6.0, 2/2010

RoHS

Switch Mode Power Supply with Multiple Linear Regulators

33730

SWITCHING POWER SUPPLY



EK SUFFIX (PB-FREE)
98ARL10543D
32-LEAD SOICW-EP

The 33730 is a multiple output power supply integrated circuit for automotive applications. The integrated circuit (IC) incorporates a switching regulator, which operates over a wide input voltage range from 4.5 to 26.5 V.

The step-down switching regulator uses a fixed frequency PWM voltage mode control. It has a 3.5 A current limit (typical) and the slew-rate is adjustable via a control pin to reduce switching noise. The switching regulator has an adjustable frequency oscillator, which allows the user to optimize its operation over a wide range of input voltages and component values.

The linear regulators can be configured either as two normal mode regulators (V_{DD3}, V_{DDL}) and one standby regulator (V_{KAM}), or as one normal mode linear regulator (V_{DDL}) and two standby regulators (V_{KAM} and V_{DD3} Standby). Two protected outputs [VREF (1, 2)] are used to provide power to external sensors.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MCZ33730EK/R2	-40°C to 125°C	32-SOICW-EP

Features

- Provides all regulated voltages for Freescale 32-bit microcontroller family
- Adjustable frequency switching buck regulator with slew-rate control
- Power sequencing provided
- Programmable voltages V_{DDL}, V_{DD3} - 3% accuracy
- Programmable standby regulator V_{KAM} - 15% accuracy, operating down to 4.5 V at the KA_VBAT pin
- V_{DD3} can be programmed as an optional second standby regulator with 15% accuracy
- Provides two 5.0 V protected supplies for sensors
- Provides reverse battery protection FET gate drive
- Provides necessary MCU monitoring and fail-safe support
- Pb-free packaging designated by suffix code EK

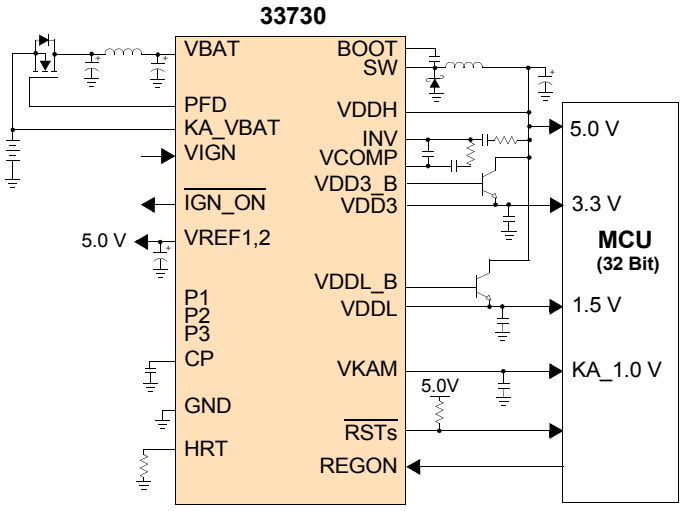


Figure 1. 33730 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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freescale semiconductor

INTERNAL BLOCK DIAGRAM

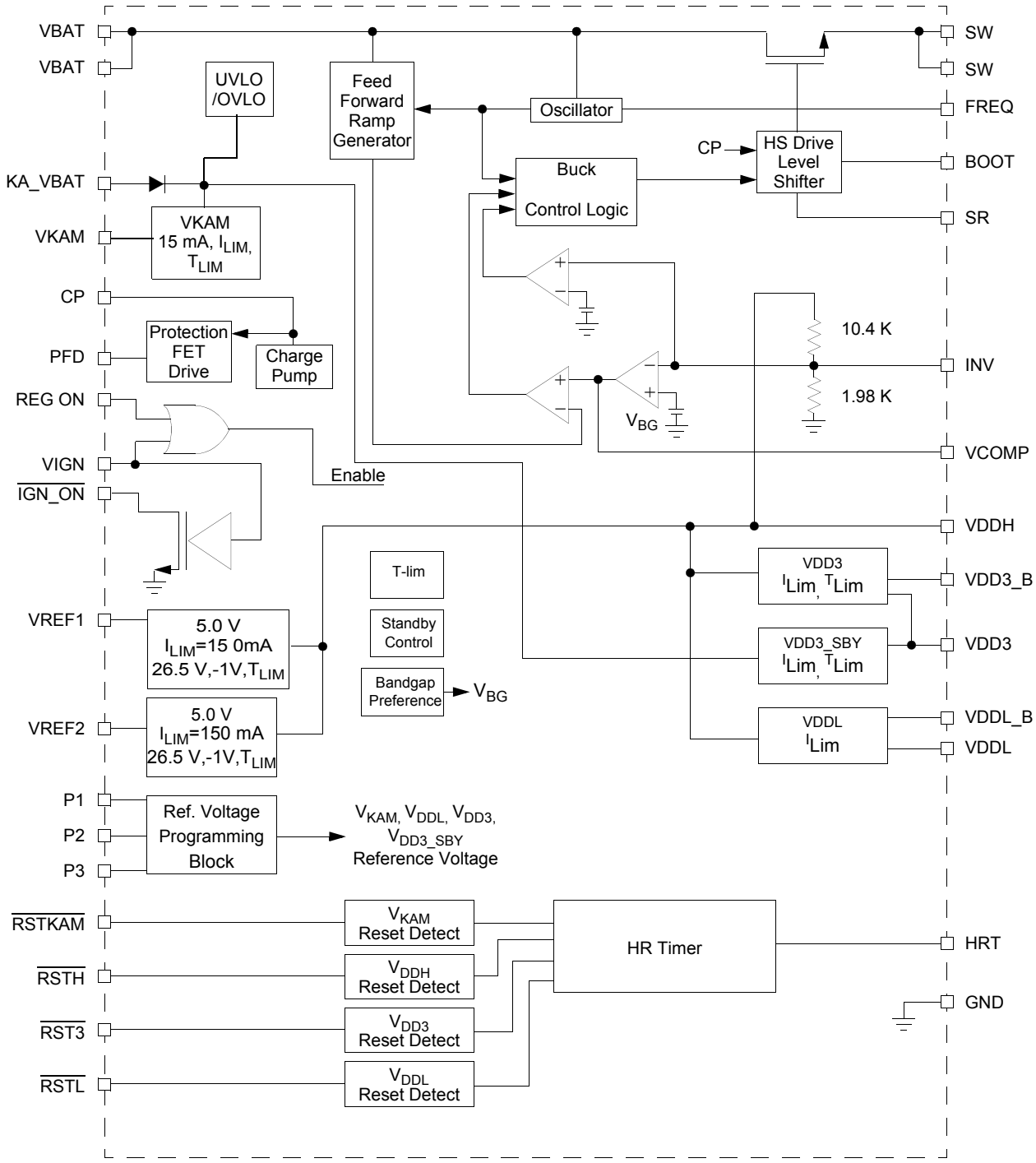
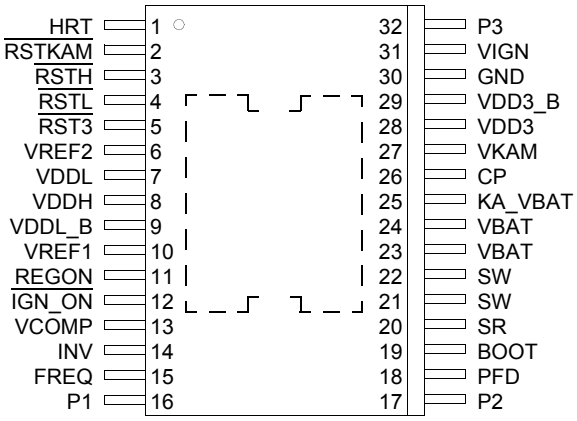


Figure 2. 33730 Simplified Internal Block Diagram

PIN CONNECTIONS



Note: The exposed pad is electrically and thermally connected to the IC ground.

Figure 3. 33730 Pin Connections

Table 1. 33730 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 11.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	HRT	Analog Output	Hardware Reset Timer	This pin is the hardware reset timer programmed with an external resistor.
2	$\overline{\text{RSTKAM}}$	Open Drain	VKAM Reset	This pin is an open drain reset output, monitoring the V_{KAM} supply to the microprocessor.
3	$\overline{\text{RSTH}}$	Open Drain	VDDH Reset	This pin is an open drain reset output, monitoring the V_{DDH} regulator.
4	$\overline{\text{RSTL}}$	Open Drain	VDDL Reset	This pin is an open drain reset output, monitoring the V_{DDL} regulator.
5	$\overline{\text{RST3}}$	Open Drain	VDD3 Reset	This pin is an open drain reset output, monitoring the V_{DD3} regulator.
6	VREF2	Power Output	VREF Output 2	This pin is the output of the protected supply VREF2. The pin is supplied from the V_{DDH} through the protection FET.
7	VDDL	Analog Input	VDDL Regulator	This pin is the V_{DDL} regulator output feedback pin.
8	VDDH	Analog/ Power Input	VDDH Regulator	This pin is the 5.0 V output feedback pin of the buck regulator. The pin is also a power input for the protected outputs VREF1,2.
9	VDDL_B	Analog Output	VDDL Regulator Base Drive	VDDL linear regulator base drive.
10	VREF1	Power Output	VREF Output 1	This pin is the output of the protected supply VREF1. The pin is supplied from the V_{DDH} through the protection FET.
11	REGON	Logic Input	Regulator Hold On	Regulator Hold On input pin (5.0 V logic level input).
12	$\overline{\text{IGN_ON}}$	Open Drain	VIGN Status	This open drain output signals the status of the VIGN pin.
13	VCOMP	Analog Output	Compensation	This pin provides switching pre-regulator compensation, it is the output of the error amplifier.
14	INV	Analog Input	Inverting Input	Inverting input of the switching regulator error amplifier.
15	FREQ	Analog Input	Frequency Adjustment	Frequency adjustment of the switching regulator. The value of the resistor to ground at this pin determines the oscillator frequency.
16	P1	Logic Input	Programming Pin 1	Programming pin 1 for the V_{DD3}, V_{DDL}, and V_{KAM} reference voltages.

Table 1. 33730 Pin Definitions(continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 11.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
17	P2	Logic Input	Programming Pin 2	Programming pin 2 for the V_{DD3}, V_{DDL}, V_{KAM} reference voltages.
18	PFD	Analog Output	Protection FET Drive	Reverse battery protection FET gate drive.
19	BOOT	Analog Input	Bootstrap	This pin is connected to the bootstrap capacitor.
20	SR	Analog Input	Slew-rate	Slew-rate Control of the switching regulator.
21,22	SW	Power Output	Switch Node	These pins are the source of the internal power switch (N-channel MOSFET).
23,24	VBAT	Power Input	Battery Voltage Supply	Voltage supply to the IC (external reverse battery protection needed in some applications).
25	KA_VBAT	Power Input	Keep Alive Supply	This pin is the keep alive supply input.
26	CP	Analog Output	Charge Pump	External capacitor reservoir of the internal charge pump.
27	VKAM	Power Output	Keep Alive Memory	Keep-Alive Memory (standby) supply output.
28	VDD3	Analog Input	V_{DD3} Linear Regulator	This is a VDD3 regulator output feedback pin. This pin is also the output of the V_{DD3} standby regulator.
29	VDD3_B	Analog Output	VDD3 Linear Regulator Base Drive	This pin can be used also as an additional standby regulator without the external pass transistor.
30	GND	Ground	Ground	This pin is a ground.
31	VIGN	Analog Input	Voltage Ignition	This pin is the ignition switch control input pin. It contains an internal protection diode.
32	P3	Logic Input	Programming Pin 3	Programming pin 3 for the V_{DD3}, V_{DDL}, and V_{KAM} reference voltages.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
Supply Voltage (VBAT)	V_{BAT}	-0.3 to +40	V
Keep-Alive Supply Voltage (KA_VBAT)	KA_V_{BAT}	-18 to +40	V
Control Inputs (VIGN, P1, P2, P3), PFD Output		-18 to +40	V
Bootstrap Voltage (BOOT, SR) referenced to ground	V_{BOOT}	-0.3 to +50	V
Bootstrap Voltage (BOOT, SR) referenced to SW	V_{BOOT} - V_{SW}	-0.3 to +12	V
Charge Pump Output Voltage (CP)	V_{CP}	-0.3 to +12	V
Switch Node Voltage SW	V_{SW}	-2.0 to +40	V
Sensor Supplies (VREF1, VREF2)	V_{REF}	-1.0 to +26.5	V
Sensor Supplies (VREF1, VREF2) Maximum Slew Rate	$V_{REFMAXSR}$	2.0	V/µs
Regulator Voltages (V_{DDH},V_{DD3}, V_{DD3_B}, V_{DDL},V_{DDL_B}, V_{KAM})	V_{REG}	-0.3 to +7.0	V
Open Drain Outputs ($\overline{RSTH}$, $\overline{RSTL}$, $\overline{RST3}$, $\overline{RSTKAM}$, $\overline{IGN_ON}$)	V_{DD}	-0.3 to +7.0	V
Regon Input	V_{REGON}	-0.3 to +7.0	V
Analog Inputs (VCOMP, INV, FREQ, HRT)	V_{IN}	-0.3 to +3.0	V
ESD Voltage[1] Human Body Model - HBM (all pins except BOOT, VDDL, RSTL) Human Body Model - HBM (Pins BOOT, VDDL, RSTL) Machine Model - MM (all pins) Charge Device Model - CDM (all pins)	V_{ESD}	 ±2000 ±1500 ±200 ±750	V
Operational Package Temperature (Ambient Temperature)	T_{A_MAX}	-40 to +125	°C
Storage Temperature	T_{STO}	-65 to +150	°C
Peak Package Reflow Temperature During Reflow[2], [3]	T_{PPRT}	Note 3	°C
Maximum Junction Temperature	T_{J_MAX}	150	°C
Thermal Resistance, Junction to Ambient[4]	$R_{\theta J\text{-}A}$	41	°C/W
Thermal Resistance, Junction to Case[5]	$R_{\theta J\text{-}C}$	1.2	°C/W

Notes

1. ESD testing is performed in accordance with the Human Body Model (HBM) (AEC-Q100-2), the Machine Model (MM) (AEC-Q100-003), R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (AEC-Q100-011).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
4. Thermal resistance measured in accordance with EIA/JESD51-2.
5. Theoretical thermal resistance from the die junction to the exposed pad.

RECOMMENDED OPERATING CONDITIONS

Table 3. Recommended Operating Conditions

All voltages are with respect to ground unless otherwise noted.

Parameter	Value	Unit
Supply Voltages (V_{BAT}, KA_V_{BAT})	*6.0 to 26.5	V
Switching Regulator Output Current (I_{VDDH}) total, VBAT = 6.0 to 26.5 V	0 to 2.0	A
V_{DD3} Standby Output Current	0 to 15	mA
V_{KAM} Standby Output Current	0 to 15	mA
$V_{REF1,2}$ Output Current	0 to 100	mA
Switching Frequency Range	100 to 500	kHz

* Tracks battery voltage from 6.0 down to 4.5 V.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristic

Characteristics noted under conditions 6.0 V ≤ KA_V_{BAT} = V_{BAT} ≤ 26.5 V, -40°C ≤ T_A ≤ 125°C using the typical application circuit, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Keep-Alive Start-up Voltage (at the KA_VBAT pin), VKAM Output Up	V_{KAM_STUP}	4.5	—	—	V
Start-up Voltage (at the KA_VBAT pin), VDD3, VDD3 standby, VDDL Up	V_{STUP}	4.5	—	—	V
Over-voltage Shutdown Voltage at KA_VBAT pin rising	V_{SHDN_R}	35	—	42	V
Under-voltage Lock-out Voltage at KA_VBAT pin falling Voltage at KA_VBAT pin rising Under-voltage Lock-out Hysteresis[6]	V_{UVLO_F} V_{UVLO_R} V_{UVLO_HYS}	3.6 3.7 —	— — 0.1	4.3 4.4 —	V
Sleep Quiescent Current (Sleep mode) V_{IGN} = 0 V, REGON = 0 V, I_{VKAM} = 0 mA, V_{DD3} OFF, V_{BAT} = 14.0 V, KA_V_{BAT} = 14 V (P1=1, P2=1, P3=1)	I_Q	—	—	500	µA
SWITCHING REGULATOR (VDDH)					
Buck Converter Output Voltage V_{BAT} = 6.0 to 26.5 V, I_{LOAD} = 100 mA V_{BAT} = 26.5 to 35 V, I_{LOAD} = 100 mA	V_{DDH}	 4.9 4.85	 5.0 5.0	 5.1 5.15	V
Switching Regulator Current Limit (see Figure 5) Pulse-by-Pulse Current Limit Extreme Current Limit (see Figure 5)[6]	 I_{LIM_SW} $I_{LIM_SW_EX}$	 -2.25 -3.75	 -3.5 -4.5	 -4.25 -6.00	A
SW Drain Source On Resistance[6] I_D = 500 mA, V_{BAT} = 5.0 V	$R_{DS(ON)}$	—	—	200	mΩ
Thermal Shutdown Junction Temperature[6]	TS_H TS_L	— 155	— —	195 —	°C
Thermal Shutdown Hysteresis[6]	TS_{HYS}	1.0	—	20	°C
VDD3 LINEAR REGULATOR					
V_{DD3} Output Voltage (Includes Line and Load Regulation) I_{VDD3} = 0 to -500 mA, See Table 1 for V_{DD3} Output Settings	V_{DD3}	-3.0	—	3.0	%
V_{DD3} Dropout Voltage (V_{DDH} - V_{DD3}) I_{VDD3} = -800 mA (VDD3 set to 3.3 V via P1, P2, P3 and with an external transistor)	V_{DD3_DO}	—	1.1	1.5	V
V_{DD3_B} Current Limit, V_{DD3_B} = 0 V, KA_V_{BAT} = 14 V, V_{BAT} = 14 V KA_V_{BAT} = 5.0 V, V_{BAT} = 5.0 V	I_{VDD3B_Lim}	 -20 -20	 — —	 -50 -50	mA

Notes
6. Guaranteed By Design.

Table 4. Static Electrical Characteristic(continued)

Characteristics noted under conditions 6.0 V ≤ KA_V_{BAT} = V_{BAT} ≤ 26.5 V, -40°C ≤ T_A ≤ 125°C using the typical application circuit, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VDD3 STANDBY LINEAR REGULATOR					
V_{DD3} Standby Output Voltage (Includes Line and Load Regulation) I_{VDD3_SBY} = 0 to -15 mA, See Table 1 for VDD3_SBY Output Setting	V_{DD3_SBY}	-15	—	15	%
V_{DD3} Dropout Voltage (KA_V_{BAT} - V_{DD3}) Standby Mode (VDD3 set at 3.3 V via P1, P2, P3) I_{VDD3} = -10 mA	V_{DD3_DO}	—	—	1.4	V
V_{DD3} Standby Current Limit, V_{DD3} = 0 V KA_V_{BAT} = 14 V, V_{BAT} = 14 V KA_V_{BAT} = 5.0 V, V_{BAT} = 5.0 V	$I_{VDD3SBY_LIM}$	 -20 -20	 — —	 -50 -50	mA
Thermal Shutdown Junction Temperature(7)	TS_H TS_L	— 150	— —	190 —	°C
Thermal Shutdown Hysteresis(7)	TS_{HYS}	5.0	—	20	°C
VDDL LINEAR REGULATOR					
V_{DDL} Output Voltage (Includes Line and Load Regulation) I_{VDDL} = 0 to -500 mA, See Table 1 for V_{DDL} Output Setting	V_{DDL}	-3.0	—	3.0	%
V_{DDL_B} Dropout Voltage (V_{DDH} - V_{DDL}) (VDDL set at 3.3 V via P1, P2, P3) I_{VDDL} = -800 mA	V_{DDL_DO}	—	—	280	mV
V_{DDL_B} Current Limit, V_{DDL} = 0 V KA_V_{BAT} = 14 V, V_{BAT} = 14 V KA_V_{BAT} = 5.0 V, V_{BAT} = 5.0 V	I_{VDDL_LIM}	 -18 -18	 — —	 -50 -50	mA
VKAM STANDBY LINEAR REGULATOR					
V_{KAM} Output Voltage (Includes Line and Load Regulation) I_{VKAM} = 0 to -15 mA, See Table 1 for V_{KAM} Output Setting	V_{KAM}	-15	—	15	%
V_{KAM} Dropout Voltage (KA_V_{BAT} - V_{KAM}) I_{VKAM} = -10 mA, V_{KAM} set to 5.0 V (P1 = L, P2 = H, P3 = L)	V_{KAM_DO}	—	—	1.4	V
VKAM STANDBY LINEAR REGULATOR (CONTINUED)					
V_{KAM} Current Limit, V_{KAM} = 0 V KA_V_{BAT} = 14 V, V_{BAT} = 14 V KA_V_{BAT} = 5.0 V, V_{BAT} = 5.0 V	I_{VKAM_LIM}	 -20 -20	 — —	 -50 -50	mA
Thermal Shutdown Junction Temperature(7)	TS_H TS_L	— 150	— —	190 —	°C
Thermal Shutdown Hysteresis(7)	TS_{HYS}	5.0	—	20	°C

Notes
7. Guaranteed By Design.

Table 4. Static Electrical Characteristic(continued)

Characteristics noted under conditions 6.0 V ≤ KA_V_{BAT} = V_{BAT} ≤ 26.5 V, -40°C ≤ T_A ≤ 125°C using the typical application circuit, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SENSOR SUPPLIES VREF1, VREF2					
V_{REF} On-resistance, I_{VREF} = -100 mA	$R_{DS(ON)}$	—	—	500	mΩ
V_{REF} Current Limit, V_{REF} = -1.0 V[8]	I_{REF_LIM}	-150	-280	-450	mA
V_{REF} Reverse Current Limit, V_{REF} = 26.5 V[8]	I_{REF_REVLIM}	—	—	40	mA
V_{REF} Leakage Current, V_{REF} Shut Down, V_{REF} = -1.0 V[8]	I_{REF_REVLIM}	-2.0	—	—	mA
Thermal Shutdown Junction Temperature[9]	TS_H TS_L	— 150	— —	190 —	°C
Thermal Shutdown Hysteresis[9]	TS_{HYS}	5.0	—	20	°C
SUPERVISORY AND CONTROL CIRCUITS					
V_{IGN} Input Voltage Threshold V_{BAT} = 14.0 V, KA_V_{BAT} = 14 V	V_{IGN_IH} V_{IGN_IL}	4.0 2.0	4.3 2.15	4.6 2.4	V
V_{IGN} Hysteresis	$V_{IGN-HYS}$	1.7	—	—	V
V_{IGN} Pull-down Current @ 5.0 V V_{BAT} = 14.0 V, KA_V_{BAT} = 14 V	I_{PD}	10	30	60	µA
REGON Input Voltage Threshold V_{BAT} = 14.0V, Battery Voltage = 14V	V_{IH} V_{IL}	1.7 -0.3	— —	— 1.0	V
REGON Input Voltage Threshold Hysteresis	V_{IHYS}	0.1	0.3	0.4	V
REGON Pull-down Current @ 3.0 V	I_{PD}	5.0	—	30	µA
Programming Pin Input Voltage Threshold V_{BAT} = KA_V_{BAT} = 14 V	V_{IH} V_{IL}	2.5 -0.3	— —	V_{BAT} 1.0	V
Programming P1, P2, P3 Leakage Current @ 14.0 V	I_{PD}	—	1.0	5.0	µA
V_{DDH} Reset Upper Threshold Voltage ($\Delta V_{DDH}/V_{DDH}$)		4.0	8.0	13.0	%
V_{DDH} Reset Lower Threshold Voltage ($\Delta V_{DDH}/V_{DDH}$)		-3.0	-8.0	-13.0	%
V_{DDL} Reset Lower Threshold Voltage ($\Delta V_{DDL}/V_{DDL}$)		-3.0	-8.0	-13.0	%
V_{DD3} Reset Lower Threshold Voltage ($\Delta V_{DD3}/V_{DD3}$)		-3.0	-8.0	-13.0	%
V_{DD3_SBY} Reset Lower Threshold Voltage ($\Delta V_{DD3_SBY}/V_{DD3_SBY}$)		-3.0	-12.5	-30	%
V_{KAM} Reset Lower Threshold Voltage ($\Delta V_{KAM}/V_{KAM}$)		-3.0	-12.5	-30	%
$\overline{RSTH}$, $\overline{RSTL}$, $\overline{RST3}$, $\overline{RSTKAM}$ Low-level Output Voltage I_{OL} = 5.0 mA		—	—	0.4	V
$\overline{IGN_ON}$ Low-level Output Voltage I_{OL} = 5.0 mA		—	—	0.4	V

Notes

8. The short circuit transient events on the VREF outputs must be limited to the voltage levels specified in the Maximum Ratings and slew rates of less than 2.0 V/µs, otherwise damage to the part may occur. Refer to the paragraph Sensor Supplies (VREF1, VREF2) on page 17 and typical application circuit diagrams on Figure 8,and Figure 9 for recommended VREF output termination.
9. Guaranteed by design.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 6.0 V ≤ KA_V_{BAT} = V_{BAT} ≤ 26.5 V, -40°C ≤ T_A ≤ 125°C using the typical application circuit, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Power On Reset Delay Time (HR Timer) (see Table 7) (Time to $\overline{\text{RESET}}$ up after Regulator in regulation)	t_{D_POR}	 0	 —	 68	ms
Power On Reset Delay Time (HR Timer) Accuracy (33 k resistor)		8.0	—	12	ms
Programming Pin Latching Delay[10]	t_{LD_P}	—	500	—	µs
SWITCHING REGULATOR					
Oscillator Frequency (Switching Freq.) Range - Adjustable (Figure 4)	Freq	100	—	500	kHz
Oscillator Frequency Tolerance at 100 kHz (FREQ Pin Open)	f_{TOL}	90	—	110	kHz
SW Node Rise Time, V_{BAT} = KA_V_{BAT} = 14 V, I_{SW} = 500 mA[10] SR pin shorted to SW pin SR pin open SR pin shorted to BOOT pin	t_{SW_R}	 — — —	 0.96 1.82 2.38	 — — —	V/ns
SW Node Fall Time, V_{BAT} = KA_V_{BAT} = 14 V, I_{SW} = 500 mA[10] SR pin shorted to SW pin SR pin open SR pin shorted to BOOT pin	t_{SW_F}	 — — —	 0.83 0.83 0.83	 — — —	V/ns

Notes

10. Guaranteed by design.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33730 multi-output power supply integrated circuit addresses the system power supply needs for applications using the Freescale 32-bit microcontroller family architecture.

FUNCTIONAL PIN DESCRIPTION

HARDWARE RESET TIMER (HRT)

This pin is the hardware reset timer input, which provides delays for the Reset outputs. This delay is programmed by an external resistor to GND.

VKAM RESET ($\overline{\text{RSTKAM}}$)

This pin is an open drain reset output monitoring the V_{KAM} supply to the microprocessor. This output is actively pulled low when the VKAM output voltage falls below its reset threshold level.

VDDH RESET ($\overline{\text{RSTH}}$)

This pin is an open drain reset output monitoring the VDDH regulator. This output is actively pulled low when the VDDH output voltage falls below its reset lower threshold level or when the VDDH output voltage exceeds its reset upper threshold level

VDDL RESET ($\overline{\text{RSTL}}$)

This pin is an open drain reset output monitoring the VDDL regulator. This output is actively pulled low when the VDDL output voltage falls below its reset threshold level.

VDD3 RESET ($\overline{\text{RST3}}$)

This pin is an open drain reset output monitoring the VDD3 regulator. This output is actively pulled low when the VDD3 output voltage falls below its reset threshold level.

VREF OUTPUT 2 (VREF2)

This pin is output of the protected supply VREF2. This output supplies sensors outside of the electronic control module and therefore it is protected against a battery short and short to -1.0 V. This pin is supplied from the V_{DDH} through the internal protection FET.

VDDL REGULATOR (VDDL)

This pin is the V_{DDL} regulator output feedback pin. The emitter of VDDL regulator external NPN pass transistor is connected to this pin.

VDDH REGULATOR (VDDH)

This pin is the 5.0 V output feedback pin of the buck regulator. This pin is also a power input for the protected outputs VREF1 and VREF2.

VDDL REGULATOR BASE DRIVE (VDDL_B)

VDDL linear regulator base drive. This output supplies current into the base of the regulator external pass NPN transistor.

VREF OUTPUT 1 (VREF1)

This pin is output of the protected supply VREF1. This output supplies sensors outside of the electronic control module and therefore it is protected against short battery and short to -1.0 V. This pin is supplied from the V_{DDH} through the internal protection FET.

REGULATOR HOLD ON (REGON)

Regulator Hold On input control pin. The 33730 can be enabled or kept in the Normal operational mode by holding this pin high. This is a 5.0 V logic input.

VIGN STATUS ($\overline{\text{IGN_ON}}$)

This open drain output signals the status of the VIGN pin. This logic output is actively pulled low when the VIGN control input is pulled high.

COMPENSATION (VCOMP)

This pin provides switching pre-regulator compensation network. It is the output of the switching regulator error amplifier.

INVERTING INPUT (INV)

This pin is the inverting input of the switching regulator error amplifier.

FREQUENCY ADJUSTMENT (FREQ)

This is the frequency adjustment input of the switching regulator. The operating frequency of the switching regulator can be programmed by an external resistor from this pin to ground.

PROGRAMMING PIN 1 (P1)

Programming Pin 1 for the VDD3, VDDL, and VKAM reference voltage. The output voltage of the VDD3, VDDL and VKAM regulators can be programmed by the P1, P2, and P3 pins (see Table 6).

PROGRAMMING PIN 2 (P2)

Programming Pin 2 for the VDD3, VDDL, and VKAM reference voltage. The output voltage of the VDD3, VDDL and VKAM regulators can be programmed by the P1, P2, and P3 pins (see Table 6).

PROGRAMMING PIN 3 (P3)

Programming Pin 3 for the VDD3, VDDL, and VKAM reference voltages. The output voltage of the VDD3, VDDL and VKAM regulators can be programmed by the P1, P2, and P3 pins (see Table 6).

PROTECTION FET DRIVE (PFD)

Reverse battery protection FET gate drive. This pin is an output drive for the gate of the external Reverse Battery Protection N-channel FET.

BOOTSTRAP (BOOT)

This pin is connected to the bootstrap capacitor. It provides the supply power for the switching regulator high-side drive.

SLEW-RATE (SR)

Slew-rate Control of the switching regulator. The slew-rate of the switching regulator can be adjusted by connecting this pin to switch node (SW pin, slow slew-rate selection), BOOT pin (fast slew-rate selection), or it can be left open (medium slew-rate selection).

SWITCH NODE (SW)

This pin is the source of the switching regulator internal power switch (N-channel MOSFET source).

BATTERY VOLTAGE SUPPLY (VBAT)

Voltage supply to the IC (external reverse battery protection is recommended).

KEEP ALIVE SUPPLY (KA_VBAT)

This pin is the keep alive supply input. This input is reverse battery protected. This input supplies power to the internal supply and bias circuits that have to do with this VKAM and other always-on supplies.

CHARGE PUMP (CP)

External reservoir capacitor of the internal charge pump. This charge pump provides the voltage needed to sufficiently enhance the gates of the internal n-channel mosfets (VREF1, VREF2, and VDDH) during the low battery condition.

KEEP ALIVE MEMORY (VKAM)

Keep Alive Memory (standby) supply output. This output supplies power for the module Keep-Alive memory. This output is always on, if the voltage at the KA_VBAT pin is above 4.5 V.

VDD3 LINEAR REGULATOR (VDD3)

This is a VDD3 regulator output feedback pin.The emitter of VDD3 regulator external NPN pass transitory is connected to this pin.

This pin can programmed to be the output of the VDD3 Standby regulator (see Table 6).

VDD3 LINEAR REGULATOR BASE DRIVE (VDD3_B)

This pin can be used also as an additional standby regulator without the external pass transistor.This output supplies current into the base of the regulator external pass NPN transistor.

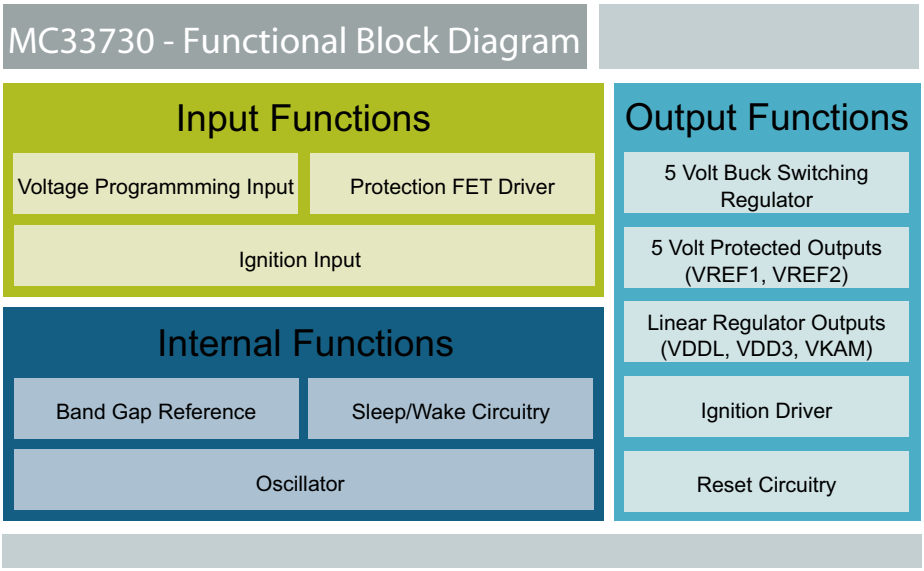
GROUND (GND)

This pin is the ground pin of the integrated circuit.

VOLTAGE IGNITION (VIGN)

This pin is the turn-on control input that is controlled through an ignition switch. This pin is reverse battery protected.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



5.0 VOLT BUCK REGULATOR

This is the main regulator that supplies 5.0 Volts to the following protected and regulated outputs, VREF1, VREF2, VDD3, and VDDL.

OSCILLATOR

This is the frequency source for the switching (buck) 5 Volt regulator. The frequency of oscillation is selected by an external resistor to ground.

BAND GAP REFERENCE

This is the main voltage reference, which is used as the standard for all the current and voltage sources in the MC33730.

PROTECTION FET DRIVER

The protection FET is used to prevent reverse battery connections from damaging the MC33730. The gate drive for the Protection FET is provided by this driver circuit.

SLEEP/WAKE CIRCUITRY

This circuitry is responsible for the two main modes of operation for the MC33730, Sleep mode and Wake mode. In the Sleep mode, only the keep alive outputs are active, and the rest of the circuitry is in a low power drawing sleep state. In the Wake mode, the MC33730 is fully functional and normal current is being consumed.

IGNITION DRIVER

This block of circuitry controls all the voltage outputs, except for the keep alive voltage output(s). It also provides an output signal to indicate that the ignition switch has been activated.

VREF1

This output is one of two protected 5.0 volt outputs that can be used to supply external sensors or other analog circuits requiring a regulated, short-circuit protected 5.0 volt supply.

VREF2

This output is one of two protected 5.0 volt outputs that can be used to supply external sensors or other analog circuits requiring a regulated, short-circuit protected 5.0 volt supply.

VDD3 REGULATOR

This is one of three, voltage programmable, regulated supplies. This supply is controlled by the ignition switch.

VDDL REGULATOR

This is one of three, voltage programmable, regulated supplies. This supply is controlled by the ignition switch.

VKAM

This is one of three, voltage programmable, regulated supplies. This supply is NOT controlled by the ignition switch.

VOLTAGE PROGRAMMING

P1, P2, and P3 are three logic level inputs that control the voltage that is available on the VDD3, VDDL and VKAM outputs.

Table 6 indicates the 8 different combinations of P1, P2, and P3 and the resultant voltage values.

RESET CIRCUITRY

There are four open drain reset lines that indicate the status of the four voltage outputs; VDDH, VDDL, VDD3, and VKAM. They are labeled: RSTH, RSTL, RST3, and RSTKAM.

REGON INPUT

This input is OR'd with VIGN. However, it is a 5.0 volt logic input, as opposed to VIGN, which is a V_{BAT} level input. This input is controlled by an MCU I/O pin, to hold power up when the ignition switch is turned off, so housekeeping functions can be performed before power is shut off, by lowering the REGON line. IF REGON is not needed, it should be tied to GND.

FUNCTIONAL DEVICE OPERATION

OPERATION DESCRIPTION

INTRODUCTION

The 33730 has two supply inputs. The KA_VBAT pin is the supply input for the standby regulators V_{KAM} (and optionally V_{DD3_SBY}, see Table 6) and for the internal supply circuits. The VBAT pin is the power input of the integrated buck regulator, which steps-down the protected battery voltage providing directly the 5.0 V system supply V_{DDH}. V_{DDH} provides power for the main linear regulator(s) V_{DDL}, V_{DD3}, and also for the other module circuits requiring 5.0 V supply voltage (e.g. protected $V_{REF1,2}$ outputs).

If the supply voltage ramps from zero volts up to its nominal level, the 33730 will start at the latest when the supply (battery) voltage reaches V_{STUP} at the KA_VBAT pin. If the supply voltage ramps down, the 33730 will keep operating (with degradation of the output voltage regulation) down to V_{UVLO_f} at the KA_VBAT pin. The V_{KAM} output stays operational down to V_{UVLO_f} at the KA_VBAT pin.

The 33730 will operate in systems with and without standby mode. In the Standby (sleep) mode of operation the IC will draw maximum I_Q quiescent current, assuming only the VKAM is used as a standby output, and it is unloaded. When VDD3 is used as an additional standby output the quiescent current increases by approximately another 100 μA.

POWER UP

The 33730 will safely power up when the power is applied simultaneously (hot plugged) or in the random sequence to the KA_VBAT, VBAT and VIGN (or REGON) inputs.

POWER DOWN

The 33730 will safely power down when the power is disconnected from any of the KA_VBAT, VBAT inputs or when control signals the VIGN or REGON inputs go low.

UNDERVOLTAGE LOCK-OUT (UVLO)

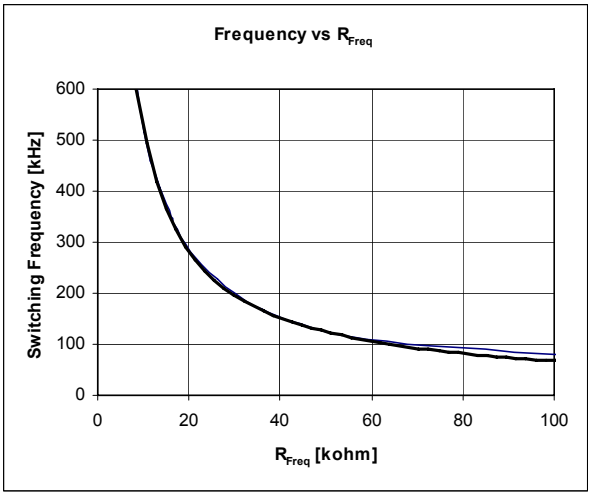
There is an under-voltage lock-out feature implemented into the IC. When the battery voltage at the KA_VBAT pin falls below V_{UVLO_f} the under-voltage comparator initiates the power down sequence for the whole IC. The under-voltage lock-out circuit has a V_{UVLO_hys} hysteresis and 5.0 μs glitch filter in order to prevent spurious tripping its threshold level and consequent system oscillations between the ON and OFF states.

SWITCHING REGULATOR

The 33730 switching regulator is a fixed frequency (externally adjustable) PWM voltage mode controller with integrated low-$R_{DS(ON)}$ N-channel power MOSFET. This architecture is widely flexible and provides a possibility to optimize its operation over a wide range of input voltages. The 33730 switching regulator provide the following features:

Adjustable Switching Frequency

The adjustable frequency feature provides the ability to modify the switcher performance for optimized cost (higher frequency, smaller, cheaper components), or higher efficiency and better EMC performance (lower switching frequency for reduced losses and EMI). The operating frequency of the switching regulator can be adjusted by means of an external resistor R_F connected from the FREQ pin to ground (see Figure 4).



$F_{SW} \cong 18.48 + (5098.7/R_{FREQ})$
F_{SW} is the switch frequency in kHz
R_{FREQ} is the resistor value in kOhms

Figure 4. Switching Regulator Frequency vs. R_{Freq} Value

Adjustable Slew-rate

The adjustable slew-rate option allows, with selection of the right switching frequency, optimization of the system for EMC performance.

Over-voltage Lock-Out (Shutdown)

The over-voltage lock-out (shutdown) feature turns the switching regulator off when the input voltage exceeds the V_{SHDN_r} limit. This extends the 33730 capability to survive the severe load dump conditions up to max V_{BAT}.

Operation at 100% Duty Cycle

The internal charge pump is used to enhance the power MOSFET gate when the switching regulator reaches 100% duty cycle during the low battery conditions.

The switching regulator output voltage V_{DDH} is regulated to provide 5.0 V @ 2.0 A with ±2% accuracy and it is intended to directly power the digital and analog circuits of the Electronic Control Module (ECM). The switching regulator

output current is also used by the following linear regulators V_{DD3_3}, V_{DDL}, and sensor supplies V_{REF1}, and V_{REF2}.

The direct voltage conversion to V_{DDH} = 5.0 V together with the Protection FET Driver circuit allows operation of the IC at very low battery voltages, which would otherwise require to use a boost regulator (with an additional system cost) or a different and more expensive switching converter topology (e.g. flyback).

Short Circuit Protection

The switching regulator is protected against the over-current and short-circuit conditions. It integrates a current limit circuit, which has two threshold levels - the pulse by pulse, and the extreme.

Pulse by Pulse Current Limit

Pulse-by-Pulse Current Limit threshold has a nominal value set I_{LIM_SW}. When the current flowing through switching regulator power FET exceeds this value the power FET is immediately turned off. During the next switching cycle the power FET is turned on again until it is commanded off by its natural duty cycle or until the current reaches the threshold level again. It should be noted that the current limit is blanked for several tens of nanoseconds during the turn-on and turn-off transition times in order to prevent erroneous turn off due to the current spikes caused by switcher parasitic components.

Extreme Current Limit.

In some cases, during the over-current or short-circuit condition, the inductor current does not sufficiently decay during the off time of the switching period. The current rise during the current limit blanking time is higher than the decay during the off time. In this case the current in the inductor builds up every consecutive switching cycle. In order to prevent the power FET failure during this condition an extreme current limit has been implemented. When the current flowing through the power FET reaches the $I_{LIM_SW_Ext}$ threshold, the switching regulator will shut off for 500 µs, before the switching regulator is allowed to turn on again (see Figure 5).

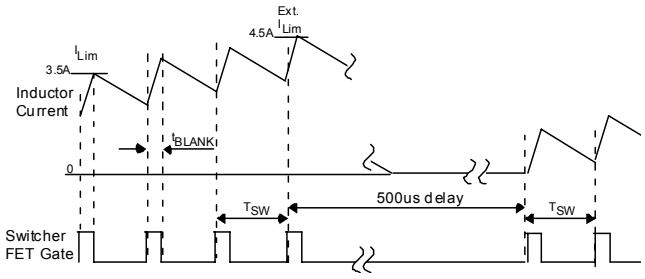


Figure 5. 33730 Current Limit

Soft Start

The switching regulator has an integrated soft-start feature. During the soft-start sequence the duty cycle of the internal power switch will be gradually increased from low value to the regulation level. This technique prevents any undesirable inrush current into the buck regulator output capacitor.

LINEAR REGULATORS

The 33730 integrates two linear regulator control circuits V_{DD3} (programmable), V_{DDL} (programmable) both capable of driving up to 15 mA (min.) base current into the external pass NPN transistors. The output voltage of both linear regulators is monitored at their feedback pins (V_{DD3} and V_{DDL}). If the voltage at any of the V_{DD3}, V_{DDL} feedback pins fall below their regulation level, the supervisory Reset control circuits will assert the corresponding reset signal ($\overline{RSTL}$, and/or $\overline{RST3}$ lines will be pulled low). See Table 6 for the output voltage selection details.

The linear regulators will stay in regulation down to 4.5 V at the KA_VBAT pin.

The 33730 linear regulators offer high flexibility and variability of the module design in terms of selectable output voltages as well as wide range of output current capability. There several types of suitable external pass NPN transistors which could be used. The choice of the particular type depends mostly on the expected power dissipation of the pass transistor. The following parts provide good solution and have been bench tested with the 33730:

BCP68T1 (SOT-223)

NJD2873T4 (DPAK)

MJB44H11 (D^2PAK)

Available from ON Semiconductor.

NOTE: The 33730 linear regulators have been designed to use low ESR ceramic output capacitors - see Figure 8 and Figure 9 for the recommended values.

STANDBY REGULATORS

The 33730 integrates two standby linear regulators, the V_{KAM} and the optional standby regulator V_{DD3} (see Figure 9) for the optional standby circuit).The output voltage levels of both standby linear regulators are programmable and supervised by the Reset control circuits ($\overline{RSTKAM}$, and/or $\overline{RST3}$). Both the V_{KAM} and V_{DD3} outputs are capable of delivering I_{VKAM_LIM} and I_{VDD3_LIM} of load current. See Table 6 for the V_{KAM} and V_{DD3} standby output voltage selection details.

The V_{KAM} standby regulator will keep functioning even below V_{UVLO_f} but the specified drop out voltage may not be maintained.

NOTE: The 33730 standby regulators have been designed to use low ESR ceramic output capacitors - see Figure 8 and Figure 9 for recommended values.

PROGRAMMING LINEAR REGULATOR OUTPUT VOLTAGE

The output voltage of the VDD3, VDDL and VKAM outputs can be externally programmed by placing logic levels on the programming pins P1, P2, and P3 (see Table 6). This extends the application flexibility of the IC without having to use an external resistor divider, thus improving the regulator accuracy over the whole temperature range, and reducing the component count.

The status of the programming pin can be selected either by tying the pin to ground (logic level “0”). The logic level “1” can be selected either by tying the programming pin up (the programming pin can be tied up to the battery voltage) or by leaving the pin open.

The programming information is read and latched with the 500 μs delay after the power is applied to the IC.

Table 6. Programming VDD3, VDDL, VKAM Output Voltage

P1	P2	P3	V_{DD3}	V_{DDL}	V_{KAM}
High	High	High	3.3 V	2.6 V	2.6 V
High	High	Low	3.3 V	3.3 V	3.3 V
High	Low	High	3.3 V	1.5 V	1.0 V
High	Low	Low	3.3 V	3.3 V	1.0 V
Low	High	High	3.3 V Standby	3.3 V	1.0 V
Low	High	Low	2.0 V	3.15 V	5.0 V
Low	Low	High	2.6 V Standby	3.3 V	1.0 V
Low	Low	Low	2.6 V Standby	3.3 V	1.5 V

The Programming Pins can be tied high to battery voltage

LOW BATTERY OPERATION

When the battery voltage falls below the specified minimum value, the 33730 switching regulator will enter a 100% duty cycle mode of operation and its output voltage V_{DDH} will follow the decreasing battery voltage. If the battery voltage continues to fall, the V_{DDH} voltage reaches its reset threshold level, and the $\overline{RSTH}$ signal will be pulled low, but the other linear regulators will continue to operate, and their monitoring signals stay high as long as the VDDH provides sufficient headroom for the regulators to stay in their regulation limits (see Figure 6 and Figure 7). If the battery voltage continues to fall, the linear regulators would not have sufficient headroom to stay in regulation, and their resets would be asserted ($\overline{RSTL}$, $\overline{RST3}$, or both would be pulled low). At that moment the power down sequence would be engaged.

The V_{KAM} standby regulator will operate down to ($V_{KAM\ and}$ V_{KAM_DO}) and V_{KAM-DO} at the KA_VBAT pin.

POWER SEQUENCING (VDDH, VDD3, VDDL)

V_{DDH}, V_{DD3}, and V_{DDL} are power sequenced by means of internal pull-down FETs. During the power up sequence, V_{DD3} and V_{DDL} will follow V_{DDH}.

During the power down sequence the VDD3 and VDDL outputs will be pulled down by the internal pull-down power FETs, and V_{DDH} will be shut off with a defined delay (~100 μs typ.).

In order to engage the power down sequence, the following conditions have to be met:

($\overline{VIGN}$. $\overline{REGON}$) + $\overline{UVLO}$ = Power Down

The VDD3 output is not power sequenced when used as a standby regulator.

SENSOR SUPPLIES (VREF1, VREF2)

There are two sensor supplies, VREF1 and VREF2, integrated into the IC. They are internally connected to V_{DDH} through power MOSFETs which protect against short to battery and short to ground conditions.

Severe fault conditions on the VREF1 and VREF2 outputs, like shorts to either ground or battery, will not disrupt the operation of the main regulator V_{DDH}, or cause assertion of any Reset signal.

IMPORTANT NOTE:

The VREF outputs MUST be externally protected against transient voltage events with slew rates faster than 2.0 V/μs, otherwise damage to the part may occur. A practical and inexpensive solution consists of using a series RC network connected from the VREF output to ground (see Figures 8 and 9 for typical component values). Other means, such as a single electrolytic capacitor with its capacitance value C > 10 μF, may be also used.

PROTECTION FET DRIVE (PFD)

The Protection FET Drive circuit allows using an optional N-channel protection MOSFET (instead of a standard reverse protection diode) to protect against a reverse battery voltage condition. This approach improves the operating capabilities at very low battery voltages.

An internal **charge pump** is used to enhance the Protection FET gate during nominal and low battery conditions. The charge pump will be enabled at the startup voltage. When the battery voltage gets sufficiently high, the Protection FET is turned off and the integrated circuit power input (VBAT pins) are supplied through the body diode of the Protection FET.

Use of the Protection FET is not necessary in systems already using a protection diode, relay or when no reverse battery protection is required.

CONTROL INPUT (VIGN)

The VIGN pin is used as a control input to the IC. The regulation circuits will function and draw current from V_{BAT} when V_{IGN} is high (active) or when the REGON pin is high. The VIGN pin has a V_{IHN-IH} power-up threshold V_{IGN-IL} typical

power-down threshold) and $V_{IGN-HYS}$ (minimum) of hysteresis. V_{IGN} is designed to operate up to max V_{BAT} battery while providing reverse battery and max V_{BAT} load dump protection.

REGON

The REGON feature permits the microcontroller to select a delayed shutdown of the 33730. It holds off the activation of the reset signals to the microcontroller after the V_{IGN} signal has transitioned. This allows the microcontroller to control the power up and power down of the main regulator outputs except for the standby supplies. The REGON pin input threshold voltages allow control by the standard 2.5 V (up to 5.0 V) logic ICs.

HARDWARE RESETS ($\overline{\text{RSTL}}$, $\overline{\text{RST3}}$, $\overline{\text{RSTH}}$, and $\overline{\text{RSTKAM}}$)

The Hardware Resets are open drain, active low outputs capable of sinking 5.0 mA current and able to withstand +7.0 V.

The $\overline{\text{RSTL}}$ control circuit monitors the V_{DDL} output. If the V_{DDL} output is out of regulation (low), the device will assert the $\overline{\text{RSTL}}$ signal low.

The $\overline{\text{RST3}}$ control circuit monitors the V_{DD3} output. If the V_{DD3} output is out of regulation (low), the device will assert the $\overline{\text{RST3}}$ signal low.

The $\overline{\text{RSTH}}$ control circuit monitors the V_{DDH} output. If the V_{DDH} output is out of regulation (low or high), the device will assert the $\overline{\text{RSTH}}$ signal low.

The $\overline{\text{RSTKAM}}$ control circuit monitors the V_{KAM} output. If the V_{KAM} output is out of regulation (low), the device will assert the $\overline{\text{RSTH}}$ signal low.

All Reset monitoring circuits have a 20 μs delay filter to avoid unintended resets caused by noise glitches on the regulator output lines.

HR TIMER

The HR (Hardware Reset) Timer provides the delay between the time when the particular regulator output voltage is in regulation and the release of the Reset signal. This delay can be programmed by a single external resistor. This solution provides better accuracy than the commonly used external RC timer. The HR Timer delay can be programmed in eight 8ms steps from 0 to 56 ms (see Table 7)

Table 7. HR Timer Delay Programming

Programming Resistor Value R_{HRT} [ohms]	Delay (typ.) [ms]
68 k	0
33 k	10
16 k	19
8.2 k	29
3.9 k	39
2.0 k	48
1.0 k	58
470	68

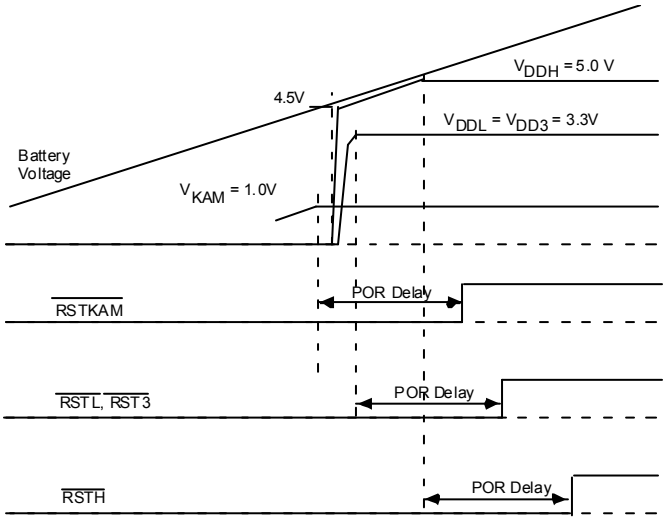


Figure 6. Battery Voltage Ramp Up

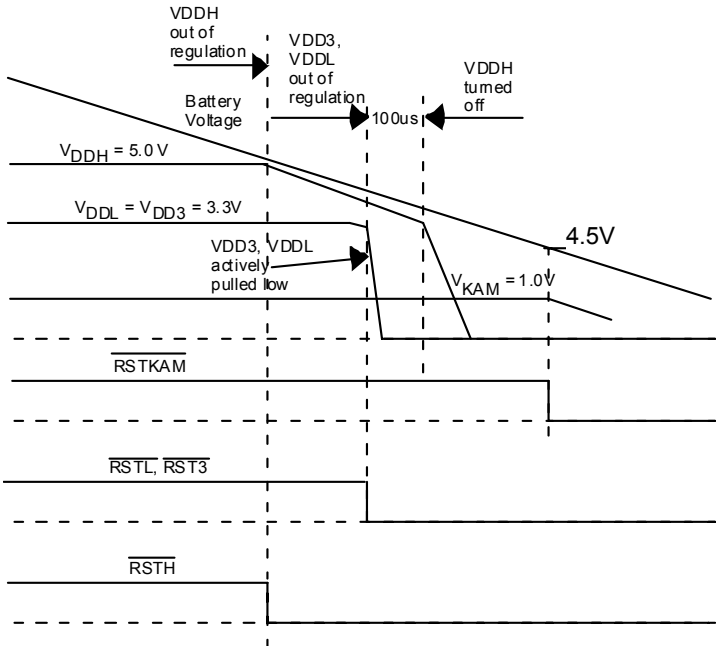


Figure 7. Battery Voltage Ramp Down

OPERATIONAL MODES

The 33730 can operate in the two modes: Low quiescent current Sleep mode and Normal mode of operation.

SLEEP MODE

The 33730 operates in the Sleep mode when both the VIGN pin and the REGON pins are pulled low. Both of these pins have internal pull-downs, which assures that the IC is in this defined state when those pins are left open.

When the IC enters the Sleep mode, all major functions are disabled except for the Standby regulators. The Keep-Alive regulator VKAM stays always operational (see Table 6). If this output stays unloaded, the IC in the Sleep mode consumes very low quiescent current (I_Q).

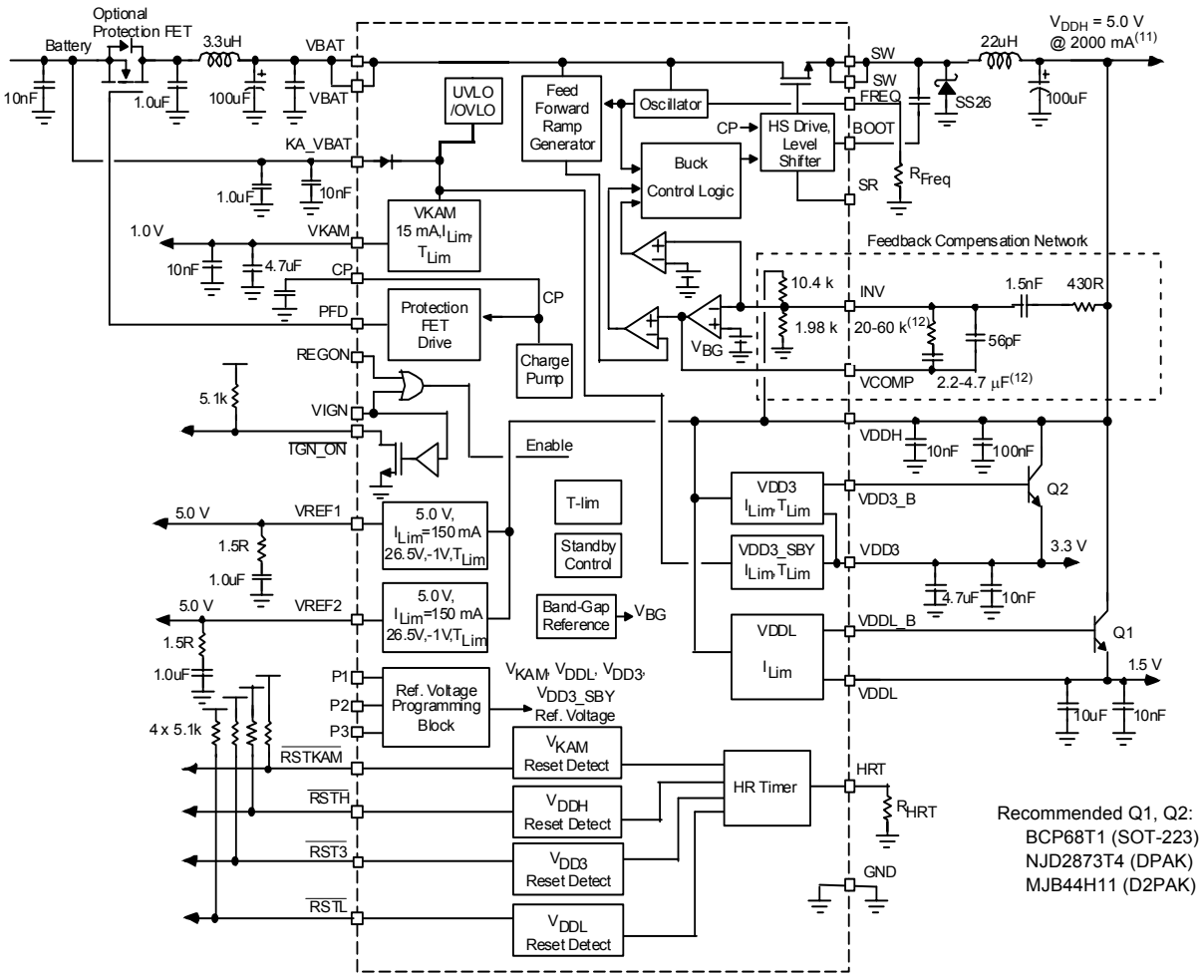
If the VDD3 output was programmed as a VDD3 Standby regulator (see Table 6), it too stays operational during the Sleep mode, as well as the VKAM regulator. In this case, the IC consumes about 100 μA of additional quiescent current (assuming both VKAM and VDD3 Standby outputs are unloaded).

NOTE: In the Sleep mode, the $\overline{\text{RSTKAM}}$ and $\overline{\text{RST3}}$ are not active and their outputs (as well as the outputs of $\overline{\text{RSTL}}$ and $\overline{\text{RSTH}}$) are in the high-impedance state.

NORMAL MODE

The 33730 enters the Normal mode of operation when either the VIGN pin or the REGON pin is pulled high. In this case the IC is fully operational with all regulator outputs ready to supply power and all control, monitoring and protection features activated.

TYPICAL APPLICATIONS



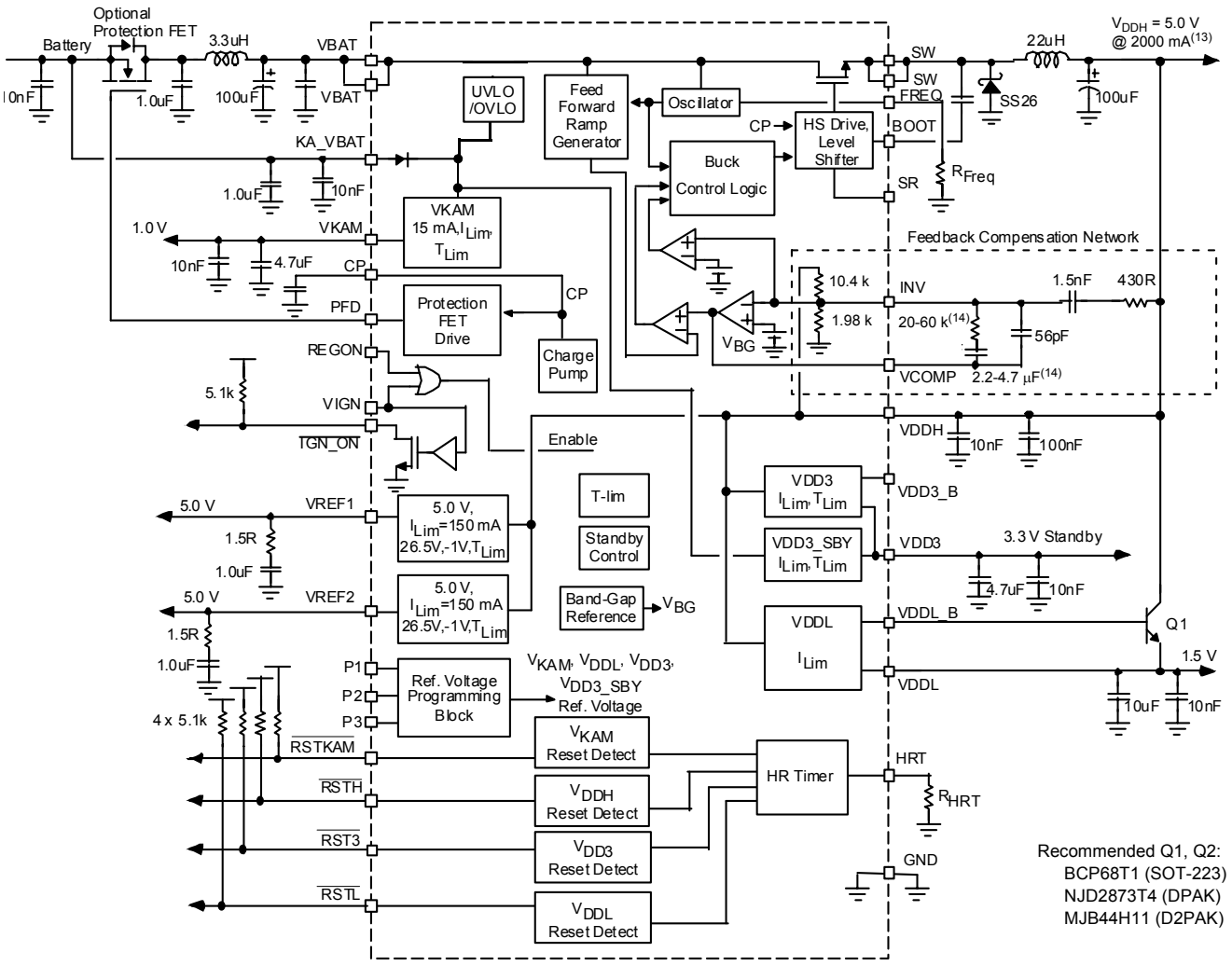
Notes

11. The V_{DDH} total current includes the sum of all output currents of the IC.
12. Higher resistance (60 k) and higher capacitance (4.7µF) in the compensation network will reduce the V_{DDH} overshoot. Compensation network values should be optimized for specific circuit applications.

Figure 8. 33730 Typical Application Circuit

Table 8. Programming Output Voltage (BOLD denotes selected combinations)

P1	P2	P3	V_{DD3}	V_{DDL}	V_{KAM}
High	High	High	3.3 V	2.6 V	2.6 V
High	High	Low	3.3 V	3.3 V	3.3 V
High	Low	High	3.3 V	1.5 V	1.0 V
High	Low	Low	3.3 V	3.3 V	1.0 V
Low	High	High	3.3 V Standby	3.3 V	1.0 V
Low	High	Low	2.0 V	3.15 V	5.0 V
Low	Low	High	2.6 V Standby	3.3 V	1.0 V
Low	Low	Low	2.6 V Standby	3.3 V	1.5 V



Notes

13. The V_{DDH} total current includes the sum of all output currents of the IC.
14. Higher resistance (60 k) and higher capacitance (4.7µF) in the compensation network will reduce the V_{DDH} overshoot. Compensation network values should be optimized for specific circuit applications.

Figure 9. 33730 Typical Application, VDD3 Standby Output @ 15 mA

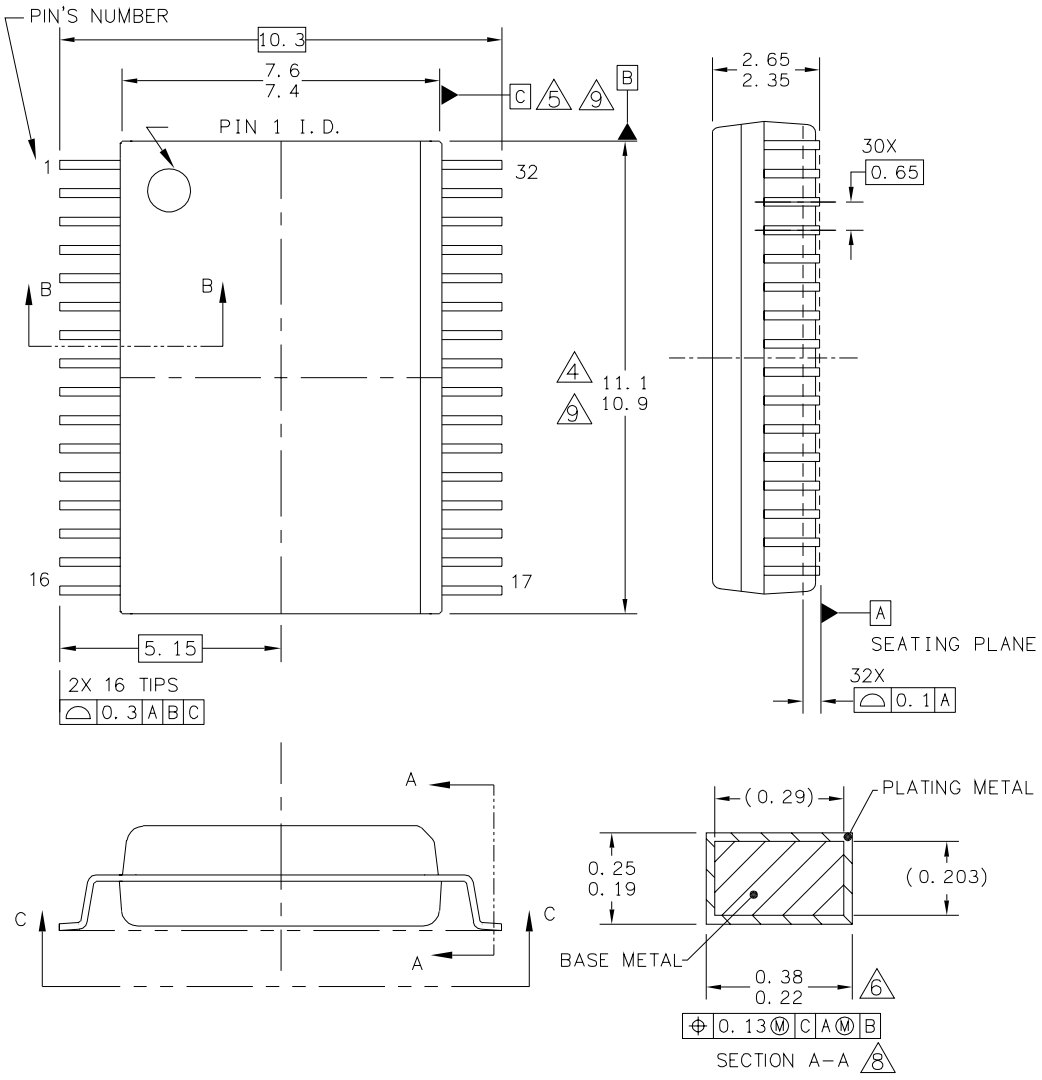
Table 9. Programming Output Voltage (BOLD denotes selected combinations)'

P1	P2	P3	V_{DD3}	V_{DDL}	V_{KAM}
High	High	High	3.3V	2.6V	2.6V
High	High	Low	3.3V	3.3V	3.3V
High	Low	High	3.3V	1.5V	1.0V
High	Low	Low	3.3V	3.3V	1.0V
Low	High	High	3.3 V Standby	3.3 V	1.0 V
Low	High	Low	2.0 V	3.15 V	5.0 V
Low	Low	High	2.6 V Standby	3.3 V	1.0 V
Low	Low	Low	2.6 V Standby	3.3 V	1.5 V

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the 98ARL10543D listed below.

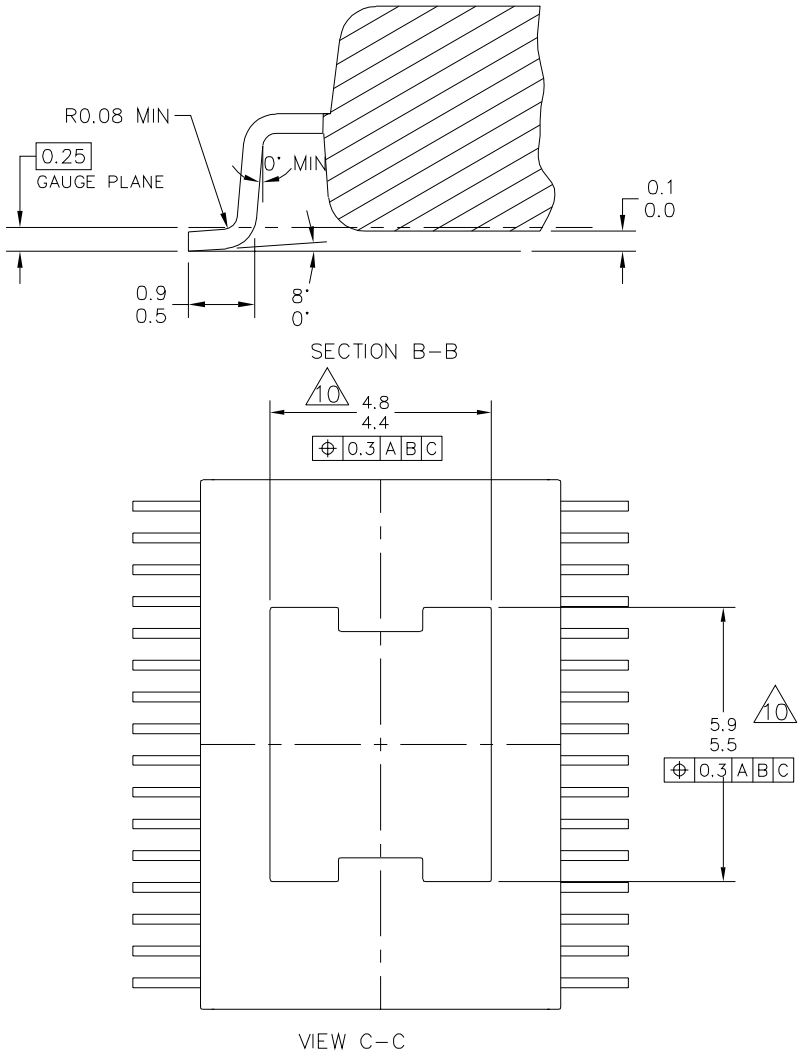


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TITLE: 32LD SOIC W/B, 0.65 PITCH 5.7 X 4.6 EXPOSED PAD CASE OUTLINE	DOCUMENT NO: 98ARL10543D	REV: C
	CASE NUMBER: 1437-03	08 MAY 2008
	STANDARD: NON-JEDEC	

EK SUFFIX (PB-FREE)
32-PIN SOICW - EP
98ARL10543D
REVISION C

33730

PACKAGE DIMENSIONS (Continued)



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TITLE: 32LD SOIC W/B, 0.65 PITCH 5.7 X 4.6 EXPOSED PAD CASE OUTLINE	DOCUMENT NO: 98ARL10543D		REV: C
	CASE NUMBER: 1437–03		08 MAY 2008
	STANDARD: NON–JEDEC		

EK SUFFIX (PB-FREE)
32-PIN SOICW - EP
98ARL10543D
REVISION C

PACKAGE DIMENSIONS (Continued)

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.9mm FROM MAXIMUM EXPOSED PAD SIZE

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MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 32LD SOIC W/B, 0.65 PITCH 5.7 X 4.6 EXPOSED PAD CASE OUTLINE	DOCUMENT NO: 98ARL10543D	REV: C
	CASE NUMBER: 1437–03	08 MAY 2008
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
32-PIN SOICW - EP
98ARL10543D
REVISION C

33730

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
5.0	2/2009	• Initial Release
6.0	2/2010	• Updated resistors on the INV pin (page 2, 20, 21) • Clarified REGON pin operation (page 3, 9, 11, 14) • Added sensor supply max. slew rate (page 5,17) • Clarified POR delay section with updated typical values (page 10,18) • Modified the SW rise and fall time to V/ns (page 10) • Provided a switching frequency equation (page 15) • Updated the recommended compensation network values (page 20,21) • Made format layout corrections

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