

Intel® Celeron® D Processor 3xx$^{\Delta}$ Sequence

Datasheet

– On 90 nm Process in the 478-pin Package

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Revision History

Revision Number	Description	Date
-001	• Initial release	June 2004
-002	• Minor updates for clarity	July 2004
-003	• Added 2.93 GHz processor	September 2004
-004	• Added 3.06 GHz processor	November 2004
-005	• Added 3.20 GHz processor (processor number 350)	June 2005



Intel® Celeron® D Processor 3xx Sequence Features

- Available at 3.20 GHz, 3.06 GHz, 2.93 GHz, 2.80 GHz, 2.66 GHz, 2.53 GHz, and 2.40 GHz
- Binary compatible with applications running on previous members of the Intel microprocessor line
- FSB frequencies at 533 MHz
- Hyper-Pipelined Technology
  - —Advance Dynamic Execution
  - —Very deep out-of-order execution
- Enhanced branch prediction
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- 478-Pin Package
- 16-KB Level 1 data cache
- 256-KB Advanced Transfer Cache (on-die, full-speed Level 2 (L2) cache) with 4-way associativity and Error Correcting Code (ECC)
- 144 Streaming SIMD Extensions 2 (SSE2) instructions
- 13 Streaming SIMD Extensions 3 (SSE3) instructions
- Power Management capabilities
  - —System Management mode
  - —Multiple low-power states

The Intel® Celeron® D processor family expands Intel's processor family into the value-priced PC market segment. Celeron D processors provide the value that offers the customer the capability to affordably get onto the Internet, and use educational programs, home-office software, and productivity applications. All of the Celeron D processors include an integrated L2 cache, and are built on Intel's advanced CMOS process technology. The Celeron D processor is backed by over 30 years of Intel experience in manufacturing high-quality, reliable microprocessors.

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1 Introduction

The Intel® Celeron® D processor on 90 nm process and in the 478-pin package uses Flip-Chip Pin Grid Array 4 (FC-mPGA4) package technology, and plugs into a 478-pin surface mount, Zero Insertion Force (ZIF) socket, referred to as the mPGA478B socket. The Celeron D processor on 90 nm process and in the 478-pin package is based on the same Intel 32-bit microarchitecture and maintains the tradition of compatibility with IA-32 software.

Note: In this document the Celeron D processor on 90 nm process in the 478-pin package will be referred to as the "Celeron D processor," or simply "the processor."

Note: In this document, unless otherwise specified, the Intel® Celeron® D processor 3xx sequence refers to Intel Celeron D processors 350, 345, 340, 335, 330, 325, and 320.

In addition to supporting all the existing Streaming SIMD Extensions 2 (SSE2), there are 13 new instructions that further extend the capabilities of Intel processor technology. These new instructions are called Steaming SIMD Extensions 3 (SSE3).

The Celeron D processor's Front Side Bus (FSB) uses a split-transaction, deferred reply protocol like the Intel® Pentium 4 processor. The FSB uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 4.2 GB/s.

Intel will enable support components for the Celeron D processor including heatsink, heatsink retention mechanism, and socket. Manufacturability is a high priority; hence, mechanical assembly may be completed from the top of the baseboard and should not require any special tooling.

The processor includes an address bus powerdown capability that removes power from the address and data pins when the FSB is not in use. This feature is always enabled on the processor.

1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

"Front Side Bus (FSB)" refers to the interface between the processor and system core logic (a.k.a. the chipset components). The FSB is a multiprocessing interface to processors, memory, and I/O.

1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- **Intel® Celeron® D processor on 90 nm process and in the 478-pin package** — Celeron D processor in the FC-mPGA4 package with a 256-KB L2 cache.
- **Processor** — For this document, the term processor is the generic form of the Celeron D processor.
- **Keep-out zone** — The area on or near the processor that system design can not use.
- **Intel® 865G/865GV/865PE/865P chipset** — Chipset that supports DDR memory technology for the Celeron D processor.
- **Intel® 845G chipset** — Chipset with embedded graphics that supports DDR memory technology. Changes are required to support the Celeron D processor on 90 nm micron process.
- **Intel® 852 GME/PM/GMV chipsets** — Intel's Portability chipsets that support DDR memory technology for the Celeron D processor
- **Processor core** — Processor core die with integrated L2 cache.
- **FC-mPGA4 package** — The Celeron D processor is available in a Flip-Chip Micro Pin Grid Array 4 package, consisting of a processor core mounted on a pinned substrate with an integrated heat spreader (IHS). This packaging technology employs a 1.27 mm [0.05 in] pitch for the substrate pins.
- **mPGA478B socket** — The Celeron D processor mates with the system board through a surface mount, 478-pin, zero insertion force (ZIF) socket.
- **Integrated heat spreader (IHS)** —A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Retention mechanism (RM)**—Since the mPGA478B socket does not include any mechanical features for heatsink attach, a retention mechanism is required. Component thermal solutions should attach to the processor via a retention mechanism that is independent of the socket.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document:

Table 1-1. References

Document	Document Number/ Location
Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide	http://developer.intel.com/design/chipsets/designex/252518.htm
Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845G/845GL Chipset Platform Design Guide	http://developer.intel.com/design/chipsets/designex/298654.htm
Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845G/845GL/ 845GV Chipset Platform Design Guide	http://developer.intel.com/design/chipsets/designex/298654.htm
Intel® Pentium® 4 Processor on 90 nm Process Thermal Design Guidelines	http://developer.intel.com/design/Pentium4/guides/300564.htm
Voltage Regulator-Down (VRD) 10.0: for Desktop Socket 478 Design Guide	http://developer.intel.com/design/Pentium4/guides/252885.htm
VRM 9.0 DC-DC Converter Design Guidelines	http://developer.intel.com/design/Pentium4/guides/249205.htm
Intel® Pentium® 4 Processor VR-Down Design Guidelines	http://developer.intel.com/design/Pentium4/guides/249891.htm
Intel® Architecture Software Developer's Manual *IA-32 Intel® Architecture Software Developer's Manual Volume 1: Basic Architecture* *IA-32 Intel® Architecture Software Developer's Manual Volume 2A: Instruction Set Reference Manual A–M* *IA-32 Intel® Architecture Software Developer's Manual Volume 2B: Instruction Set Reference Manual, N–Z* *IA-32 Intel® Architecture Software Developer's Manual Volume 3: System Programming Guide*	http://developer.intel.com/design/pentium4/manuals/index_new.htm
IA-32 Intel® Architecture and Intel® Extended Memory 64 Software Developer's Manual Documentation Changes	http://developer.intel.com/design/pentium4/manuals/index_new.htm
ITP700 Debug Port Design Guide	http://www.intel.com/design/Xeon/guides/249679.htm

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2 Electrical Specifications

This chapter describes the electrical characteristics of the processor interfaces and signals. DC electrical characteristics are provided.

2.1 FSB and GTLREF

Most Celeron D processor FSB signals use Gunning Transceiver Logic (GTL+) signaling technology. The termination voltage level for the Celeron D processor GTL+ signals is V_{CC}, which is the operating voltage of the processor core. Because of the speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families.

The GTL+ inputs require a reference voltage (GTLREF) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board (see Table 2-18 for GTLREF specifications). Termination resistors are provided on the processor silicon and are terminated to its core voltage (V_{CC}). Intel chipsets will also provide on-die termination, thus eliminating the need to terminate the bus on the system board for most GTL+ signals.

Some GTL+ signals do not include on-die termination and must be terminated on the system board. See Table 2-4 for details regarding these signals.

The GTL+ bus depends on incident wave switching. Therefore, timing calculations for GTL+ signals are based on flight time instead of capacitive deratings. Analog signal simulation of the FSB, including trace lengths, is highly recommended when designing a system.

2.2 Power and Ground Pins

For clean on-chip power distribution, the Celeron D processor has 85 VCC (power) and 179 VSS (ground) pins. All power pins must be connected to V_{CC}, while all VSS pins must be connected to a system ground plane.The processor VCC pins must be supplied by the voltage determined by the VID (Voltage identification) pins.

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 2-8. Failure to do so can result in timing violations or reduced lifetime of the component. For further information and design guidelines, refer to the applicable VRD design guide.

2.3.1 V_{CC} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep a low interconnect resistance from the regulator to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low power states, must be provided by the voltage regulator solution (VR). For more details on this topic, refer to the applicable VRD design guide.

2.3.2 FSB GTL+ Decoupling

The Celeron D processor integrates signal termination on the die as well as incorporating high frequency decoupling capacitance on the processor package. Decoupling must also be provided by the system baseboard for proper GTL+ bus operation.

2.3.3 FSB Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous generation processors, the Celeron D processor core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier will be set at its default ratio during manufacturing.

The Celeron D processor uses a differential clocking implementation. For more information on the Celeron D processor clocking, refer to the *CK409 Clock Synthesizer/Driver Specification or CK408 Clock Synthesizer/Driver Specifications.*

Table 2-1. Core Frequency to FSB Multiplier Configuration

Multiplication of System Core Frequency to FSB Frequency	Processor Number	Core Frequency (133 MHz BCLK/ 533 MHz FSB)	Notes[1]
1/24	350	3.20 GHz	—
1/23	345	3.06 GHz	—
1/22	340	2.93 GHz	—
1/21	335	2.80 GHz	—
1/20	330	2.66 GHz	—
1/19	325	2.53 GHz	—
1/18	320	2.40 GHz	—

NOTES:
1. Individual processors operate only at or below the rated frequency.

2.4 Voltage Identification

The VID specification for the Celeron D processor is supported by the applicable VRD design guide. The voltage set by the VID pins is the maximum voltage allowed by the processor. A minimum voltage is provided in Table 2-8 and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator can work with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same speed may have different VID settings.

The Celeron D processor uses six voltage identification pins, VID[5:0], to support automatic selection of power supply voltages. Table 2-2 specifies the voltage level corresponding to the state of VID[5:0]. A '1' in this table refers to a high voltage level and a '0' refers to low voltage level. If the processor socket is empty (VID[5:0] = x11111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself. See the applicable VRD design guide for more details.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

The Celeron D processor's Voltage Identification circuit requires an independent 1.2 V supply and some other power sequencing considerations.

Table 2-2. Voltage Identification Definition

VID5	VID4	VID3	VID2	VID1	VID0	VID
1	0	1	0	0	1	0.850
1	0	1	0	0	0	0.875
1	0	0	1	1	1	0.900
1	0	0	1	1	0	0.925
1	0	0	1	0	1	0.950
1	0	0	1	0	0	0.975
1	0	0	0	1	1	1.000
1	0	0	0	1	0	1.025
1	0	0	0	0	1	1.050
1	0	0	0	0	0	1.075
1	1	1	1	1	1	VR output off
1	1	1	1	1	0	1.100
1	1	1	1	0	1	1.125
1	1	1	1	0	0	1.150
1	1	1	0	1	1	1.175
1	1	1	0	1	0	1.200

VID5	VID4	VID3	VID2	VID1	VID0	VID
1	1	1	0	0	1	1.225
1	1	1	0	0	0	1.250
1	1	0	1	1	1	1.275
1	1	0	1	1	0	1.300
1	1	0	1	0	1	1.325
1	1	0	1	0	0	1.350
1	1	0	0	1	1	1.375
1	1	0	0	1	0	1.400
1	1	0	0	0	1	1.425
1	1	0	0	0	0	1.450
1	0	1	1	1	1	1.475
1	0	1	1	1	0	1.500
1	0	1	1	0	1	1.525
1	0	1	1	0	0	1.550
1	0	1	0	1	1	1.575
1	0	1	0	1	0	1.600

2.4.1 Phase Lock Loop (PLL) Power and Filter

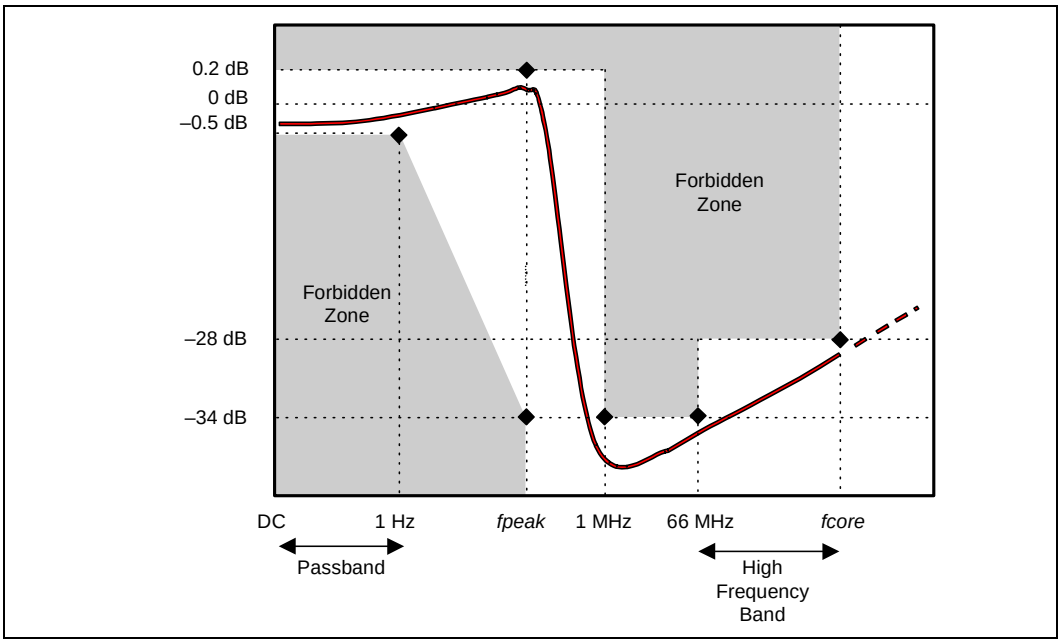
V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the Celeron D processor silicon. Since these PLLs are analog, they require low noise power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{CC}.

The AC low-pass requirements, with input at V_{CC} are as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in Figure 2-1.

Figure 2-1. Phase Lock Loop (PLL) Filter Requirements



NOTES:
1. Diagram not to scale.
2. No specification exists for frequencies beyond fcore (core frequency).
3. fpeak, if existent, should be less than 0.05 MHz.

2.5 Reserved, Unused, and TESTHI Pins

All RESERVED pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Chapter 4 for a pin listing of the processor and the location of all RESERVED pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. In a system-level design, on-die termination has been included on the Celeron D processor to allow signals to be terminated within the processor silicon. Most unused GTL+ inputs should be left as no connects, as GTL+ termination is provided on the processor silicon. However, see Table 2-4 for details on GTL+ signals that do not include on-die termination. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected; however, this may interfere with some test access port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused GTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors (R_{TT}). See Table 2-18.

TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Inputs and used outputs must be terminated on the system board. Unused outputs may be terminated on the system board or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing.

The TESTHI pins must be tied to the processor V_{CC} using a matched resistor, where a matched resistor has a resistance value within ±20% of the impedance of the board transmission line traces. For example, if the trace impedance is 60 Ω, then a value between 48 Ω and 72 Ω is required.

The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. A matched resistor must be used for each group:

- TESTHI[1:0]
- TESTHI[7:2]
- TESTHI8 – cannot be grouped with other TESTHI signals
- TESTHI9 – cannot be grouped with other TESTHI signals
- TESTHI10 – cannot be grouped with other TESTHI signals
- TESTHI11 – cannot be grouped with other TESTHI signals
- TESTHI12 – cannot be grouped with other TESTHI signals

2.6 FSB Signal Groups

The FSB signals have been combined into groups by buffer type. GTL+ input signals have differential input buffers that use GTLREF as a reference level. In this document, the term "GTL+ Input" refers to the GTL+ input group as well as the GTL+ I/O group when receiving. Similarly, "GTL+ Output" refers to the GTL+ output group as well as the GTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals that are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals that are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 2-3 identifies which signals are common clock, source synchronous, and asynchronous.

Table 2-3. FSB Pin Groups

Signal Group	Type	Signals[1]
GTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, RS[2:0]#, RSP#, TRDY#
GTL+ Common Clock I/O	Synchronous to BCLK[1:0]	AP[1:0]#, ADS#, BINIT#, BNR#, BPM[5:0]#, BR0#, DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#
GTL+ Source Synchronous I/O	Synchronous to Associated strobe	**Signals** / **Associated Strobe** REQ[4:0]#, A[16:3]#[2] / ADSTB0# A[35:17]#[2] / ADSTB1# D[15:0]#, DBI0# / DSTBP0#, DSTBN0# D[31:16]#, DBI1# / DSTBP1#, DSTBN1# D[47:32]#, DBI2# / DSTBP2#, DSTBN2# D[63:48]#, DBI3# / DSTBP3#, DSTBN3#
GTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
Asynchronous GTL+ Input		A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, STPCLK#, RESET#
Asynchronous GTL+ Output		FERR#/PBE#, IERR#, THERMTRIP#
Asynchronous GTL+ Input/Output		PROCHOT#
TAP Input	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output	Synchronous to TCK	TDO
FSB Clock	Clock	BCLK[1:0], ITP_CLK[1:0][3]
Power/Other		VCC, VCCA, VCCIOPLL, VID[5:0], VSS, VSSA, GTLREF[3:0], COMP[1:0], RESERVED, TESTHI[12:0], THERMDA, THERMDC, VCC_SENSE, VSS_SENSE, VCCVID, VCCVIDLB, BSEL[1:0], SKTOCC#, DBR#[3], VIDPWRGD, BOOTSELECT, OPTIMIZED/COMPAT#, PWRGOOD

NOTES:
1. Refer to Section 4.2 for signal descriptions.
2. The value of these pins during the active-to-inactive edge of RESET# defines the processor configuration options. See Section 6.1 for details.
3. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.

Table 2-4. Signal Characteristics

Signals with R_{TT}	Signals with no R_{TT}
A[35:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BOOTSELECT[1], BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, HIT#, HITM#, LOCK#, MCERR#, OPTIMIZED/COMPAT#[1], PROCHOT#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY#	A20M#, BCLK[1:0], BPM[5:0]#, BR0#, BSEL[1:0], COMP[1:0], FERR#/PBE#, IERR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, RESET#, SKTOCC#, SLP#, SMI#, STPCLK#, TDO, TESTHI[12:0], THERMDA, THERMDC, THERMTRIP#, VID[5:0], VIDPWRGD, GTLREF[3:0], TCK, TDI, TRST#, TMS
Open Drain Signals[2]	
BSEL[1:0], VID[5:0], THERMTRIP#, FERR#/PBE#, IERR#, BPM[5:0]#, BR0#, TDO	

NOTES:
1. The OPTIMIZED/COMPAT# and BOOTSELECT pins have a 500–5000 Ω pull-up to V_{CCVID} rather than R_{TT}.
2. Signals that do not have R_{TT}, nor are actively driven to their high-voltage level.

Table 2-5. Signal Reference Voltages

GTLREF	$V_{CC}/2$	$V_{CCVID}/2$
BPM[5:0]#, LINT0/INTR, LINT1/NMI, RESET#, BINIT#, BNR#, HIT#, HITM#, MCERR#, PROCHOT#, BR0#, A[35:0]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, LOCK#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY#	A20M#, IGNNE#, INIT#, PWRGOOD[1], SLP#, SMI#, STPCLK#, TCK[1], TDI[1], TMS[1], TRST#[1]	VIDPWRGD, BOOTSELECT, OPTIMIZED/ COMPAT#

NOTES:
1. These signals also have hysteresis added to the reference voltage. See Table 2-12 for more information.

2.7 Asynchronous GTL+ Signals

Legacy input signals (such as A20M#, IGNNE#, INIT#, SMI#, SLP#, and STPCLK#) use CMOS input buffers. All of these signals follow the same DC requirements as GTL+ signals; however, the outputs are not actively driven high (during a logical 0-to-1 transition) by the processor. These signals do not have setup or hold time specifications in relation to BCLK[1:0].

All of the Asynchronous GTL+ signals are required to be asserted/de-asserted for at least six BCLKs for the processor to recognize the proper signal state. See Section 2.11 for the DC specifications for the Asynchronous GTL+ signal groups. See Section 6.2 for additional timing requirements for entering and leaving the low power states.

2.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Celeron D processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage level. Similar considerations must be made for TCK, TMS, TRST#, TDI, and TDO. Two copies of each signal may be required, with each driving a different voltage level.

2.9 FSB Frequency Select Signals (BSEL[1:0])

The BSEL[1:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). Table 2-6 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All agents must operate at the same frequency.

The Celeron D processor currently operates at a 533 MHz FSB frequency (selected by a 133 MHz BCLK[1:0] frequency). Individual processors will only operate at their specified FSB frequency.

For more information about these pins, refer to Section 4.2.

Table 2-6. BSEL[1:0] Frequency Table for BCLK[1:0]

BSEL1	BSEL0	Function
L	H	133 MHz

2.10 Absolute Maximum and Minimum Ratings

Table 2-7 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 2-7. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{CC}	Core voltage with respect to V_{SS}	- 0.3	1.55	V	1
V_{TT}	FSB termination voltage with respect to V_{SS}	- 0.3	1.55	V	1
T_C	Processor case temperature	See Chapter 5	See Chapter 5	°C	2, 3
$T_{STORAGE}$	Processor storage temperature	–40	+85	°C	2, 3

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, refer to the processor case temperature specifications.
3. This rating applies to the processor and does not include any tray or packaging.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core silicon and not at the package pins unless noted otherwise. See Chapter 4 for the pin signal definitions and signal pin assignments. Most of the signals on the processor FSB are in the GTL+ signal group. The DC specifications for these signals are listed in Table 2-10.

Previously, legacy signals and Test Access Port (TAP) signals to the processor used low-voltage CMOS buffer types. However, these interfaces now follow DC specifications similar to GTL+. The DC specifications for these signal groups are listed in Table 2-11 and Table 2-12.

Table 2-8 through Table 2-15 list the DC specifications for the Celeron D processor and are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 2-8. Voltage and Current Specifications

Symbol	Parameter		Min	Typ	Max	Unit	Notes
VID range	VID		1.250	—	1.400	V	1
V_{CC}	V_{CC}		See Table 2-9 and Figure 2-2		VID – I_{CC}(max) * 1.45 mΩ	V	2,3,4
I_{CC}	Processor Number	Core Frequency					
		I_{CC} for processor with multiple VID:	—	—		A	5
	350	3.20 GHz			73		
	345	3.06 GHz			73		
	340	2.93 GHz			73		
	335	2.80 GHz			73		
	330	2.66 GHz			73		
	325	2.53 GHz			73		
	320	2.40 GHz			73		
I_{SGNT} I_{SLP}		I_{CC} Stop-Grant	—	—		A	6,7
	350	3.20 GHz			40		
	345	3.06 GHz			40		
	340	2.93 GHz			40		
	335	2.80 GHz			40		
	330	2.66 GHz			40		
	325	2.53 GHz			40		
	320	2.40 GHz			40		
I_{TCC}	I_{CC} TCC active		—	—	I_{CC}	A	8
I_{CC_VCCA}	I_{CC} for PLL pins		—	—	60	mA	9
$I_{CC_VCCIOPLL}$	I_{CC} for I/O PLL pin		—	—	60	mA	9
I_{CC_GTLREF}	I_{CC} for GTLREF pins (all pins)		—	—	200	µA	
I_{CC_VCCVID}/ VCCVIDLB	I_{CC} for VCCVID/VCCVIDLB		—	—	150	mA	9

NOTES:
1. Individual processor VID values may be calibrated during manufacturing such that two devices at the same speed may have different VID settings.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.4 and Table 2-2 for more information.

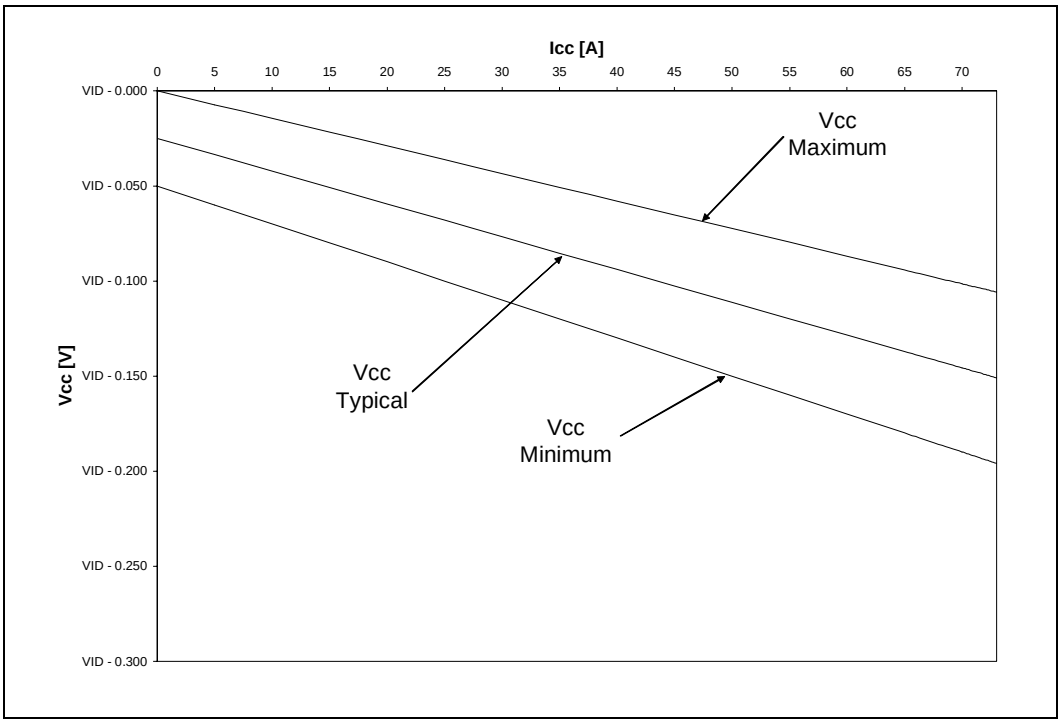
3. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE pins at the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. Refer to Table 2-9 and Figure 2-2 for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} for a given current. Moreover, V_{CC} should never exceed the VID voltage. Failure to adhere to this specification can shorten the processor lifetime.
5. I_{CC_MAX} is specified at V_{CC_MAX} .
6. The current specified is also for AutoHALT state.
7. I_{CC} Stop-Grant and I_{CC} Sleep are specified at V_{CC_MAX} .
8. The maximum instantaneous current the processor will draw while the thermal control circuit is active as indicated by the assertion of PROCHOT# is the same as the maximum I_{CC} for the processor.
9. These parameters are based on design characterization and are not tested.

Table 2-9. V_{CC} Static and Transient Tolerance

Icc (A)	Voltage Deviation from VID Setting (V)[1,2,3]		
	Maximum Voltage	Typical Voltage	Minimum Voltage
0	0.000	-0.025	-0.050
5	-0.007	-0.034	-0.060
10	-0.015	-0.042	-0.070
15	-0.022	-0.051	-0.080
20	-0.029	-0.060	-0.090
25	-0.036	-0.068	-0.100
30	-0.044	-0.077	-0.110
35	-0.051	-0.085	-0.120
40	-0.058	-0.094	-0.130
45	-0.065	-0.103	-0.140
50	-0.073	-0.111	-0.150
55	-0.080	-0.120	-0.160
60	-0.087	-0.129	-0.170
65	-0.094	-0.137	-0.180
70	-0.102	-0.146	-0.190
73	-0.106	-0.151	-0.196

NOTES:
1. The loadline specification includes both static and transient limits except for overshoot allowed as shown in Section 2.12.
2. This table is intended to aid in reading discrete points on Figure 2-3.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS pins. Refer to the *Voltage Regulator-Down (VRD) 10.0 Design Guidelines for Desktop Socket 478* for socket loadline guidelines and VR implementation details.

Figure 2-2. V_{CC} Static and Transient Tolerance



NOTES:

1. The loadline specification includes both static and transient limits except for overshoot allowed as shown in Section 2.12.
2. This loadline specification shows the deviation from the VID set point.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS pins. Refer to the *Voltage Regulator-Down (VRD) 10.0 Design Guidelines for Desktop Socket 478* for socket loadline guidelines and VR implementation details.

Table 2-10. GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	0.0	GTLREF – (0.10 * V_{CC})	V	2,3
V_{IH}	Input High Voltage	GTLREF + (0.10 * V_{CC})	V_{CC}	V	3,4,5
V_{OH}	Output High Voltage	0.90*V_{CC}	V_{CC}	V	3,5
I_{OL}	Output Low Current	N/A	V_{CC}/ [0.50*RR_{TT_MIN}+R_{ON_MIN}]	A	
I_{LI}	Input Leakage Current	N/A	± 200	µA	6
I_{LO}	Output Leakage Current	N/A	± 200	µA	7
$R_{on_compatible}$	Buffer On Resistance	6.33	10.33	Ω	8
$R_{on_optimized}$	Buffer On Resistance	8	12	Ω	8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
3. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.
4. V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CC}.
6. Leakage to V_{SS} with pin held at V_{CC}.
7. Leakage to V_{CC} with pin held at 300 mV.
8. These specifications are different depending on whether the platform is forward compatible to the Celeron D processor or if it is optimized for the Celeron D processor. A compatible platform is one that is designed for a previous generation processor but has some level of compatibility with the Celeron D processor. An optimized platform is one designed specifically for the Celeron D processor; however, it may have some level of compatibility with previous generation processors.

Table 2-11. Asynchronous GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	0.0	V_{CC}/2 – (0.10 * V_{CC})	V	2,3
V_{IH}	Input High Voltage	V_{CC}/2 + (0.10 * V_{CC})	V_{CC}	V	3,4,5,6
V_{OH}	Output High Voltage	0.90*V_{CC}	V_{CC}	V	5,6,7
I_{OL}	Output Low Current	—	V_{CC}/[0.50*R_{TT_MIN}+R_{ON_MIN}]	A	8
I_{IL}	Input Leakage Current	N/A	± 200	µA	9
I_{LO}	Output Leakage Current	N/A	± 200	µA	10
$R_{on_compatible}$	Buffer On Resistance	6.33	10.33	W	11
$R_{on_optimized}$	Buffer On Resistance	8	12	W	11

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
3. LINT0/INTR and LINT1/NMI use GTLREF as a reference voltage. For these two signals V_{IH} = GTLREF + (0.10 * V_{CC}) and V_{IL}= GTLREF – (0.10 * V_{CC}).
4. V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CC}.
6. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
7. All outputs are open drain.
8. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
9. Leakage to V_{SS} with pin held at V_{CC}.
10. Leakage to V_{CC} with pin held at 300 mV.

11. These specifications are different depending on whether the platform is forward compatible to the Celeron D processor or if it is optimized for the Celeron D processor. A compatible platform is one that is designed for a previous generation processor but has some level of compatibility with the Celeron D processor. An optimized platform is one designed specifically for the Celeron D processor; however, it may have some level of compatibility with previous generation processors.

Table 2-12. PWRGOOD and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1,2]
V_{HYS}	Input Hysteresis	200	350	mV	3
V_{T+}	Input low to high threshold voltage	0.5 * (V_{CC} + V_{HYS_MIN})	0.5 * (V_{CC} + V_{HYS_MAX})	V	4
V_{T-}	Input high to low threshold voltage	0.5 * (V_{CC} – V_{HYS_MAX})	0.5 * (V_{CC} – V_{HYS_MIN})	V	4
V_{OH}	Output High Voltage	N/A	V_{CC}	V	4
I_{OL}	Output Low Current	—	45	mA	5
I_{LI}	Input Leakage Current	—	± 200	µA	6
I_{LO}	Output Leakage Current	—	± 200	µA	7
Ron	Buffer On Resistance	7	12	Ω	8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open drain.
3. V_{HYS} represents the amount of hysteresis, nominally centered about 0.5 * V_{CC} for all TAP inputs.
4. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
5. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
6. Leakage to V_{SS} with pin held at V_{CC}.
7. Leakage to V_{CC} with Pin held at 300 mV.
8. These values work for compatible and optimized platforms. A compatible platform is one that is designed for a previous generation processor but has some level of compatibility with the Celeron D processor. An optimized platform is one designed specifically for the Celeron D processor; however, it may have some level of compatibility with previous generation processors.

Table 2-13. VCCVID DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VCCVID	Voltage	1.14	1.2	1.26	V	
VCCVIDLB	Voltage	1.14	1.2	1.26	V	

Table 2-14. VIDPWRGD DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input Low Voltage	—	—	0.3	V	
V_{IH}	Input High Voltage	0.9	—	—	V	

Table 2-15. BSEL [1:0] and VID[5:0] DC Specifications

Symbol	Parameter	Max	Unit	Notes[1]
R_{on} (BSEL)	Buffer On Resistance	60	Ω	2
R_{on} (VID)	Buffer On Resistance	60	Ω	2
I_{OL}	Max Pin Current	8	mA	
I_{LO}	Output Leakage Current	200	µA	3
V_{TOL}	Voltage Tolerance	3.3 + 5%	V	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are not tested and are based on design simulations.
3. Leakage to V_{SS} with pin held at 2.5 V.

Table 2-16. BOOTSELECT DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	—	—	0.2 * VCCVID	V	
V_{IH}	Input High Voltage	0.8 * VCCVID	—	—	V	

NOTES:
1. These parameters are not tested and are based on design simulations.

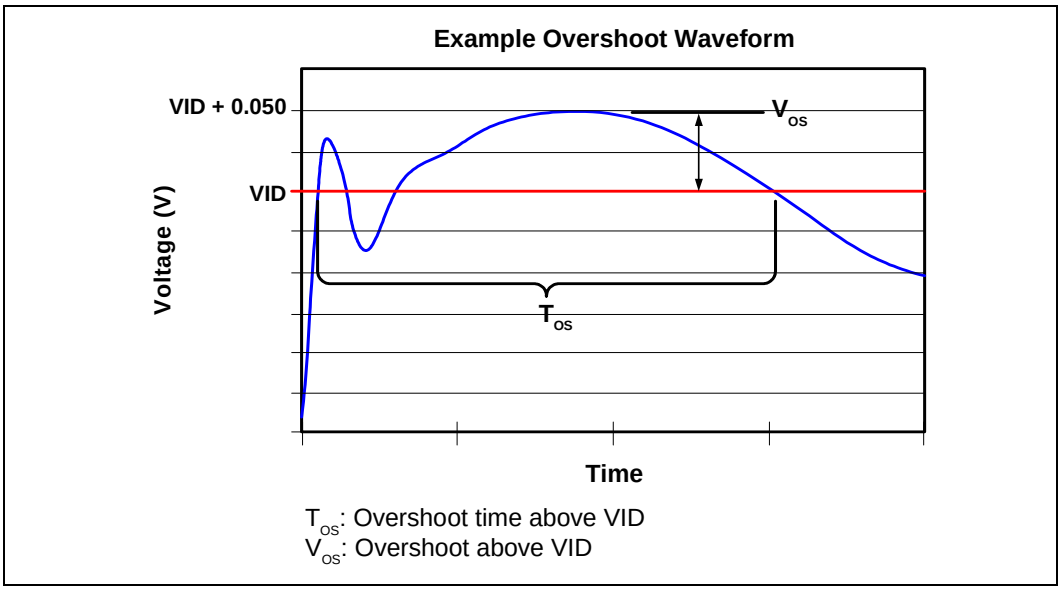
2.12 V_{CC} Overshoot Specification

The Celeron D processor can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage when transitioning from a high to low current load condition. This overshoot cannot exceed VID + V_{OS_MAX} (V_{OS_MAX} is the maximum allowable overshoot voltage). The time duration of the overshoot event must not exceed T_{OS_MAX} (T_{OS_MAX} is the maximum allowable time duration above VID). These specifications apply to the processor die voltage as measured across the VCC_SENSE and VSS_SENSE pins.

Table 2-17. V_{CC} Overshoot Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CC} overshoot above VID	—	—	0.050	V	2-3	
T_{OS_MAX}	Time duration of V_{CC} overshoot above VID	—	—	25	µs	2-3	

Figure 2-3. V_{CC} Overshoot Example Waveform



NOTES:
1. V_{OS} is measured overshoot voltage.
2. T_{OS} is measured time duration above VID.

2.12.1 Die Voltage Validation

Overshoot events from application testing on real processors must meet the specifications in Table 2-17 when measured across the VCC_SENSE and VSS_SENSE pins. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

2.13 GTL+ FSB Specifications

Termination resistors are not required for most GTL+ signals; they are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers that compare a signal's voltage with a reference voltage called GTLREF. Table 2-18 lists the GTLREF specifications. The GTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits.

Table 2-18. GTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
$GTLREF_{_compatible}$	Bus Reference Voltage	0.98 * (2/3 V_{CC})	2/3 V_{CC}	1.02 * (2/3 V_{CC})	V	2,3,4,5
$GTLREF_{_optimized}$	Bus Reference Voltage	(0.98 * 0.63) * V_{CC}	0.63 * V_{CC}	(1.02 * 0.63) * V_{CC}	V	2,3,4,5
$R_{_pullup}$	On die pull-up for BOOTSELECT and OPTIMIZED/ COMPAT# pins	500	—	5000	Ω	5,6
$R_{TT_compatible}$	Termination Resistance	45	50	55	Ω	5,7
$R_{TT_optimized}$	Termination Resistance	54	60	66	Ω	5
$COMP[1:0]_{_compatible}$	COMP Resistance	49.4	49.9	50.4	Ω	5,8
$COMP[1:0]_{_optimized}$	COMP Resistance	61.3	61.9	62.5	Ω	5,8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The tolerances for this specification have been stated generically to enable the system designer to calculate the minimum and maximum values across the range of V_{CC}.
3. GTLREF should be generated from V_{CC} by a voltage divider of 1% resistors or 1% matched resistors.
4. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.
5. These specifications are different depending on whether the platform is forward compatible to the Celeron D processor or if it is optimized for the Celeron D processor. A compatible platform is one that is designed for a previous generation processor but has some level of compatibility with the Celeron D processor. An optimized platform is one designed specifically for the Celeron D processor; however, it may have some level of compatibility with previous generation processors.
6. These pull-ups are to the internal V_{CCVID} supply.
7. R_{TT} is the on-die termination resistance measured at V_{CC}/2 of the GTL+ output driver.
8. COMP resistance must be provided on the system board with 1% resistors.

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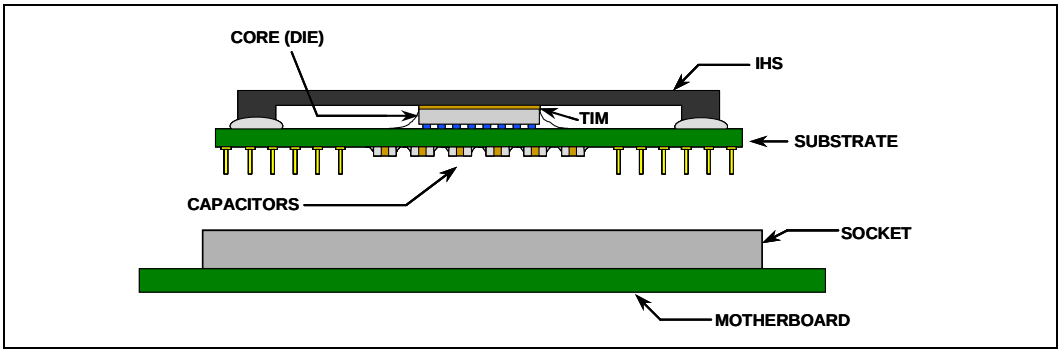
3 Package Mechanical Specifications

The Celeron D processor is packaged in a Flip-Chip Pin Grid Array (FC-mPGA4) package that interfaces with the motherboard via a mPGA478B socket. The package consists of a processor core mounted on a substrate pin-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions (such as a heatsink). Figure 3-1 shows a sketch of the processor package components and how they are assembled together. Refer to the *mPGA479, mPGA478A, mPGA478B, mPGA478C, and mPGA476 Socket Design Guidelines* for complete details on the mPGA478B socket.

The package components shown in Figure 3-1 include the following:

- Integrated Heat Spreader (IHS)
- Thermal Interface Material (TIM)
- Processor core (die)
- Package substrate
- Capacitors

Figure 3-1. Processor Package Assembly Sketch



NOTE:
1. Socket and motherboard are included for reference and are not part of processor package.

3.1 Package Mechanical Drawing

The package mechanical drawings are shown in Figure 3-2 and Figure 3-3. The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions include:

- Package reference with tolerances (total height, length, width, etc.)
- IHS parallelism and tilt
- Pin dimensions
- Top-side and back-side component keep-out dimensions
- Reference datums

All drawing dimensions are in mm [in].

Figure 3-2. Processor Package Drawing (Sheet 1 of 2)

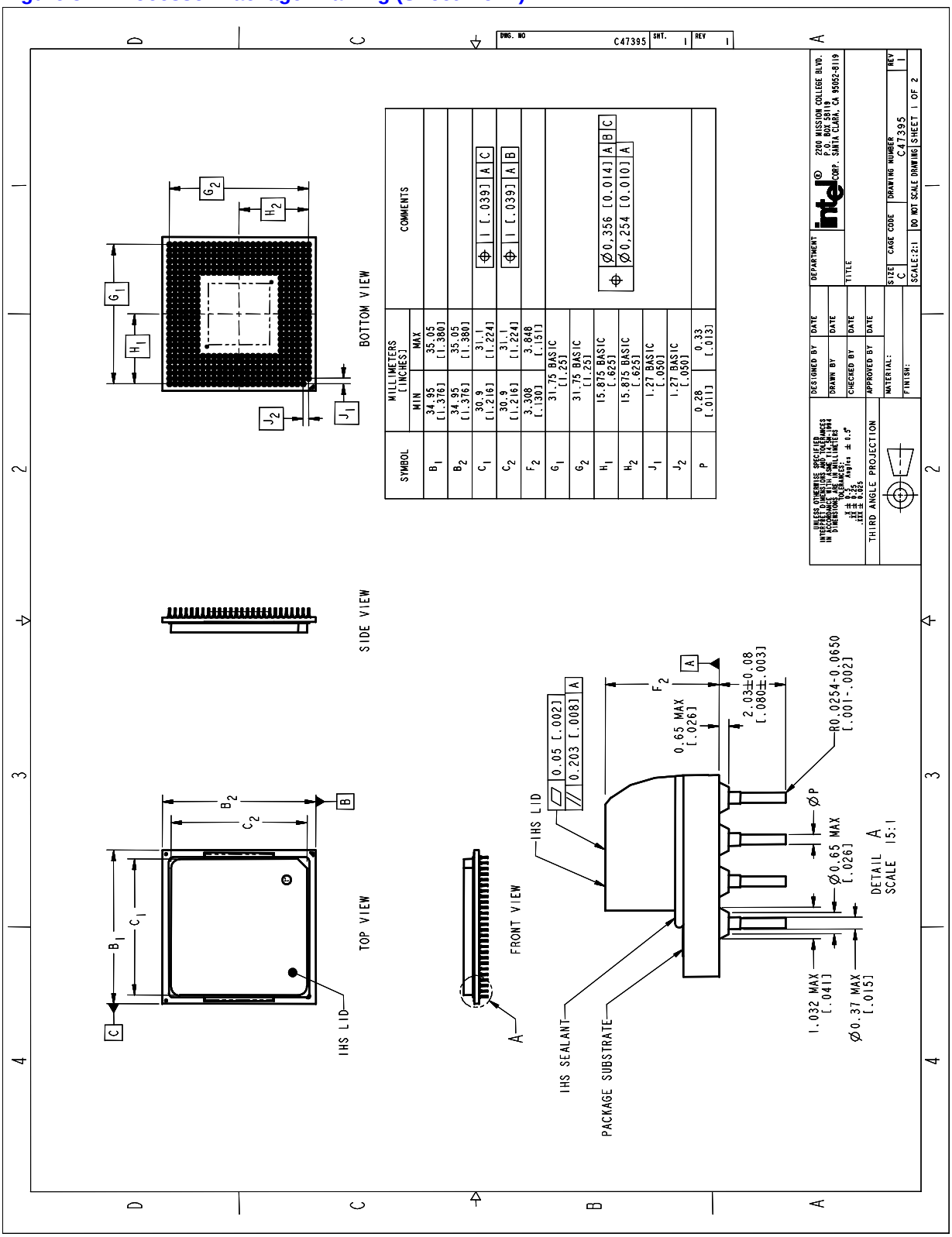
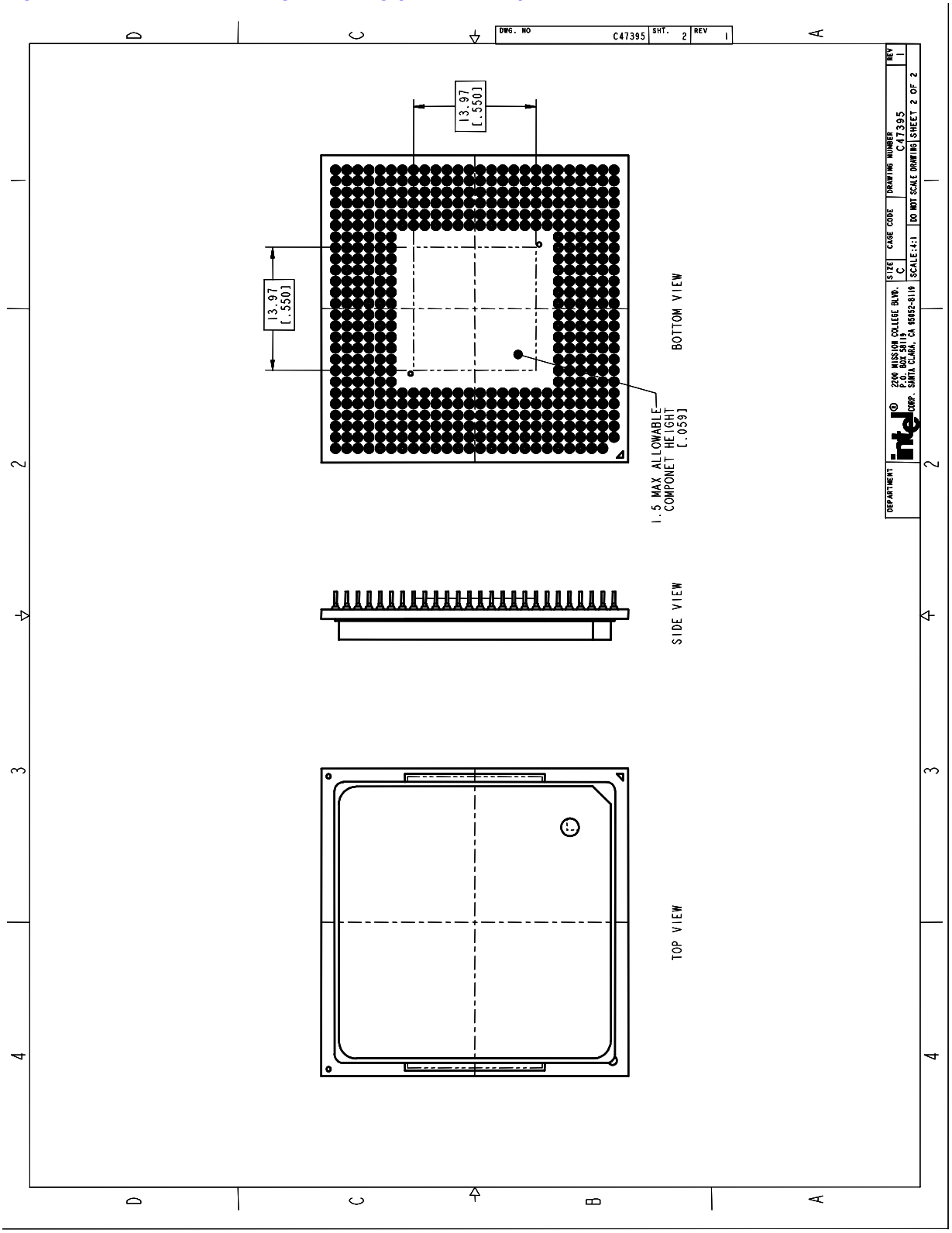


Figure 3-3. Processor Package Drawing (Sheet 2 of 2)



3.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted to either the topside or pin-side of the package substrate. See Figure 3-2 and Figure 3-3 for keep-out zones.

The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in.

3.3 Package Loading Specifications

Table 3-1 provides dynamic and static load specifications for the processor package. These mechanical maximum load limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Also, any mechanical system or component testing should not exceed the maximum limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solution. The minimum loading specification must be maintained by any thermal and mechanical solutions.

Table 3-1. Processor Loading Specifications

Parameter	Minimum	Maximum	Notes
Static	44 N [10 lbf]	445 N [100 lbf]	1,2,3
Dynamic	—	890 N [200 lbf]	1,3,4
Transient	—	667 N [150 lbf]	1,3,5

NOTES:
1. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
2. This is the maximum force that can be applied by a heatsink retention clip. The clip must also provide the minimum specified load on the processor package.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only and does not include the limits of the processor socket.
4. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
5. Transient loading is defined as a 2 second duration peak load superimposed on the static load requirement, representative of loads experienced by the package during heatsink installation.

3.4 Package Handling Guidelines

Table 3-2 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 3-2. Package Handling Guidelines

Parameter	Maximum Recommended	Notes
Shear	356 N [80 lbf]	1,2
Tensile	156 N [35 lbf]	2,3
Torque	8 N-m [70 lbf-in]	2,4

NOTES:
1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. These guidelines are based on limited testing for design characterization.
3. A tensile load is defined as a pulling load applied to the IHS in a direction normal to the IHS surface.
4. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.

3.5 Package Insertion Specifications

The Celeron D processor can be inserted into and removed from a mPGA478B socket 15 times. The socket should meet the mPGA478B requirements detailed in the *mPGA479, mPGA478A, mPGA478B, mPGA478C, and mPGA476 Socket Design Guidelines.*

3.6 Processor Mass Specification

The typical mass of the Celeron D processor is 19 g [0.67 oz]. This mass [weight] includes all the components that are included in the package.

3.7 Processor Materials

Table 3-3 lists some of the package components and associated materials.

Table 3-3. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Fiber Reinforced Resin
Substrate Pins	Gold Plated Copper

3.8 Processor Markings

Figure 3-5 and Figure 3-5 show the topside markings on the processor. These diagrams are to aid in the identification of the Celeron D processor.

Figure 3-4. Processor Top-Side Marking Example (with Processor Number)

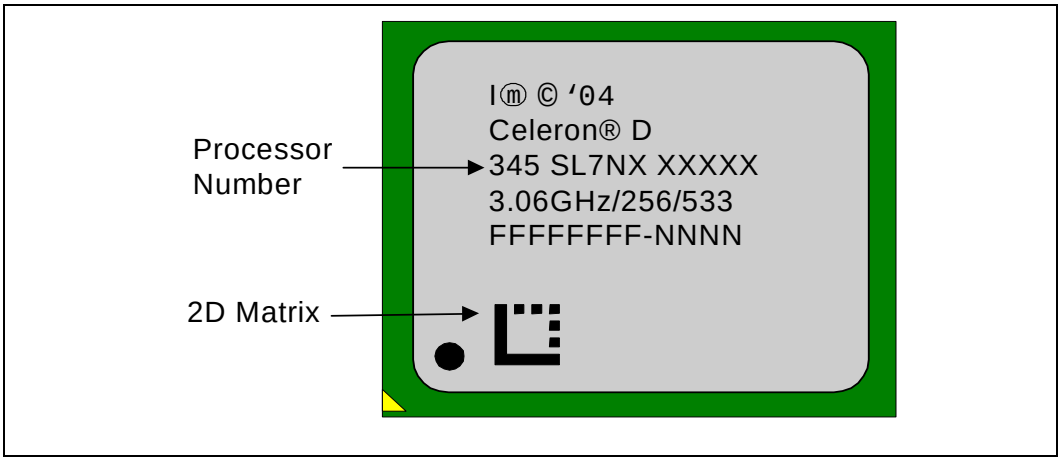
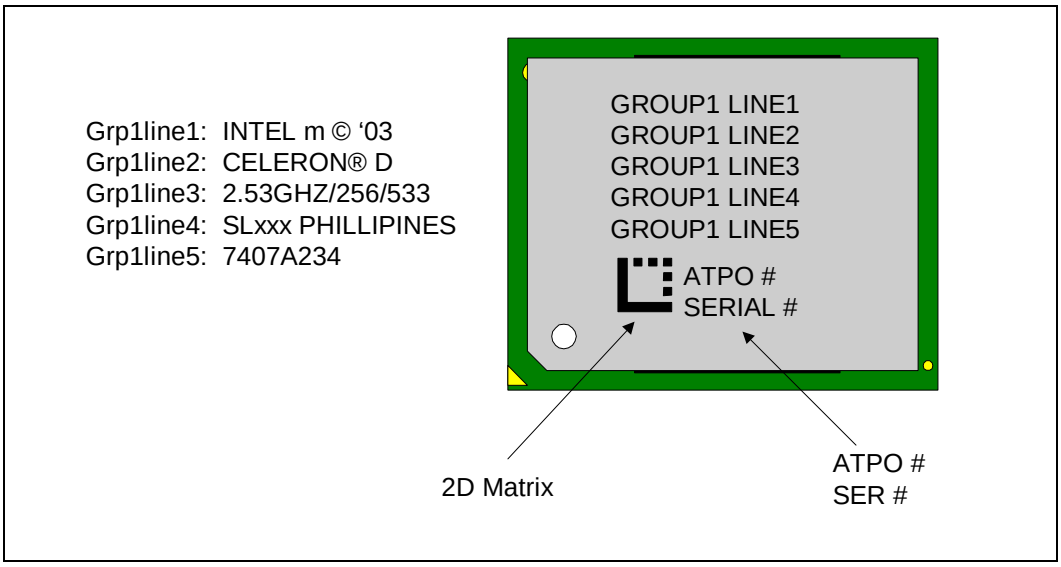


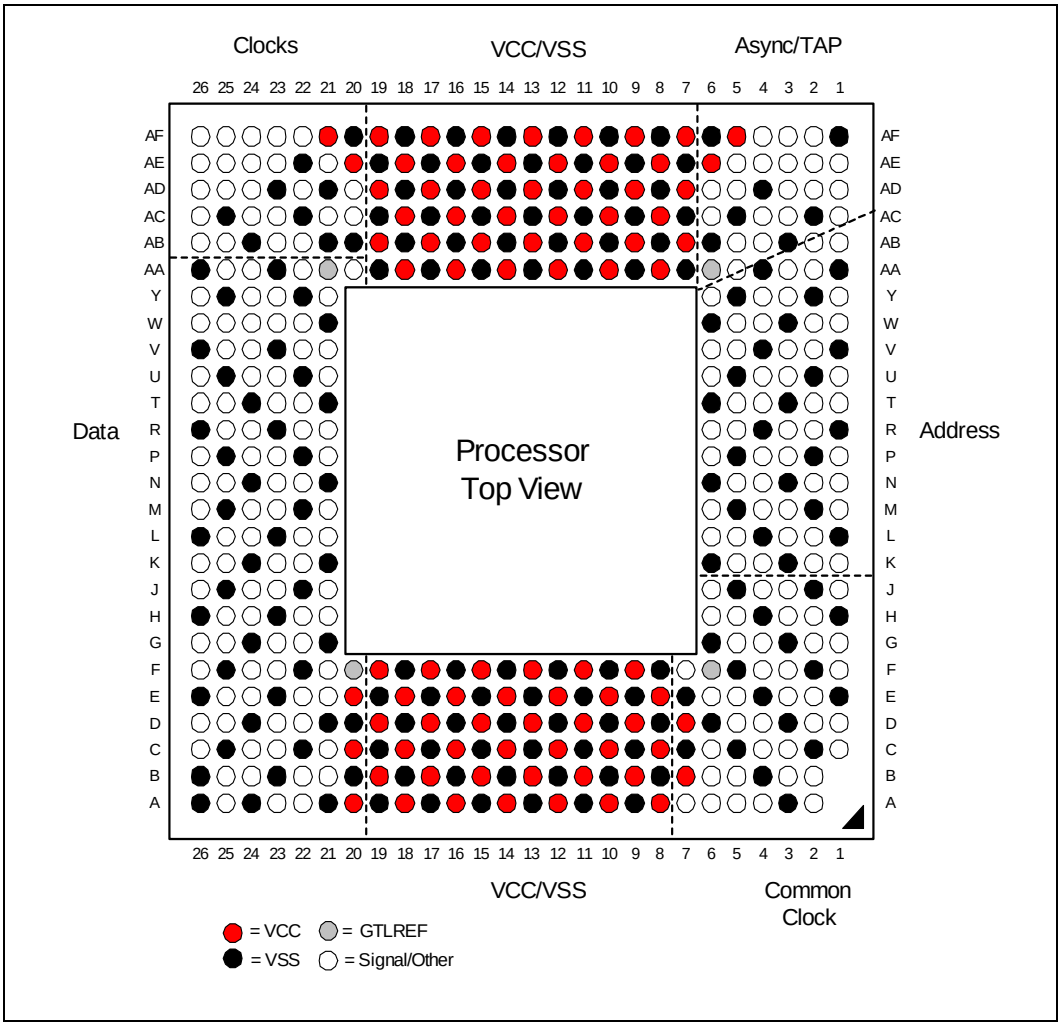
Figure 3-5. Processor Top-Side Marking Example



3.9 Processor Pinout Coordinates

Figure 3-6 shows the top view of the processor pin coordinates. The coordinates are referred to throughout the document to identify processor pins

Figure 3-6. Processor Pinout Coordinates (Top View)



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4 Pin Listing and Signal Descriptions

This chapter provides the Celeron D processor pinout and signal description.

4.1 Processor Pin Assignments

The pinout footprint is shown in Figure 4-1 and Figure 4-2. These figures represent the pinout arranged by pin number. Table 4-1 provides the pinout arranged alphabetically by signal name and Table 4-2 provides the pinout arranged numerically by pin number.

Figure 4-1. Pinout Diagram (Top View—Left Side)

	26	25	24	23	22	21	20	19	18	17	16	15	14	
AF	SKTOCC#	Reserved	Reserved	BCLK1	BCLK0	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	AF
AE	OPTIMIZED/ COMPAT#	DBR#	VSS	VCCA	VSS	Reserved	VCC	VSS	VCC	VSS	VCC	VSS	VCC	AE
AD	ITP_CLK1	TESTHI12	TESTHI0	VSS	VSSA	VSS	VCCIOPLL	VCC	VSS	VCC	VSS	VCC	VSS	AD
AC	ITP_CLK0	VSS	TESTHI4	TESTHI5	VSS	TESTHI2	TESTHI3	VSS	VCC	VSS	VCC	VSS	VCC	AC
AB	SLP#	RESET#	VSS	PWR GOOD	TESTHI7	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS	AB
AA	VSS	D61#	D63#	VSS	D62#	GTLREF	TESTHI6	VSS	VCC	VSS	VCC	VSS	VCC	AA
Y	D56#	VSS	D59#	D58#	VSS	D60#								Y
W	D55#	D57#	VSS	DSTBP3#	DSTBN3#	VSS								W
V	VSS	D51#	D54#	VSS	D53#	DBI3#								V
U	D48#	VSS	D49#	D50#	VSS	D52#								U
T	D44#	D45#	VSS	D47#	D46#	VSS								T
R	VSS	D42#	D43#	VSS	DSTBN2#	D40#								R
P	DBI2#	VSS	D41#	DSTBP2#	VSS	D34#								P
N	D38#	D39#	VSS	D36#	D33#	VSS								N
M	D37#	VSS	D35#	D32#	VSS	D27#								M
L	VSS	DP3#	COMP0	VSS	D28#	D24#								L
K	DP2#	DP1#	VSS	D30#	DSTBN1#	VSS								K
J	DP0#	VSS	D29#	DSTBP1#	VSS	D14#								J
H	VSS	D31#	D26#	VSS	D16#	D11#								H
G	D25#	DBI1#	VSS	D18#	D10#	VSS								G
F	D22#	VSS	D20#	D19#	VSS	DSTBP0#	GTLREF	VCC	VSS	VCC	VSS	VCC	VSS	F
E	VSS	D21#	D17#	VSS	DSTBN0#	DBI0#	VCC	VSS	VCC	VSS	VCC	VSS	VCC	E
D	D23#	D15#	VSS	D13#	D5#	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS	D
C	D12#	VSS	D8#	D7#	VSS	D4#	VCC	VSS	VCC	VSS	VCC	VSS	VCC	C
B	VSS	D9#	D6#	VSS	D1#	D0#	VSS	VCC	VSS	VCC	VSS	VCC	VSS	B
A	VSS	D3#	VSS	D2#	Reserved	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	A
	26	25	24	23	22	21	20	19	18	17	16	15	14	

Figure 4-2. Pinout Diagram (Top View—Right Side)

	13	12	11	10	9	8	7	6	5	4	3	2	1	
AF	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCCVID	VCCVIDLB	VCC	VSS	AF
AE	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VID0	VID1	VID2	VID3	VID4	AE
AD	VCC	VSS	VCC	VSS	VCC	VSS	VCC	BSEL0	BSEL1	VSS	VID5	VIDPWRGD	BOOT SELECT	AD
AC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	BPM0#	VSS	BPM2#	IERR#	VSS	AP0#	AC
AB	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	BPM1#	BPM5#	VSS	RSP#	A35#	AB
AA	VSS	VCC	VSS	VCC	VSS	VCC	VSS	GTLREF	BPM4#	VSS	BINIT#	TESTHI1	VSS	AA
Y								BPM3#	VSS	STPCLK#	TESTHI10	VSS	A34#	Y
W								VSS	INIT#	TESTHI9	VSS	A33#	A29#	W
V								MCERR#	AP1#	VSS	A32#	A27#	VSS	V
U								TESTHI8	VSS	A31#	A25#	VSS	A23#	U
T								VSS	A30#	A26#	VSS	A22#	A17#	T
R								A28#	ADSTB1#	VSS	A21#	A18#	VSS	R
P								A24#	VSS	A20#	A19#	VSS	COMP1	P
N								VSS	A16#	A15#	VSS	A14#	A12#	N
M								A8#	VSS	A11#	A10#	VSS	A13#	M
L								A5#	ADSTB0#	VSS	A7#	A9#	VSS	L
K								VSS	REQ1#	A4#	VSS	A3#	A6#	K
J								TRDY#	VSS	REQ2#	REQ3#	VSS	REQ0#	J
H								BR0#	DBSY#	VSS	REQ4#	DRDY#	VSS	H
G								VSS	RS1#	LOCK#	VSS	BNR#	ADS#	G
F	VCC	VSS	VCC	VSS	VCC	VSS	TMS	GTLREF	VSS	RS2#	HIT#	VSS	RS0#	F
E	VSS	VCC	VSS	VCC	VSS	VCC	VSS	TRST#	LINT1	VSS	HITM#	DEFER#	VSS	E
D	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	TDO	TCK	VSS	BPRI#	LINT0	D
C	VSS	VCC	VSS	VCC	VSS	VCC	VSS	A20M#	VSS	THERMDC	PROCHOT#	VSS	TDI	C
B	VCC	VSS	VCC	VSS	VCC	VSS	VCC	FERR#/ PBE#	SMI#	VSS	THERMDA	IGNNE#		B
A	VSS	VCC	VSS	VCC	VSS	VCC	Reserved	TESTHI11	VCC_SENSE	VSS_SENSE	VSS	THERMTRIP#		A
	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
A3#	K2	Source Synch	Input/Output
A4#	K4	Source Synch	Input/Output
A5#	L6	Source Synch	Input/Output
A6#	K1	Source Synch	Input/Output
A7#	L3	Source Synch	Input/Output
A8#	M6	Source Synch	Input/Output
A9#	L2	Source Synch	Input/Output
A10#	M3	Source Synch	Input/Output
A11#	M4	Source Synch	Input/Output
A12#	N1	Source Synch	Input/Output
A13#	M1	Source Synch	Input/Output
A14#	N2	Source Synch	Input/Output
A15#	N4	Source Synch	Input/Output
A16#	N5	Source Synch	Input/Output
A17#	T1	Source Synch	Input/Output
A18#	R2	Source Synch	Input/Output
A19#	P3	Source Synch	Input/Output
A20#	P4	Source Synch	Input/Output
A21#	R3	Source Synch	Input/Output
A22#	T2	Source Synch	Input/Output
A23#	U1	Source Synch	Input/Output
A24#	P6	Source Synch	Input/Output
A25#	U3	Source Synch	Input/Output
A26#	T4	Source Synch	Input/Output
A27#	V2	Source Synch	Input/Output
A28#	R6	Source Synch	Input/Output
A29#	W1	Source Synch	Input/Output
A30#	T5	Source Synch	Input/Output
A31#	U4	Source Synch	Input/Output
A32#	V3	Source Synch	Input/Output
A33#	W2	Source Synch	Input/Output
A34#	Y1	Source Synch	Input/Output
A35#	AB1	Source Synch	Input/Output
A20M#	C6	Asynch GTL+	Input
ADS#	G1	Common Clock	Input/Output
ADSTB0#	L5	Source Synch	Input/Output
ADSTB1#	R5	Source Synch	Input/Output
AP0#	AC1	Common Clock	Input/Output
AP1#	V5	Common Clock	Input/Output
BCLK0	AF22	Bus Clock	Input
BCLK1	AF23	Bus Clock	Input

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
BINIT#	AA3	Common Clock	Input/Output
BNR#	G2	Common Clock	Input/Output
BOOTSELECT	AD1	Power/Other	Input
BPM0#	AC6	Common Clock	Input/Output
BPM1#	AB5	Common Clock	Input/Output
BPM2#	AC4	Common Clock	Input/Output
BPM3#	Y6	Common Clock	Input/Output
BPM4#	AA5	Common Clock	Input/Output
BPM5#	AB4	Common Clock	Input/Output
BPRI#	D2	Common Clock	Input
BR0#	H6	Common Clock	Input/Output
BSEL0	AD6	Power/Other	Output
BSEL1	AD5	Power/Other	Output
COMP0	L24	Power/Other	Input
COMP1	P1	Power/Other	Input
D0#	B21	Source Synch	Input/Output
D1#	B22	Source Synch	Input/Output
D2#	A23	Source Synch	Input/Output
D3#	A25	Source Synch	Input/Output
D4#	C21	Source Synch	Input/Output
D5#	D22	Source Synch	Input/Output
D6#	B24	Source Synch	Input/Output
D7#	C23	Source Synch	Input/Output
D8#	C24	Source Synch	Input/Output
D9#	B25	Source Synch	Input/Output
D10#	G22	Source Synch	Input/Output
D11#	H21	Source Synch	Input/Output
D12#	C26	Source Synch	Input/Output
D13#	D23	Source Synch	Input/Output
D14#	J21	Source Synch	Input/Output
D15#	D25	Source Synch	Input/Output
D16#	H22	Source Synch	Input/Output
D17#	E24	Source Synch	Input/Output
D18#	G23	Source Synch	Input/Output
D19#	F23	Source Synch	Input/Output
D20#	F24	Source Synch	Input/Output
D21#	E25	Source Synch	Input/Output
D22#	F26	Source Synch	Input/Output
D23#	D26	Source Synch	Input/Output
D24#	L21	Source Synch	Input/Output
D25#	G26	Source Synch	Input/Output

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
D26#	H24	Source Synch	Input/Output
D27#	M21	Source Synch	Input/Output
D28#	L22	Source Synch	Input/Output
D29#	J24	Source Synch	Input/Output
D30#	K23	Source Synch	Input/Output
D31#	H25	Source Synch	Input/Output
D32#	M23	Source Synch	Input/Output
D33#	N22	Source Synch	Input/Output
D34#	P21	Source Synch	Input/Output
D35#	M24	Source Synch	Input/Output
D36#	N23	Source Synch	Input/Output
D37#	M26	Source Synch	Input/Output
D38#	N26	Source Synch	Input/Output
D39#	N25	Source Synch	Input/Output
D40#	R21	Source Synch	Input/Output
D41#	P24	Source Synch	Input/Output
D42#	R25	Source Synch	Input/Output
D43#	R24	Source Synch	Input/Output
D44#	T26	Source Synch	Input/Output
D45#	T25	Source Synch	Input/Output
D46#	T22	Source Synch	Input/Output
D47#	T23	Source Synch	Input/Output
D48#	U26	Source Synch	Input/Output
D49#	U24	Source Synch	Input/Output
D50#	U23	Source Synch	Input/Output
D51#	V25	Source Synch	Input/Output
D52#	U21	Source Synch	Input/Output
D53#	V22	Source Synch	Input/Output
D54#	V24	Source Synch	Input/Output
D55#	W26	Source Synch	Input/Output
D56#	Y26	Source Synch	Input/Output
D57#	W25	Source Synch	Input/Output
D58#	Y23	Source Synch	Input/Output
D59#	Y24	Source Synch	Input/Output
D60#	Y21	Source Synch	Input/Output
D61#	AA25	Source Synch	Input/Output
D62#	AA22	Source Synch	Input/Output
D63#	AA24	Source Synch	Input/Output
DBI0#	E21	Source Synch	Input/Output
DBI1#	G25	Source Synch	Input/Output
DBI2#	P26	Source Synch	Input/Output

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
DBI3#	V21	Source Synch	Input/Output
DBR#	AE25	Power/Other	Output
DBSY#	H5	Common Clock	Input/Output
DEFER#	E2	Common Clock	Input
DP0#	J26	Common Clock	Input/Output
DP1#	K25	Common Clock	Input/Output
DP2#	K26	Common Clock	Input/Output
DP3#	L25	Common Clock	Input/Output
DRDY#	H2	Common Clock	Input/Output
DSTBN0#	E22	Source Synch	Input/Output
DSTBN1#	K22	Source Synch	Input/Output
DSTBN2#	R22	Source Synch	Input/Output
DSTBN3#	W22	Source Synch	Input/Output
DSTBP0#	F21	Source Synch	Input/Output
DSTBP1#	J23	Source Synch	Input/Output
DSTBP2#	P23	Source Synch	Input/Output
DSTBP3#	W23	Source Synch	Input/Output
FERR#/PBE#	B6	Asynch AGL+	Output
GTLREF	AA21	Power/Other	Input
GTLREF	AA6	Power/Other	Input
GTLREF	F20	Power/Other	Input
GTLREF	F6	Power/Other	Input
HIT#	F3	Common Clock	Input/Output
HITM#	E3	Common Clock	Input/Output
IERR#	AC3	Asynch GTL+	Output
IGNNE#	B2	Asynch GTL+	Input
INIT#	W5	Asynch GTL+	Input
ITP_CLK0	AC26	TAP	Input
ITP_CLK1	AD26	TAP	Input
LINT0	D1	Asynch GTL+	Input
LINT1	E5	Asynch GTL+	Input
LOCK#	G4	Common Clock	Input/Output
MCERR#	V6	Common Clock	Input/Output
OPTIMIZED/ COMPAT#	AE26	Power/Other	Input
PROCHOT#	C3	Asynch GTL+	Input/Output
PWRGOOD	AB23	Power/Other	Input
REQ0#	J1	Source Synch	Input/Output
REQ1#	K5	Source Synch	Input/Output
REQ2#	J4	Source Synch	Input/Output
REQ3#	J3	Source Synch	Input/Output
REQ4#	H3	Source Synch	Input/Output

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
RESERVED	A22		
RESERVED	A7		
RESERVED	AE21		
RESERVED	AF24		
RESERVED	AF25		
RESET#	AB25	Common Clock	Input
RS0#	F1	Common Clock	Input
RS1#	G5	Common Clock	Input
RS2#	F4	Common Clock	Input
RSP#	AB2	Common Clock	Input
SKTOCC#	AF26	Power/Other	Output
SLP#	AB26	Asynch GTL+	Input
SMI#	B5	Asynch GTL+	Input
STPCLK#	Y4	Asynch GTL+	Input
TCK	D4	TAP	Input
TDI	C1	TAP	Input
TDO	D5	TAP	Output
TESTHI0	AD24	Power/Other	Input
TESTHI1	AA2	Power/Other	Input
TESTHI2	AC21	Power/Other	Input
TESTHI3	AC20	Power/Other	Input
TESTHI4	AC24	Power/Other	Input
TESTHI5	AC23	Power/Other	Input
TESTHI6	AA20	Power/Other	Input
TESTHI7	AB22	Power/Other	Input
TESTHI8	U6	Power/Other	Input
TESTHI9	W4	Power/Other	Input
TESTHI10	Y3	Power/Other	Input
TESTHI11	A6	Power/Other	Input
TESTHI12	AD25	Power/Other	Input
THERMDA	B3	Power/Other	
THERMDC	C4	Power/Other	
THERMTRIP#	A2	Asynch GTL+	Output
TMS	F7	TAP	Input
TRDY#	J6	Common Clock	Input
TRST#	E6	TAP	Input
VCC	A10	Power/Other	
VCC	A12	Power/Other	
VCC	A14	Power/Other	
VCC	A16	Power/Other	
VCC	A18	Power/Other	

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	A20	Power/Other	
VCC	A8	Power/Other	
VCC	AA10	Power/Other	
VCC	AA12	Power/Other	
VCC	AA14	Power/Other	
VCC	AA16	Power/Other	
VCC	AA18	Power/Other	
VCC	AA8	Power/Other	
VCC	AB11	Power/Other	
VCC	AB13	Power/Other	
VCC	AB15	Power/Other	
VCC	AB17	Power/Other	
VCC	AB19	Power/Other	
VCC	AB7	Power/Other	
VCC	AB9	Power/Other	
VCC	AC10	Power/Other	
VCC	AC12	Power/Other	
VCC	AC14	Power/Other	
VCC	AC16	Power/Other	
VCC	AC18	Power/Other	
VCC	AC8	Power/Other	
VCC	AD11	Power/Other	
VCC	AD13	Power/Other	
VCC	AD15	Power/Other	
VCC	AD17	Power/Other	
VCC	AD19	Power/Other	
VCC	AD7	Power/Other	
VCC	AD9	Power/Other	
VCC	AE10	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE16	Power/Other	
VCC	AE18	Power/Other	
VCC	AE20	Power/Other	
VCC	AE6	Power/Other	
VCC	AE8	Power/Other	
VCC	AF11	Power/Other	
VCC	AF13	Power/Other	
VCC	AF15	Power/Other	
VCC	AF17	Power/Other	
VCC	AF19	Power/Other	

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	AF2	Power/Other	
VCC	AF21	Power/Other	
VCC	AF5	Power/Other	
VCC	AF7	Power/Other	
VCC	AF9	Power/Other	
VCC	B11	Power/Other	
VCC	B13	Power/Other	
VCC	B15	Power/Other	
VCC	B17	Power/Other	
VCC	B19	Power/Other	
VCC	B7	Power/Other	
VCC	B9	Power/Other	
VCC	C10	Power/Other	
VCC	C12	Power/Other	
VCC	C14	Power/Other	
VCC	C16	Power/Other	
VCC	C18	Power/Other	
VCC	C20	Power/Other	
VCC	C8	Power/Other	
VCC	D11	Power/Other	
VCC	D13	Power/Other	
VCC	D15	Power/Other	
VCC	D17	Power/Other	
VCC	D19	Power/Other	
VCC	D7	Power/Other	
VCC	D9	Power/Other	
VCC	E10	Power/Other	
VCC	E12	Power/Other	
VCC	E14	Power/Other	
VCC	E16	Power/Other	
VCC	E18	Power/Other	
VCC	E20	Power/Other	
VCC	E8	Power/Other	
VCC	F11	Power/Other	
VCC	F13	Power/Other	
VCC	F15	Power/Other	
VCC	F17	Power/Other	
VCC	F19	Power/Other	
VCC	F9	Power/Other	
VCCA	AE23	Power/Other	
VCCIOPLL	AD20	Power/Other	

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VCC_SENSE	A5	Power/Other	Output
VCCVID	AF4	Power/Other	Input
VCCVIDLB	AF3	Power/Other	Input
VID0	AE5	Power/Other	Output
VID1	AE4	Power/Other	Output
VID2	AE3	Power/Other	Output
VID3	AE2	Power/Other	Output
VID4	AE1	Power/Other	Output
VID5	AD3	Power/Other	Output
VIDPWRGD	AD2	Power/Other	Input
VSS	A11	Power/Other	
VSS	A13	Power/Other	
VSS	A15	Power/Other	
VSS	A17	Power/Other	
VSS	A19	Power/Other	
VSS	A21	Power/Other	
VSS	A24	Power/Other	
VSS	A26	Power/Other	
VSS	A3	Power/Other	
VSS	A9	Power/Other	
VSS	AA1	Power/Other	
VSS	AA11	Power/Other	
VSS	AA13	Power/Other	
VSS	AA15	Power/Other	
VSS	AA17	Power/Other	
VSS	AA19	Power/Other	
VSS	AA23	Power/Other	
VSS	AA26	Power/Other	
VSS	AA4	Power/Other	
VSS	AA7	Power/Other	
VSS	AA9	Power/Other	
VSS	AB10	Power/Other	
VSS	AB12	Power/Other	
VSS	AB14	Power/Other	
VSS	AB16	Power/Other	
VSS	AB18	Power/Other	
VSS	AB20	Power/Other	
VSS	AB21	Power/Other	
VSS	AB24	Power/Other	
VSS	AB3	Power/Other	
VSS	AB6	Power/Other	

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	AB8	Power/Other	
VSS	AC11	Power/Other	
VSS	AC13	Power/Other	
VSS	AC15	Power/Other	
VSS	AC17	Power/Other	
VSS	AC19	Power/Other	
VSS	AC2	Power/Other	
VSS	AC22	Power/Other	
VSS	AC25	Power/Other	
VSS	AC5	Power/Other	
VSS	AC7	Power/Other	
VSS	AC9	Power/Other	
VSS	AD10	Power/Other	
VSS	AD12	Power/Other	
VSS	AD14	Power/Other	
VSS	AD16	Power/Other	
VSS	AD18	Power/Other	
VSS	AD21	Power/Other	
VSS	AD23	Power/Other	
VSS	AD4	Power/Other	
VSS	AD8	Power/Other	
VSS	AE11	Power/Other	
VSS	AE13	Power/Other	
VSS	AE15	Power/Other	
VSS	AE17	Power/Other	
VSS	AE19	Power/Other	
VSS	AE22	Power/Other	
VSS	AE24	Power/Other	
VSS	AE7	Power/Other	
VSS	AE9	Power/Other	
VSS	AF1	Power/Other	
VSS	AF10	Power/Other	
VSS	AF12	Power/Other	
VSS	AF14	Power/Other	
VSS	AF16	Power/Other	
VSS	AF18	Power/Other	
VSS	AF20	Power/Other	
VSS	AF6	Power/Other	
VSS	AF8	Power/Other	
VSS	B10	Power/Other	
VSS	B12	Power/Other	

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	B14	Power/Other	
VSS	B16	Power/Other	
VSS	B18	Power/Other	
VSS	B20	Power/Other	
VSS	B23	Power/Other	
VSS	B26	Power/Other	
VSS	B4	Power/Other	
VSS	B8	Power/Other	
VSS	C11	Power/Other	
VSS	C13	Power/Other	
VSS	C15	Power/Other	
VSS	C17	Power/Other	
VSS	C19	Power/Other	
VSS	C2	Power/Other	
VSS	C22	Power/Other	
VSS	C25	Power/Other	
VSS	C5	Power/Other	
VSS	C7	Power/Other	
VSS	C9	Power/Other	
VSS	D10	Power/Other	
VSS	D12	Power/Other	
VSS	D14	Power/Other	
VSS	D16	Power/Other	
VSS	D18	Power/Other	
VSS	D20	Power/Other	
VSS	D21	Power/Other	
VSS	D24	Power/Other	
VSS	D3	Power/Other	
VSS	D6	Power/Other	
VSS	D8	Power/Other	
VSS	E1	Power/Other	
VSS	E11	Power/Other	
VSS	E13	Power/Other	
VSS	E15	Power/Other	
VSS	E17	Power/Other	
VSS	E19	Power/Other	
VSS	E23	Power/Other	
VSS	E26	Power/Other	
VSS	E4	Power/Other	
VSS	E7	Power/Other	
VSS	E9	Power/Other	

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	F10	Power/Other	
VSS	F12	Power/Other	
VSS	F14	Power/Other	
VSS	F16	Power/Other	
VSS	F18	Power/Other	
VSS	F2	Power/Other	
VSS	F22	Power/Other	
VSS	F25	Power/Other	
VSS	F5	Power/Other	
VSS	F8	Power/Other	
VSS	G21	Power/Other	
VSS	G24	Power/Other	
VSS	G3	Power/Other	
VSS	G6	Power/Other	
VSS	H1	Power/Other	
VSS	H23	Power/Other	
VSS	H26	Power/Other	
VSS	H4	Power/Other	
VSS	J2	Power/Other	
VSS	J22	Power/Other	
VSS	J25	Power/Other	
VSS	J5	Power/Other	
VSS	K21	Power/Other	
VSS	K24	Power/Other	
VSS	K3	Power/Other	
VSS	K6	Power/Other	
VSS	L1	Power/Other	
VSS	L23	Power/Other	
VSS	L26	Power/Other	
VSS	L4	Power/Other	
VSS	M2	Power/Other	
VSS	M22	Power/Other	
VSS	M25	Power/Other	
VSS	M5	Power/Other	
VSS	N21	Power/Other	
VSS	N24	Power/Other	
VSS	N3	Power/Other	
VSS	N6	Power/Other	
VSS	P2	Power/Other	
VSS	P22	Power/Other	
VSS	P25	Power/Other	

Table 4-1. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	P5	Power/Other	
VSS	R1	Power/Other	
VSS	R23	Power/Other	
VSS	R26	Power/Other	
VSS	R4	Power/Other	
VSS	T21	Power/Other	
VSS	T24	Power/Other	
VSS	T3	Power/Other	
VSS	T6	Power/Other	
VSS	U2	Power/Other	
VSS	U22	Power/Other	
VSS	U25	Power/Other	
VSS	U5	Power/Other	
VSS	V1	Power/Other	
VSS	V23	Power/Other	
VSS	V26	Power/Other	
VSS	V4	Power/Other	
VSS	W21	Power/Other	
VSS	W24	Power/Other	
VSS	W3	Power/Other	
VSS	W6	Power/Other	
VSS	Y2	Power/Other	
VSS	Y22	Power/Other	
VSS	Y25	Power/Other	
VSS	Y5	Power/Other	
VSSA	AD22	Power/Other	
VSS_SENSE	A4	Power/Other	Output

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
A2	THERMTRIP#	Asynch GTL+	Output
A3	VSS	Power/Other	
A4	VSS_SENSE	Power/Other	Output
A5	VCC_SENSE	Power/Other	Output
A6	TESTHI11	Power/Other	Input
A7	RESERVED		
A8	VCC	Power/Other	
A9	VSS	Power/Other	
A10	VCC	Power/Other	
A11	VSS	Power/Other	
A12	VCC	Power/Other	
A13	VSS	Power/Other	
A14	VCC	Power/Other	
A15	VSS	Power/Other	
A16	VCC	Power/Other	
A17	VSS	Power/Other	
A18	VCC	Power/Other	
A19	VSS	Power/Other	
A20	VCC	Power/Other	
A21	VSS	Power/Other	
A22	RESERVED		
A23	D2#	Source Synch	Input/Output
A24	VSS	Power/Other	
A25	D3#	Source Synch	Input/Output
A26	VSS	Power/Other	
B2	IGNNE#	Asynch GTL+	Input
B3	THERMDA	Power/Other	
B4	VSS	Power/Other	
B5	SMI#	Asynch GTL+	Input
B6	FERR#/PBE#	Asynch AGL+	Output
B7	VCC	Power/Other	
B8	VSS	Power/Other	
B9	VCC	Power/Other	
B10	VSS	Power/Other	
B11	VCC	Power/Other	
B12	VSS	Power/Other	
B13	VCC	Power/Other	
B14	VSS	Power/Other	
B15	VCC	Power/Other	
B16	VSS	Power/Other	
B17	VCC	Power/Other	

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
B18	VSS	Power/Other	
B19	VCC	Power/Other	
B20	VSS	Power/Other	
B21	D0#	Source Synch	Input/Output
B22	D1#	Source Synch	Input/Output
B23	VSS	Power/Other	
B24	D6#	Source Synch	Input/Output
B25	D9#	Source Synch	Input/Output
B26	VSS	Power/Other	
C1	TDI	TAP	Input
C2	VSS	Power/Other	
C3	PROCHOT#	Asynch GTL+	Input/Output
C4	THERMDC	Power/Other	
C5	VSS	Power/Other	
C6	A20M#	Asynch GTL+	Input
C7	VSS	Power/Other	
C8	VCC	Power/Other	
C9	VSS	Power/Other	
C10	VCC	Power/Other	
C11	VSS	Power/Other	
C12	VCC	Power/Other	
C13	VSS	Power/Other	
C14	VCC	Power/Other	
C15	VSS	Power/Other	
C16	VCC	Power/Other	
C17	VSS	Power/Other	
C18	VCC	Power/Other	
C19	VSS	Power/Other	
C20	VCC	Power/Other	
C21	D4#	Source Synch	Input/Output
C22	VSS	Power/Other	
C23	D7#	Source Synch	Input/Output
C24	D8#	Source Synch	Input/Output
C25	VSS	Power/Other	
C26	D12#	Source Synch	Input/Output
D1	LINT0	Asynch GTL+	Input
D2	BPRI#	Common Clock	Input
D3	VSS	Power/Other	
D4	TCK	TAP	Input
D5	TDO	TAP	Output
D6	VSS	Power/Other	

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
D7	VCC	Power/Other	
D8	VSS	Power/Other	
D9	VCC	Power/Other	
D10	VSS	Power/Other	
D11	VCC	Power/Other	
D12	VSS	Power/Other	
D13	VCC	Power/Other	
D14	VSS	Power/Other	
D15	VCC	Power/Other	
D16	VSS	Power/Other	
D17	VCC	Power/Other	
D18	VSS	Power/Other	
D19	VCC	Power/Other	
D20	VSS	Power/Other	
D21	VSS	Power/Other	
D22	D5#	Source Synch	Input/Output
D23	D13#	Source Synch	Input/Output
D24	VSS	Power/Other	
D25	D15#	Source Synch	Input/Output
D26	D23#	Source Synch	Input/Output
E1	VSS	Power/Other	
E2	DEFER#	Common Clock	Input
E3	HITM#	Common Clock	Input/Output
E4	VSS	Power/Other	
E5	LINT1	Asynch GTL+	Input
E6	TRST#	TAP	Input
E7	VSS	Power/Other	
E8	VCC	Power/Other	
E9	VSS	Power/Other	
E10	VCC	Power/Other	
E11	VSS	Power/Other	
E12	VCC	Power/Other	
E13	VSS	Power/Other	
E14	VCC	Power/Other	
E15	VSS	Power/Other	
E16	VCC	Power/Other	
E17	VSS	Power/Other	
E18	VCC	Power/Other	
E19	VSS	Power/Other	
E20	VCC	Power/Other	
E21	DBI0#	Source Synch	Input/Output

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
E22	DSTBN0#	Source Synch	Input/Output
E23	VSS	Power/Other	
E24	D17#	Source Synch	Input/Output
E25	D21#	Source Synch	Input/Output
E26	VSS	Power/Other	
F1	RS0#	Common Clock	Input
F2	VSS	Power/Other	
F3	HIT#	Common Clock	Input/Output
F4	RS2#	Common Clock	Input
F5	VSS	Power/Other	
F6	GTLREF	Power/Other	Input
F7	TMS	TAP	Input
F8	VSS	Power/Other	
F9	VCC	Power/Other	
F10	VSS	Power/Other	
F11	VCC	Power/Other	
F12	VSS	Power/Other	
F13	VCC	Power/Other	
F14	VSS	Power/Other	
F15	VCC	Power/Other	
F16	VSS	Power/Other	
F17	VCC	Power/Other	
F18	VSS	Power/Other	
F19	VCC	Power/Other	
F20	GTLREF	Power/Other	Input
F21	DSTBP0#	Source Synch	Input/Output
F22	VSS	Power/Other	
F23	D19#	Source Synch	Input/Output
F24	D20#	Source Synch	Input/Output
F25	VSS	Power/Other	
F26	D22#	Source Synch	Input/Output
G1	ADS#	Common Clock	Input/Output
G2	BNR#	Common Clock	Input/Output
G3	VSS	Power/Other	
G4	LOCK#	Common Clock	Input/Output
G5	RS1#	Common Clock	Input
G6	VSS	Power/Other	
G21	VSS	Power/Other	
G22	D10#	Source Synch	Input/Output
G23	D18#	Source Synch	Input/Output
G24	VSS	Power/Other	

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
G25	DBI1#	Source Synch	Input/Output
G26	D25#	Source Synch	Input/Output
H1	VSS	Power/Other	
H2	DRDY#	Common Clock	Input/Output
H3	REQ4#	Source Synch	Input/Output
H4	VSS	Power/Other	
H5	DBSY#	Common Clock	Input/Output
H6	BR0#	Common Clock	Input/Output
H21	D11#	Source Synch	Input/Output
H22	D16#	Source Synch	Input/Output
H23	VSS	Power/Other	
H24	D26#	Source Synch	Input/Output
H25	D31#	Source Synch	Input/Output
H26	VSS	Power/Other	
J1	REQ0#	Source Synch	Input/Output
J2	VSS	Power/Other	
J3	REQ3#	Source Synch	Input/Output
J4	REQ2#	Source Synch	Input/Output
J5	VSS	Power/Other	
J6	TRDY#	Common Clock	Input
J21	D14#	Source Synch	Input/Output
J22	VSS	Power/Other	
J23	DSTBP1#	Source Synch	Input/Output
J24	D29#	Source Synch	Input/Output
J25	VSS	Power/Other	
J26	DP0#	Common Clock	Input/Output
K1	A6#	Source Synch	Input/Output
K2	A3#	Source Synch	Input/Output
K3	VSS	Power/Other	
K4	A4#	Source Synch	Input/Output
K5	REQ1#	Source Synch	Input/Output
K6	VSS	Power/Other	
K21	VSS	Power/Other	
K22	DSTBN1#	Source Synch	Input/Output
K23	D30#	Source Synch	Input/Output
K24	VSS	Power/Other	
K25	DP1#	Common Clock	Input/Output
K26	DP2#	Common Clock	Input/Output
L1	VSS	Power/Other	
L2	A9#	Source Synch	Input/Output
L3	A7#	Source Synch	Input/Output

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
L4	VSS	Power/Other	
L5	ADSTB0#	Source Synch	Input/Output
L6	A5#	Source Synch	Input/Output
L21	D24#	Source Synch	Input/Output
L22	D28#	Source Synch	Input/Output
L23	VSS	Power/Other	
L24	COMP0	Power/Other	Input
L25	DP3#	Common Clock	Input/Output
L26	VSS	Power/Other	
M1	A13#	Source Synch	Input/Output
M2	VSS	Power/Other	
M3	A10#	Source Synch	Input/Output
M4	A11#	Source Synch	Input/Output
M5	VSS	Power/Other	
M6	A8#	Source Synch	Input/Output
M21	D27#	Source Synch	Input/Output
M22	VSS	Power/Other	
M23	D32#	Source Synch	Input/Output
M24	D35#	Source Synch	Input/Output
M25	VSS	Power/Other	
M26	D37#	Source Synch	Input/Output
N1	A12#	Source Synch	Input/Output
N2	A14#	Source Synch	Input/Output
N3	VSS	Power/Other	
N4	A15#	Source Synch	Input/Output
N5	A16#	Source Synch	Input/Output
N6	VSS	Power/Other	
N21	VSS	Power/Other	
N22	D33#	Source Synch	Input/Output
N23	D36#	Source Synch	Input/Output
N24	VSS	Power/Other	
N25	D39#	Source Synch	Input/Output
N26	D38#	Source Synch	Input/Output
P1	COMP1	Power/Other	Input
P2	VSS	Power/Other	
P3	A19#	Source Synch	Input/Output
P4	A20#	Source Synch	Input/Output
P5	VSS	Power/Other	
P6	A24#	Source Synch	Input/Output
P21	D34#	Source Synch	Input/Output
P22	VSS	Power/Other	

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
P23	DSTBP#2	Source Synch	Input/Output
P24	D41#	Source Synch	Input/Output
P25	VSS	Power/Other	
P26	DBI2#	Source Synch	Input/Output
R1	VSS	Power/Other	
R2	A18#	Source Synch	Input/Output
R3	A21#	Source Synch	Input/Output
R4	VSS	Power/Other	
R5	ADSTB1#	Source Synch	Input/Output
R6	A28#	Source Synch	Input/Output
R21	D40#	Source Synch	Input/Output
R22	DSTBN#2	Source Synch	Input/Output
R23	VSS	Power/Other	
R24	D43#	Source Synch	Input/Output
R25	D42#	Source Synch	Input/Output
R26	VSS	Power/Other	
T1	A17#	Source Synch	Input/Output
T2	A22#	Source Synch	Input/Output
T3	VSS	Power/Other	
T4	A26#	Source Synch	Input/Output
T5	A30#	Source Synch	Input/Output
T6	VSS	Power/Other	
T21	VSS	Power/Other	
T22	D46#	Source Synch	Input/Output
T23	D47#	Source Synch	Input/Output
T24	VSS	Power/Other	
T25	D45#	Source Synch	Input/Output
T26	D44#	Source Synch	Input/Output
U1	A23#	Source Synch	Input/Output
U2	VSS	Power/Other	
U3	A25#	Source Synch	Input/Output
U4	A31#	Source Synch	Input/Output
U5	VSS	Power/Other	
U6	TESTHI8	Power/Other	Input
U21	D52#	Source Synch	Input/Output
U22	VSS	Power/Other	
U23	D50#	Source Synch	Input/Output
U24	D49#	Source Synch	Input/Output
U25	VSS	Power/Other	
U26	D48#	Source Synch	Input/Output
V1	VSS	Power/Other	

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
V2	A27#	Source Synch	Input/Output
V3	A32#	Source Synch	Input/Output
V4	VSS	Power/Other	
V5	AP1#	Common Clock	Input/Output
V6	MCERR#	Common Clock	Input/Output
V21	DBI3#	Source Synch	Input/Output
V22	D53#	Source Synch	Input/Output
V23	VSS	Power/Other	
V24	D54#	Source Synch	Input/Output
V25	D51#	Source Synch	Input/Output
V26	VSS	Power/Other	
W1	A29#	Source Synch	Input/Output
W2	A33#	Source Synch	Input/Output
W3	VSS	Power/Other	
W4	TESTHI9	Power/Other	Input
W5	INIT#	Asynch GTL+	Input
W6	VSS	Power/Other	
W21	VSS	Power/Other	
W22	DSTBN3#	Source Synch	Input/Output
W23	DSTBP3#	Source Synch	Input/Output
W24	VSS	Power/Other	
W25	D57#	Source Synch	Input/Output
W26	D55#	Source Synch	Input/Output
Y1	A34#	Source Synch	Input/Output
Y2	VSS	Power/Other	
Y3	TESTHI10	Power/Other	Input
Y4	STPCLK#	Asynch GTL+	Input
Y5	VSS	Power/Other	
Y6	BPM3#	Common Clock	Input/Output
Y21	D60#	Source Synch	Input/Output
Y22	VSS	Power/Other	
Y23	D58#	Source Synch	Input/Output
Y24	D59#	Source Synch	Input/Output
Y25	VSS	Power/Other	
Y26	D56#	Source Synch	Input/Output
AA1	VSS	Power/Other	
AA2	TESTHI1	Power/Other	Input
AA3	BINIT#	Common Clock	Input/Output
AA4	VSS	Power/Other	
AA5	BPM4#	Common Clock	Input/Output
AA6	GTLREF	Power/Other	Input

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
AA7	VSS	Power/Other	
AA8	VCC	Power/Other	
AA9	VSS	Power/Other	
AA10	VCC	Power/Other	
AA11	VSS	Power/Other	
AA12	VCC	Power/Other	
AA13	VSS	Power/Other	
AA14	VCC	Power/Other	
AA15	VSS	Power/Other	
AA16	VCC	Power/Other	
AA17	VSS	Power/Other	
AA18	VCC	Power/Other	
AA19	VSS	Power/Other	
AA20	TESTHI6	Power/Other	Input
AA21	GTLREF	Power/Other	Input
AA22	D62#	Source Synch	Input/Output
AA23	VSS	Power/Other	
AA24	D63#	Source Synch	Input/Output
AA25	D61#	Source Synch	Input/Output
AA26	VSS	Power/Other	
AB1	A35#	Source Synch	Input/Output
AB2	RSP#	Common Clock	Input
AB3	VSS	Power/Other	
AB4	BPM5#	Common Clock	Input/Output
AB5	BPM1#	Common Clock	Input/Output
AB6	VSS	Power/Other	
AB7	VCC	Power/Other	
AB8	VSS	Power/Other	
AB9	VCC	Power/Other	
AB10	VSS	Power/Other	
AB11	VCC	Power/Other	
AB12	VSS	Power/Other	
AB13	VCC	Power/Other	
AB14	VSS	Power/Other	
AB15	VCC	Power/Other	
AB16	VSS	Power/Other	
AB17	VCC	Power/Other	
AB18	VSS	Power/Other	
AB19	VCC	Power/Other	
AB20	VSS	Power/Other	
AB21	VSS	Power/Other	

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
AB22	TESTHI7	Power/Other	Input
AB23	PWRGOOD	Power/Other	Input
AB24	VSS	Power/Other	
AB25	RESET#	Common Clock	Input
AB26	SLP#	Asynch GTL+	Input
AC1	AP0#	Common Clock	Input/Output
AC2	VSS	Power/Other	
AC3	IERR#	Asynch GTL+	Output
AC4	BPM2#	Common Clock	Input/Output
AC5	VSS	Power/Other	
AC6	BPM0#	Common Clock	Input/Output
AC7	VSS	Power/Other	
AC8	VCC	Power/Other	
AC9	VSS	Power/Other	
AC10	VCC	Power/Other	
AC11	VSS	Power/Other	
AC12	VCC	Power/Other	
AC13	VSS	Power/Other	
AC14	VCC	Power/Other	
AC15	VSS	Power/Other	
AC16	VCC	Power/Other	
AC17	VSS	Power/Other	
AC18	VCC	Power/Other	
AC19	VSS	Power/Other	
AC20	TESTHI3	Power/Other	Input
AC21	TESTHI2	Power/Other	Input
AC22	VSS	Power/Other	
AC23	TESTHI5	Power/Other	Input
AC24	TESTHI4	Power/Other	Input
AC25	VSS	Power/Other	
AC26	ITP_CLK0	TAP	Input
AD1	BOOTSELECT	Power/Other	Input
AD2	VIDPWRGD	Power/Other	Input
AD3	VID5	Power/Other	Output
AD4	VSS	Power/Other	
AD5	BSEL1	Power/Other	Output
AD6	BSEL0	Power/Other	Output
AD7	VCC	Power/Other	
AD8	VSS	Power/Other	
AD9	VCC	Power/Other	
AD10	VSS	Power/Other	

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
AD11	VCC	Power/Other	
AD12	VSS	Power/Other	
AD13	VCC	Power/Other	
AD14	VSS	Power/Other	
AD15	VCC	Power/Other	
AD16	VSS	Power/Other	
AD17	VCC	Power/Other	
AD18	VSS	Power/Other	
AD19	VCC	Power/Other	
AD20	VCCIOPLL	Power/Other	
AD21	VSS	Power/Other	
AD22	VSSA	Power/Other	
AD23	VSS	Power/Other	
AD24	TESTHI0	Power/Other	Input
AD25	TESTHI12	Power/Other	Input
AD26	ITP_CLK1	TAP	Input
AE1	VID4	Power/Other	Output
AE2	VID3	Power/Other	Output
AE3	VID2	Power/Other	Output
AE4	VID1	Power/Other	Output
AE5	VID0	Power/Other	Output
AE6	VCC	Power/Other	
AE7	VSS	Power/Other	
AE8	VCC	Power/Other	
AE9	VSS	Power/Other	
AE10	VCC	Power/Other	
AE11	VSS	Power/Other	
AE12	VCC	Power/Other	
AE13	VSS	Power/Other	
AE14	VCC	Power/Other	
AE15	VSS	Power/Other	
AE16	VCC	Power/Other	
AE17	VSS	Power/Other	
AE18	VCC	Power/Other	
AE19	VSS	Power/Other	
AE20	VCC	Power/Other	
AE21	RESERVED		
AE22	VSS	Power/Other	
AE23	VCCA	Power/Other	
AE24	VSS	Power/Other	
AE25	DBR#	Power/Other	Output

Table 4-2. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
AE26	OPTIMIZED/ COMPAT#	Power/Other	Input
AF1	VSS	Power/Other	
AF2	VCC	Power/Other	
AF3	VCCVIDLB	Power/Other	Input
AF4	VCCVID	Power/Other	Input
AF5	VCC	Power/Other	
AF6	VSS	Power/Other	
AF7	VCC	Power/Other	
AF8	VSS	Power/Other	
AF9	VCC	Power/Other	
AF10	VSS	Power/Other	
AF11	VCC	Power/Other	
AF12	VSS	Power/Other	
AF13	VCC	Power/Other	
AF14	VSS	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VCC	Power/Other	
AF18	VSS	Power/Other	
AF19	VCC	Power/Other	
AF20	VSS	Power/Other	
AF21	VCC	Power/Other	
AF22	BCLK0	Bus Clock	Input
AF23	BCLK1	Bus Clock	Input
AF24	RESERVED		
AF25	RESERVED		
AF26	SKTOCC#	Power/Other	Output

4.2 Alphabetical Signals Reference

Table 4-3. Signal Description (Sheet 1 of 8)

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Celeron® D processor FSB. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration. See Section 6.1 for more details.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** — **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB0# A[35:17]# — ADSTB1#
AP[1:0]#	Input/ Output	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Celeron D processor FSB agents. The following table defines the coverage model of these signals. **Request Signals** — **Subphase 1** — **Subphase 2** A[35:24]# — AP0# — AP1# A[23:3]# — AP1# — AP0# REQ[4:0]# — AP1# — AP0#
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the FSB frequency. All processor FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.

Table 4-3. Signal Description (Sheet 2 of 8)

Name	Type	Description
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor FSB agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the FSB and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BOOTSELECT	Input	This input is required to determine whether the processor is installed in a platform that supports the Celeron D processor. The Celeron D processor will not operate if this pin is low. This input has a weak internal pull-up.
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all Celeron D processor FSB agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Refer to the applicable chipset platform design guide for more detailed information. These signals do not have on-die termination. Refer to Section 2.5, and the applicable chipset platform design guide for termination requirements.
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor FSB. It must connect the appropriate pins of all processor FSB agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by de-asserting BPRI#.
BR0#	Input/ Output	BR0# (Bus Request 0) drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0. This signal does not have on-die termination and must be terminated.
BSEL[1:0]	Output	The BCLK[1:0] frequency select signals BSEL[1:0] are used to select the processor input clock frequency. Table 2-6 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. For more information about these pins, including termination recommendations refer to Section 2.9 and the appropriate platform design guidelines.
COMP[1:0]	Analog	COMP[1:0] must be terminated on the system board using precision resistors. Refer to the applicable chipset platform design guide for details on implementation.

Table 4-3. Signal Description (Sheet 3 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>D[63:0]#</td><td>Input/ Output</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor FSB agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#.

Quad-Pumped Signal Groups

<table>
<tr><th>Data Group</th><th>DSTBN#/ DSTBP#</th><th>DBI#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>

Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBI[3:0]#</td><td>Input/ Output</td><td>DBI[3:0]# (Data Bus Invert) are source synchronous and indicate the polarity of the D[63:0]# signals.The DBI[3:0]# signals are activated when the data on the data bus is inverted. If more than half the data bits, within a 16-bit group, would have been asserted electrically low, the bus agent may invert the data bus signals for that particular sub-phase for that 16-bit group.

DBI[3:0] Assignment To Data Bus

<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DBI3#</td><td>D[63:48]#</td></tr>
<tr><td>DBI2#</td><td>D[47:32]#</td></tr>
<tr><td>DBI1#</td><td>D[31:16]#</td></tr>
<tr><td>DBI0#</td><td>D[15:0]#</td></tr>
</table>
</td></tr>
<tr><td>DBR#</td><td>Output</td><td>DBR# (Debug Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.</td></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor FSB to indicate that the data bus is in use. The data bus is released after DBSY# is de-asserted. This signal must connect the appropriate pins on all processor FSB agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor FSB agents.</td></tr>
<tr><td>DP[3:0]#</td><td>Input/ Output</td><td>DP[3:0]# (Data Parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Celeron D processor FSB agents.</td></tr>
</table>

Table 4-3. Signal Description (Sheet 4 of 8)

Name	Type	Description
DRDY#	Input/ Output	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be de-asserted to insert idle clocks. This signal must connect the appropriate pins of all processor FSB agents.
DSTBN[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. **Signals** — **Associated Strobe** D[15:0]#, DBI0# — DSTBN0# D[31:16]#, DBI1# — DSTBN1# D[47:32]#, DBI2# — DSTBN2# D[63:48]#, DBI3# — DSTBN3#
DSTBP[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. **Signals** — **Associated Strobe** D[15:0]#, DBI0# — DSTBP0# D[31:16]#, DBI1# — DSTBP1# D[47:32]#, DBI2# — DSTBP2# D[63:48]#, DBI3# — DSTBP3#
FERR#/PBE#	Output	FERR#/PBE# (Floating Point Error/Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to volume 3 of the *Intel Architecture Software Developer's Manual* and the *Intel Processor Identification and the CPUID Instruction* application note.
GTLREF	Input	GTLREF determines the signal reference level for GTL+ input pins. GTLREF is used by the GTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the applicable chipset platform design guide for more information.
HIT# HITM#	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#. This signal does not have on-die termination. Refer to Section 2.5 for termination requirements.

Table 4-3. Signal Description (Sheet 5 of 8)

Name	Type	Description
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is de-asserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor FSB, it will wait until it observes LOCK# de-asserted. This enables symmetric agents to retain ownership of the processor FSB throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor FSB agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.

Table 4-3. Signal Description (Sheet 6 of 8)

Name	Type	Description
OPTIMIZED/ COMPAT#	Input	This is an input to the processor to determine if the processor is in an optimized platform or a compatible platform. This input has a weak internal pull-up. A compatible platform is one that is designed for a previous generation processor but has some level of compatibility with the Celeron D processor. An optimized platform is one designed specifically for the Celeron D processor; however, it may have some level of compatibility with previous generation processors.
PROCHOT#	Input/ Output	As an output, PROCHOT# (Processor Hot) goes active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system activates the TCC, if enabled. The TCC remains active until the system de-asserts PROCHOT#.
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification and be followed by a 1 ms to 10 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request) must connect the appropriate pins of all processor FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least 1 ms after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, all FSB agents will de-assert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 6.1. This signal does not have on-die termination and must be terminated on the system board.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor FSB agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor FSB agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.

Table 4-3. Signal Description (Sheet 7 of 8)

Name	Type	Description
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, and de-assertion of SLP#. If SLP# is de-asserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the de-assertion of RESET#, the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is de-asserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12:0]	Input	TESTHI[12:0] must be connected to a V_{CC} power source through a resistor for proper processor operation. See Section 2.5 for more details.
THERMDA	Other	Thermal Diode Anode. See Section 5.2.6.
THERMDC	Other	Thermal Diode Cathode. See Section 5.2.6.
THERMTRIP#	Output	In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature approximately 20 °C above the maximum T_C. Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (V_{CC}) must be removed following the assertion of THERMTRIP#. Driving of the THERMTRIP# signal is enabled within 10 µs of the assertion of PWRGOOD and is disabled on de-assertion of PWRGOOD. Once activated, THERMTRIP# remains latched until PWRGOOD is de-asserted. While the de-assertion of the PWRGOOD signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 µs of the assertion of PWRGOOD.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all FSB agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.

Table 4-3. Signal Description (Sheet 8 of 8)

Name	Type	Description
VCC	Input	VCC are the power pins for the processor. The voltage supplied to these pins is determined by the VID[5:0] pins.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the applicable chipset platform design guide for complete implementation details.
VCCIOPLL	Input	VCCIOPLL provides isolated power for internal processor FSB PLLs. Follow the guidelines for VCCA, and refer to the applicable chipset platform design guide for complete implementation details.
VCC_SENSE	Output	VCC_SENSE is an isolated low impedance connection to processor core power (V_{CC}). It can be used to sense or measure voltage near the silicon with little noise.
VCCVID	Input	1.2 V is required to be supplied to the VCCVID pin if the platform is going to support the Celeron D processor. Refer to the applicable chipset platform design guide for more information.
VCCVIDLB	Input	1.2 V is required to be supplied to the VCCVIDLB pin if the platform is going to support the Celeron D processor. Refer to the applicable chipset platform design guide for more information.
VID[5:0]	Output	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). These are open drain signals that are driven by the Celeron D processor and must be pulled up to 3.3 V with 1 kΩ 5% resistors. The voltage supply for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 2-2 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
VIDPWRGD	Input	The processor requires this input to determine that the VCCVID and VCCVIDLB voltages are stable and within specification.
VSS	Input	VSS are the ground pins for the processor and should be connected to the system ground plane.
VSSA	Input	VSSA is the isolated ground for internal PLLs.
VSS_SENSE	Output	VSS_SENSE is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise.

§



5 Thermal Specifications and Design Considerations

5.1 Processor Thermal Specifications

The Celeron D processor requires a thermal solution to maintain temperatures within operating limits as set forth in Section 5.1.1. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor Integrated Heat Spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

For more information on designing a component level thermal solution, refer to the applicable thermal design guide.

Note: The boxed processor will ship with a component thermal solution. Refer to Chapter 7 for details on the boxed processor.

5.1.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum case temperature (T_C) specifications when operating at or below the Thermal Design Power (TDP) value listed per frequency in Table 5-1. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, refer to the appropriate processor thermal design guidelines.

The Celeron D processor introduces a new methodology for managing processor temperatures through fan speed control. Selection of the appropriate fan speed will be based on the temperature reported by the processor's Thermal Diode. The fan must be turned on to full speed when T_{DIODE} is at or above $T_{CONTROL}$ and T_C must be maintained at or below T_C (max) as defined by the processor thermal specifications in Table 5-1. The fan speed may be lowered when the processor temperature can be maintained below $T_{CONTROL}$ as measured by the thermal diode. Systems implementing fan speed control must be designed to read temperature values from the diode and $T_{CONTROL}$ register and take appropriate action. Systems that do not alter the fan speed (always at full speed) only need to guarantee the case temperature meets specifications in Table 5-1.

The case temperature is defined at the geometric top center of the processor IHS. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained periods of time. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 5-1 instead of the maximum processor

power consumption. The Thermal Monitor feature is intended to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 5.2. **In all cases, the Thermal Monitor feature must be enabled for the processor to remain within specification.**

Table 5-1. Processor Thermal Specifications

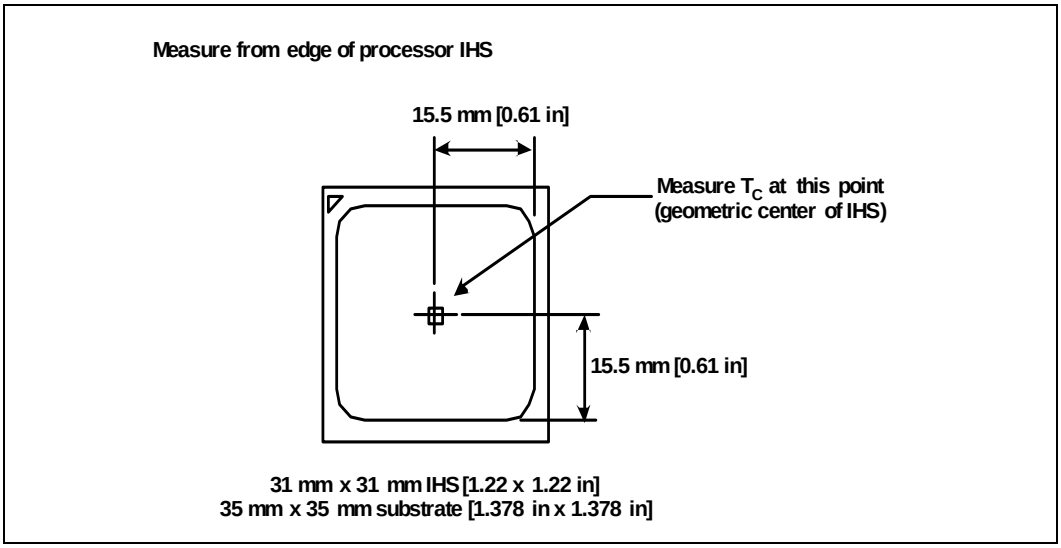
Processor Number	Core Frequency (GHz)	Thermal Design Power (W)	Minimum T_C (°C)	Maximum T_C (°C)	Notes[1,2]
350	3.20	73	5	67	—
345	3.06	73	5	67	—
340	2.93	73	5	67	—
335	2.80	73	5	67	—
330	2.66	73	5	67	—
325	2.53	73	5	67	—
320	2.40	73	5	67	—

NOTES:
1. Thermal Design Power (TDP) should be used for processor thermal solution design targets. The TDP is not the maximum power that the processor can dissipate.
2. This table shows the maximum TDP for a given frequency range. Individual processors may have a lower TDP.

5.1.2 Thermal Metrology

The maximum and minimum case temperatures (T_C) are specified in Table 5-1. These temperature specifications are meant to help ensure proper operation of the processor. Figure 5-1 illustrates where Intel recommends T_C thermal measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the applicable thermal design guide.

Figure 5-1. Case Temperature (T_C) Measurement Location



5.2 Processor Thermal Features

5.2.1 Thermal Monitor

The Thermal Monitor feature helps control the processor temperature by activating the TCC when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption as needed by modulating (starting and stopping) the internal processor core clocks. **The Thermal Monitor feature must be enabled for the processor to be operating within specifications.** The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor feature is enabled, and a high temperature situation exists (i.e., TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30–50%). Clocks often will not be off for more than 3.0 microseconds when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may result in a T_C that exceeds the specified maximum temperature and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the applicable thermal design guide for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

5.2.2 On-Demand Mode

The Celeron D processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as "On-Demand" mode and is distinct from the Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems using the Celeron D processor must not rely on software usage of this mechanism to limit the processor temperature.

If bit 4 of the ACPI P_CNT Control Register (located in the processor IA32_THERM_CONTROL MSR) is written to a '1', the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI P_CNT Control Register. In On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5%

increments. On-Demand mode may be used in conjunction with the Thermal Monitor. If the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

5.2.3 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If the Thermal Monitor is enabled (note that the Thermal Monitor must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. Refer to the *Intel Architecture Software Developer's Manuals* for specific register and programming details.

The Celeron D processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from over-temperature situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

One application is the thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR can cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its Thermal Design Power. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss. Refer to the applicable chipset platform design guide and the applicable VRD design guide for details on implementing the bi-directional PROCHOT# feature.

5.2.4 THERMTRIP# Signal Pin

Regardless of whether or not the Thermal Monitor feature is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Table 4-3). At this point, the FSB signal THERMTRIP# will go active and stay active as described in Table 4-3. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

5.2.5 $T_{CONTROL}$ and Fan Speed Reduction (Optional)

$T_{CONTROL}$ and Fan Speed Reduction are not requirements for the Celeron D processor on 90 nm process and in the 478-pin package, but are provided as options for platforms that can use these features. $T_{CONTROL}$ is part of the temperature specification that defines temperature for system fan speed management. The BIOS reads the $T_{CONTROL}$ value once and configures the fan control chip appropriately. The value for $T_{CONTROL}$ will be set during manufacturing and is unique for each processor. The $T_{CONTROL}$ temperature for a given processor can be obtained by reading the IA32_TEMPERATURE_TARGET MSR in the processor and is in hexadecimal format.

The value of $T_{CONTROL}$ (read from IA32_TEMPERATURE_TARGET MSR) can vary from 00 h to 1E h (0 to 30 °C). The $T_{CONTROL}$ read from the IA32_TEMPERATURE_TARGET MSR needs to be added to a base value of 50 °C to get the final value for comparison with Thermal Diode temperature (T_{DIODE}). $T_{CONTROL}$ plus the base value of 50 °C is compared to the temperature reported by T_{DIODE}. When the T_{DIODE} temperature is below $T_{CONTROL}$, fan speed can be at minimum. As T_{DIODE} approaches $T_{CONTROL}$ plus the base value of 50 °C, fan speed should be increased in an effort to maintain T_{DIODE} at/below $T_{CONTROL}$ plus the base value of 50 °C. For platforms that support this feature, the processor $T_{C\text{-}MAX}$ specification must be within guidelines, as defined by the processor thermal specifications in Table 5-1. For 845G/x chipset platforms that were not designed to read IA32_TEMPERATURE_TARGET MSR, the processor must be kept within the $T_{C\text{-}MAX}$ specification.

5.2.6 Thermal Diode

The processor incorporates an on-die thermal diode. A thermal sensor located on the system board may monitor the die temperature of the processor for thermal management/long term die temperature change purposes. Table 5-2 and Table 5-3 provide the diode parameter and interface specifications. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 5-2. Thermal Diode Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	11	—	187	uA	1
n	Diode Ideality Factor	1.0083	1.011	1.0137	—	2,3,4
R_T	Series Resistance	3.242	3.33	3.594	Ω	2,3,5

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized at 75 °C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:
$$I_{FW} = I_S * (e^{qV_D/nkT} - 1)$$
where I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, R_T, is provided to allow for a more accurate measurement of the junction temperature. R_T, as defined, includes the pins of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. R_T can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:
$$T_{error} = [R_T * (N-1) * I_{FWmin}] / [nk/q * \ln N]$$
where T_{error} = sensor temperature error, N = sensor current ratio, k = Boltzmann Constant, q = electronic charge.

Table 5-3. Thermal Diode Interface

Pin Name	Pin Number	Pin Description
THERMDA	B3	diode anode
THERMDC	C4	diode cathode

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6 Features

This chapter contains power-on configuration options and clock control/low power state descriptions.

6.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The Celeron D processor samples the hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, refer to Table 6-1.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor; for reset purposes, the processor does not distinguish between a "warm" reset and a "power-on" reset.

Table 6-1. Power-On Configuration Option Pins

Configuration Option	Pin[1,2]
Output tristate	SMI#
Execute BIST	INIT#
In Order Queue pipelining (set IOQ depth to 1)	A7#
Disable MCERR# observation	A9#
Disable BINIT# observation	A10#
APIC Cluster ID (0-3)	A[12:11]#
Disable bus parking	A15#
Symmetric agent arbitration ID	BR0#
RESERVED	A[6:3]#, A8#, A[14:13]#, A[16:35]#

NOTES:
1. Asserting this signal during RESET# will select the corresponding option.
2. Address pins not identified in this table as configuration options should not be asserted during RESET#.

6.2 Clock Control and Low Power States

The processor allows the use of AutoHALT, Stop-Grant, and Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 6-1 for a visual representation of the processor low power states.

6.2.1 Normal State—State 1

This is the normal operating state for the processor.

6.2.2 AutoHALT Powerdown State—State 2

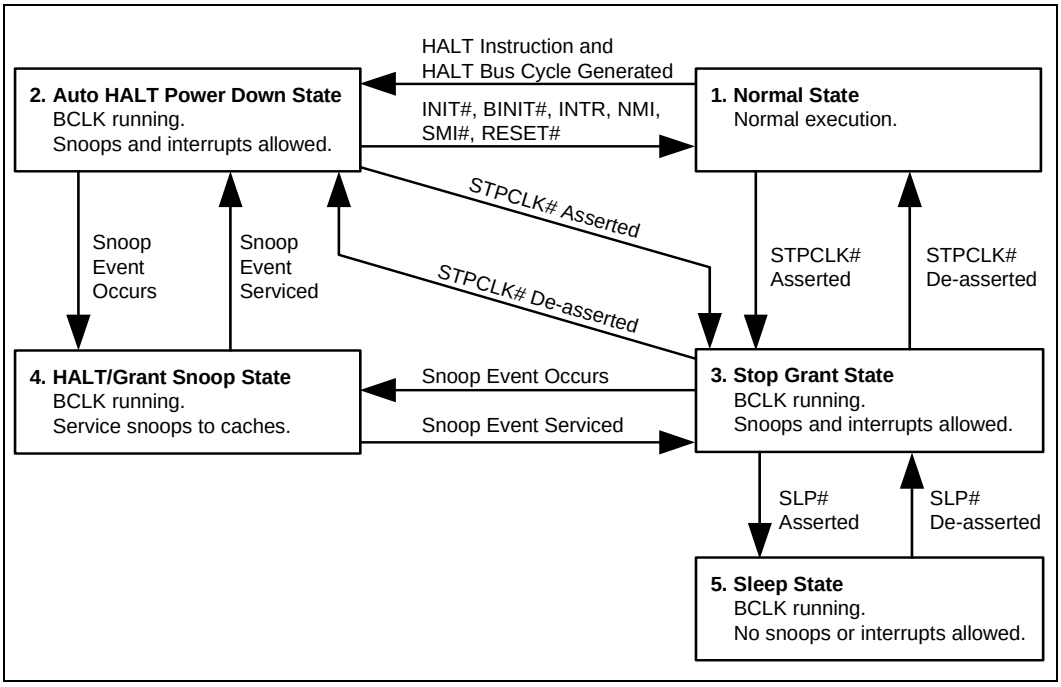
AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system de-asserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Power Down state, the processor will process FSB snoops and interrupts.

Figure 6-1. Stop Clock State Machine



6.2.3 Stop-Grant State—State 3

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle.

Since the GTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to V_{CC}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.

BINIT# will not be serviced while the processor is in the Stop-Grant state. The event is latched and can be serviced by software upon exit from the Stop Grant state.

RESET# causes the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal. When re-entering the Stop Grant state from the Sleep state, STPCLK# should only be de-asserted one or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state occurs when the processor detects a snoop on the FSB (see Section 6.2.4). A transition to the Sleep state (see Section 6.2.5) occurs with the assertion of the SLP# signal.

While in the Stop-Grant state, SMI#, INIT#, BINIT# and LINT[1:0] are latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor processes snoops on the FSB and latches interrupts delivered on the FSB.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# is asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

6.2.4 HALT/Grant Snoop State—State 4

The processor responds to snoop or interrupt transactions on the FSB while in Stop-Grant state or in AutoHALT Power Down state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor stays in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor returns to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

6.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the processor will enter the Sleep state upon the assertion of the SLP# signal. The SLP# pin should only be asserted when the processor is in the Stop Grant state. SLP# assertions while the processor is not in the Stop Grant state is out of specification and may result in erroneous processor operation.

Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the FSB while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be de-asserted immediately after RESET# is asserted to ensure the processor correctly executes the reset sequence.

Once in the Sleep state, the SLP# pin must be de-asserted if another asynchronous FSB event needs to occur. The SLP# pin has a minimum assertion of one BCLK period.

When the processor is in the Sleep state, it does not respond to interrupts or snoop transactions.

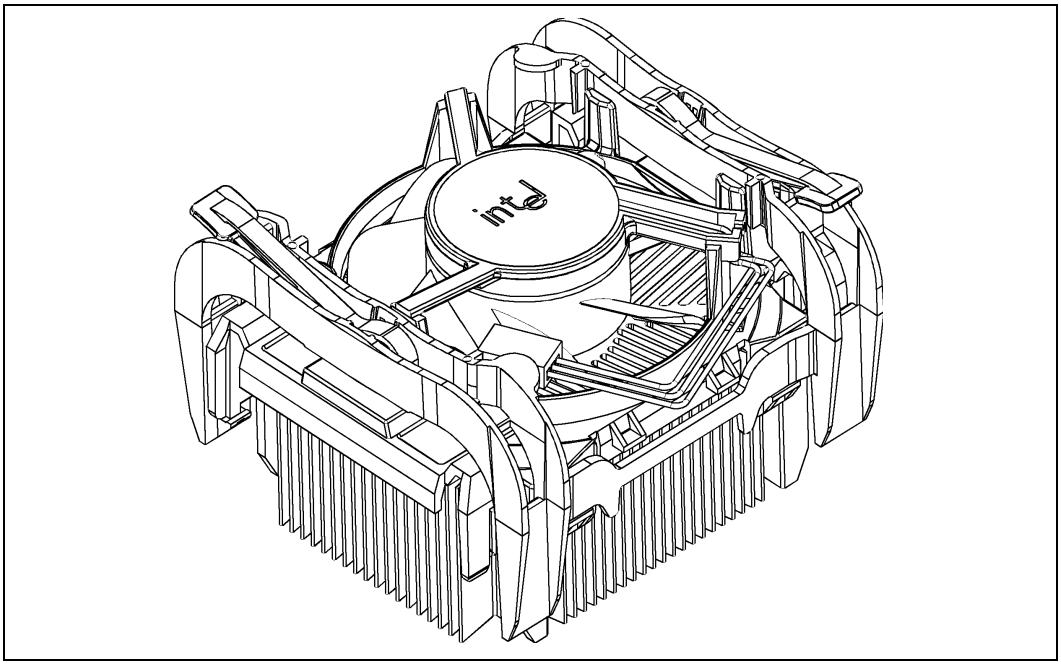
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7 Boxed Processor Specifications

The Celeron D processor is also offered as a boxed Intel processor. Boxed Intel processors are intended for system integrators who build systems from baseboards and standard components. The boxed Celeron D processor will be supplied with a cooling solution. This chapter documents baseboard and system requirements for the cooling solution that will be supplied with the boxed Celeron D processor. This chapter is particularly important for OEMs that manufacture baseboards for system integrators. Unless otherwise noted, all figures in this chapter are dimensioned in millimeters and inches [in brackets]. Figure 7-1 shows a mechanical representation of a boxed Celeron D processor.

- Drawings in this section reflect only the specifications on the boxed Intel processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designer's responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platform and chassis. Refer to the *Intel® Pentium 4 Processor on 90 nm Process Thermal Design Guidelines* for further guidance. Contact your local Intel Sales Representative for this document.

Figure 7-1. Mechanical Representation of the Boxed Intel® Celeron® D Processor



NOTE: The airflow of the fan heatsink is into the center and out of the sides of the fan heatsink.

7.1 Mechanical Specifications

7.1.1 Boxed Processor Cooling Solution Dimensions

This section documents the mechanical specifications of the boxed Celeron D processor. The boxed processor will be shipped with an unattached fan heatsink. Figure 7-1 shows a mechanical representation of the boxed Celeron D processor.

Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor with assembled fan heatsink are shown in Figure 7-2 (Side Views), and Figure 7-3 (Top View). The airspace requirements for the boxed processor fan heatsink must also be incorporated into new baseboard and system designs. Airspace requirements are shown in Figure 7-6 and Figure 7-7. Note that some figures have centerlines shown (marked with alphabetic designations) to clarify relative dimensioning.

Figure 7-2. Requirements for the Boxed Processor (Side View)

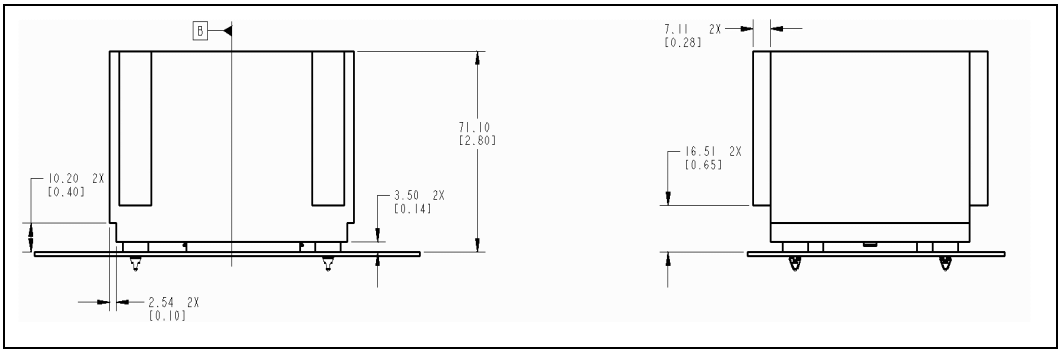
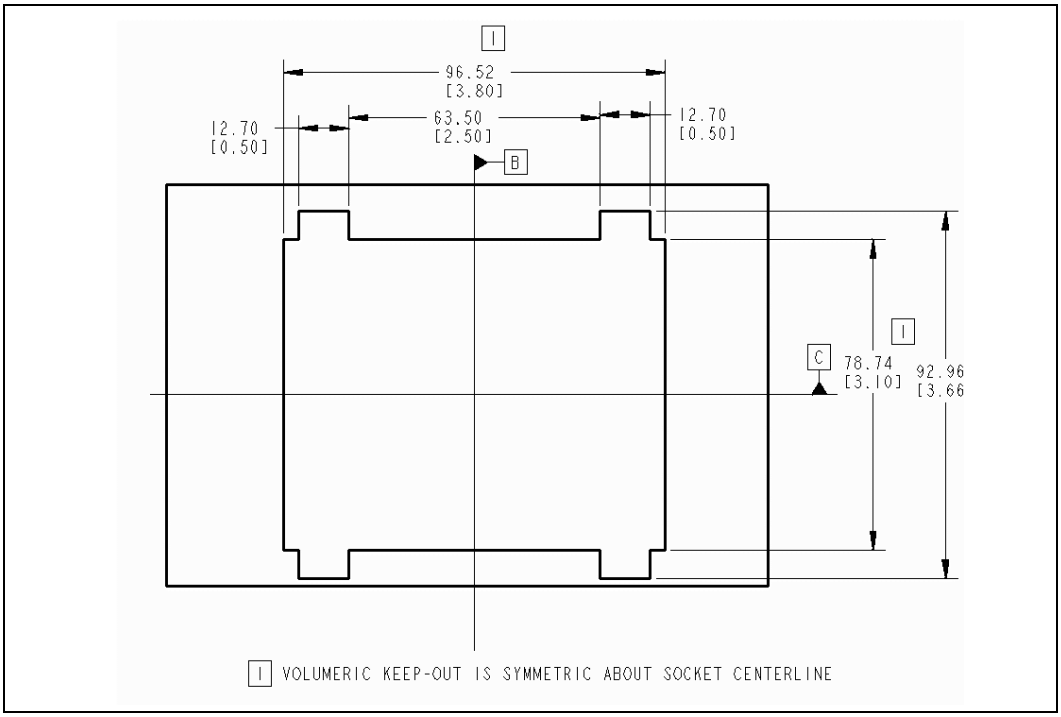


Figure 7-3. Space Requirements for the Boxed Processor (Top View)



7.1.2 Boxed Processor Fan Heatsink Weight

The boxed processor fan heatsink will not weigh more than 450 grams. See Chapter 5 and the *Intel® Pentium 4 Processor on 90 nm Process Thermal Design Guidelines* for details on the processor weight and heatsink requirements.

Note: The processor retention mechanism based on the Intel reference design should be used, to ensure compatibility with the heatsink attach clip assembly and the boxed processor thermal solution. The heatsink attach clip assembly is latched to the retention tab features at each corner of the retention mechanism.

The target load applied by the clips to the processor heat spreader for Intel's reference design is 75 ±15 lbf (maximum load is constrained by the package load capability). It is normal to observe a bow or bend in the board due to this compressive load on the processor package and the socket. The level of bow or bend depends on the motherboard material properties and component layout. Any additional board stiffening devices (such as plates) are not necessary and should not be used along with the reference mechanical components and boxed processor. Using such devices increases the compressive load on the processor package and socket, likely beyond the maximum load that is specified for those components. See the *Intel® Pentium 4 Processor on 90 nm Process Thermal Design Guidelines* for details on the Intel reference design.

Chassis that have adequate clearance between the motherboard and chassis wall (minimum 0.250 inch) should be selected to ensure the board's underside bend does not contact the chassis.

7.1.3 Boxed Processor Retention Mechanism and Heatsink Attach Clip Assembly

The boxed processor thermal solution requires a processor retention mechanism and a heatsink attach clip assembly, to secure the processor and fan heatsink in the baseboard socket. The boxed processor will not ship with retention mechanisms but will ship with the heatsink attach clip assembly. Baseboards designed for use by system integrators should include the retention mechanism that supports the boxed Celeron D processor. Baseboard documentation should include appropriate retention mechanism installation instructions.

7.2 Electrical Requirements

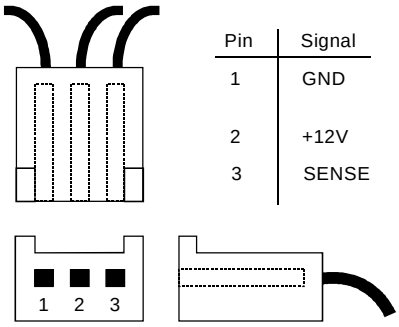
7.2.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable will be shipped with the boxed processor to draw power from a power header on the baseboard. The power cable connector and pinout are shown in Figure 7-4. Baseboards must provide a matched power header to support the boxed processor. Table 7-1 contains specifications for the input and output signals at the fan heatsink connector. The fan heatsink outputs a SENSE signal, which is an open-collector output that pulses at a rate of 2 pulses per fan revolution. A baseboard pull-up resistor provides V_{OH} to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

Note: The motherboard must supply a constant +12 V to the processor's power header to ensure proper operation of the variable speed fan for the boxed processor.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. Figure 7-7 shows the location of the fan power connector relative to the processor socket. The baseboard power header should be positioned within 4.33 inches from the center of the processor socket.

Figure 7-4. Boxed Processor Fan Heatsink Power Cable Connector Description



Pin	Signal
1	GND
2	+12V
3	SENSE

Straight square pin, 3-pin terminal housing with polarizing ribs and friction locking ramp.

0.100" pin pitch, 0.025" square pin width.

Waldom*/Molex* P/N 22-01-3037 or equivalent.

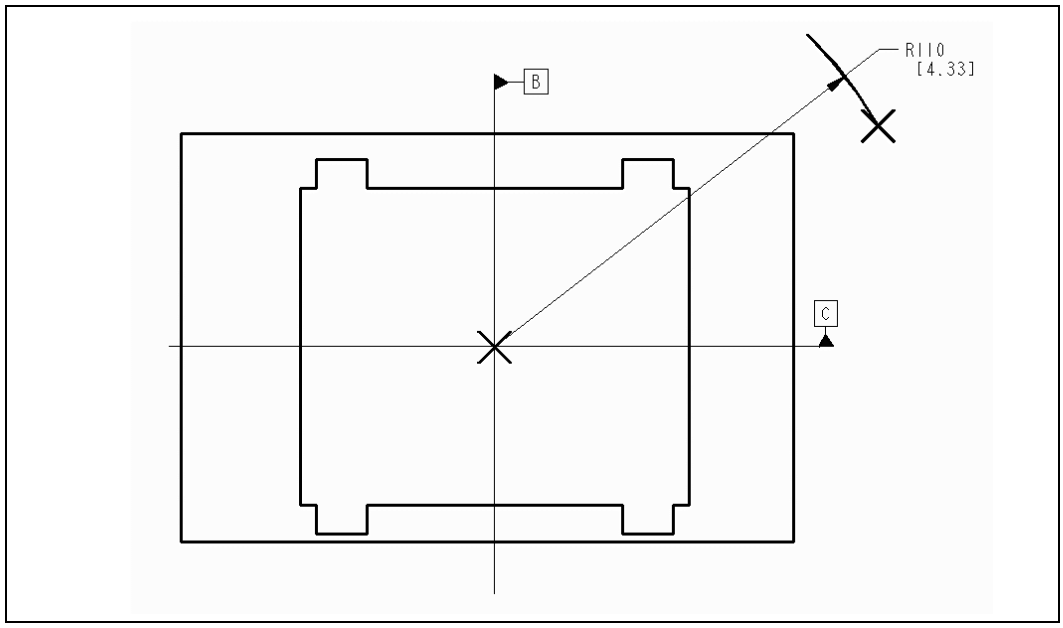
Match with straight pin, friction lock header on motherboard Waldom/Molex P/N 22-23-2031, AMP* P/N 640456-3, or equivalent.

Table 7-1. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max	Unit	Notes
+12 V: 12 volt fan power supply	10.2	12	13.8	V	—
IC: Fan current draw	—	—	740	mA	—
SENSE: SENSE frequency	—	2	—	pulses per fan revolution	1

NOTES:
1. Baseboard should pull this pin up to 5 V with a resistor.

Figure 7-5. Baseboard Power Header Placement Relative to Processor Socket



7.3 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution used by the boxed processor.

7.3.1 Boxed Processor Cooling Requirements

The boxed processor may be directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is found in Chapter 5 of this document. The boxed processor fan heatsink is able to keep the processor temperature within the specifications (see Table 5-1) in chassis that provide good thermal management. For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink is unimpeded. Airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 7-6 and Figure 7-7 illustrate an acceptable airspace clearance for the fan heatsink. The air temperature entering the fan is required to be at or below 38 °C. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

Figure 7-6. Boxed Processor Fan Heatsink Airspace Keepout Requirements (Side 1 View)

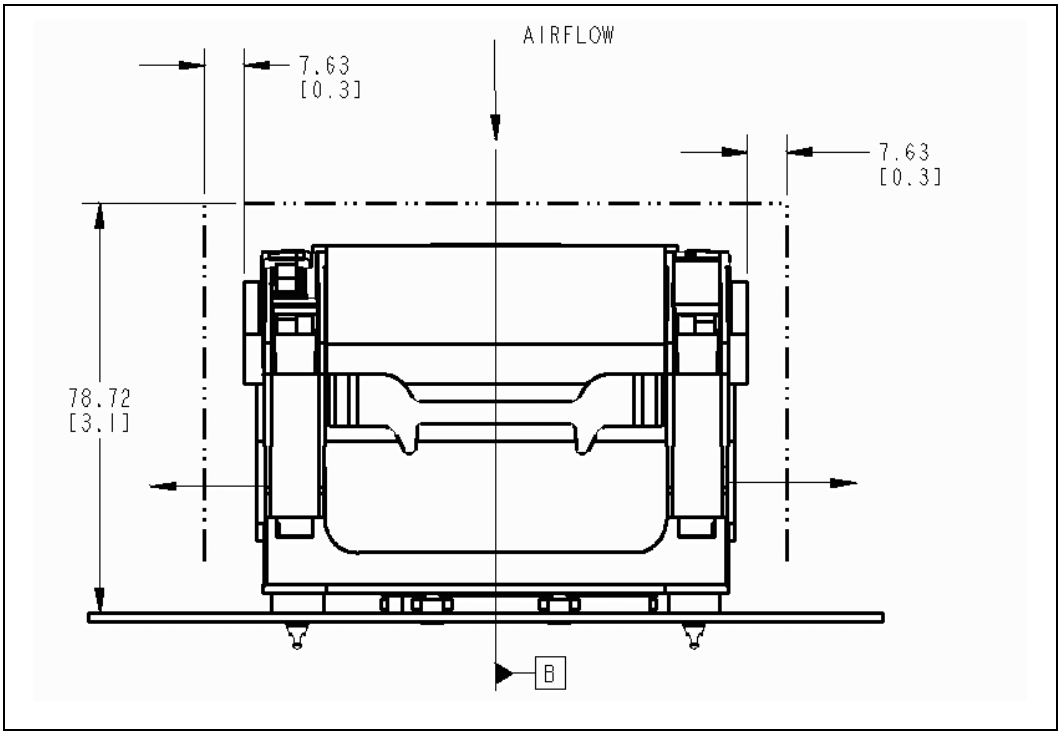
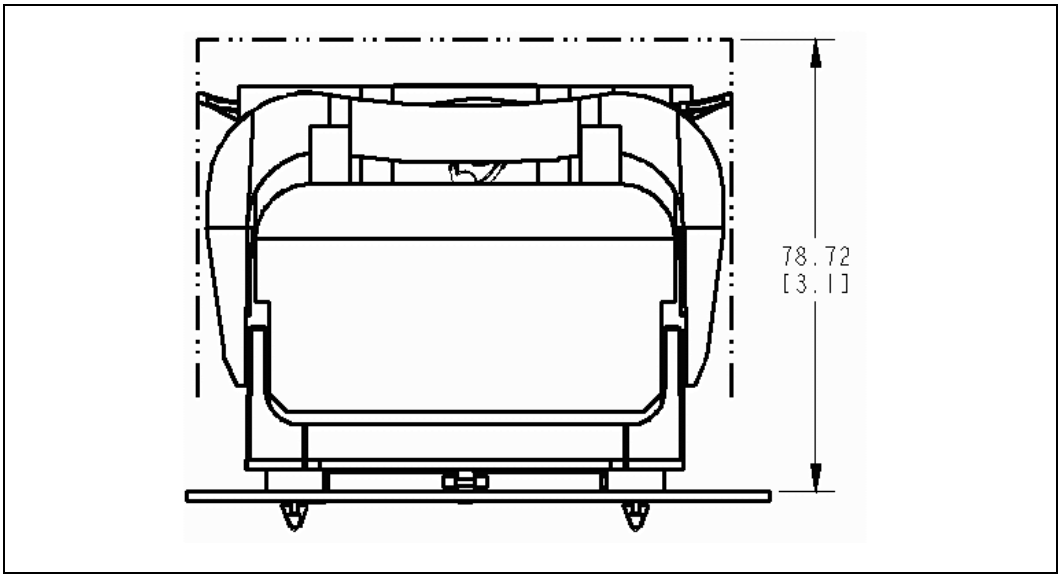


Figure 7-7. Boxed Processor Fan Heatsink Airspace Keepout Requirements (Side 2 View)



7.3.2 Variable Speed Fan

The boxed processor fan operates at different speeds over a short range of internal chassis temperatures. This allows the processor fan to operate at a lower speed and noise level, while internal chassis temperatures are low. If internal chassis temperature increases beyond a lower set point, the fan speed will rise linearly with the internal temperature until the higher set point is reached. At that point, the fan speed is at its maximum. As fan speed increases, so does fan noise levels. Systems should be designed to provide adequate air around the boxed processor fan heatsink that remains below the lower set point. These set points, represented in Figure 7-8 and Table 7-2, can vary by a few degrees from fan heatsink to fan heatsink. The internal chassis temperature should be kept below 38 ºC. Meeting the processor's temperature specification (see Chapter 5) is the responsibility of the system integrator.

Note: The motherboard must supply a constant +12 V to the processor's power header to ensure proper operation of the variable speed fan for the boxed processor (refer to Table 7-1 for the specific requirements).

Figure 7-8. Boxed Processor Fan Heatsink Set Points

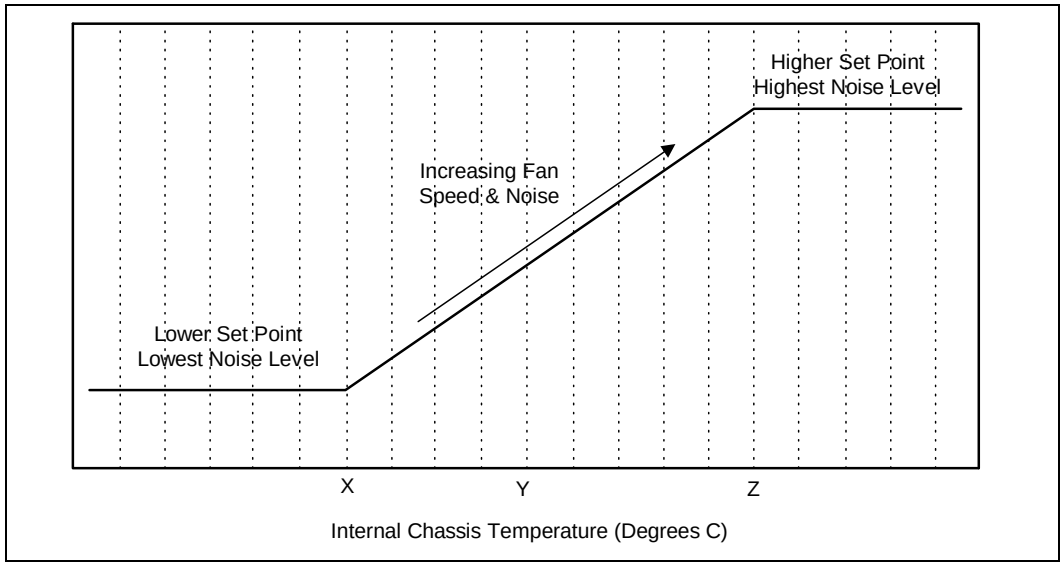


Table 7-2. Boxed Processor Fan Heatsink Set Points

Boxed Processor Fan Heatsink Set Point (ºC)	Boxed Processor Fan Speed	Notes
X ≤ 30 °C	When the internal chassis temperature is below or equal to this set point, the fan operates at its lowest speed. Recommended maximum internal chassis temperature for nominal operating environment.	1
Y = 34 °C	When the internal chassis temperature is at this point, the fan operates between its lowest and highest speeds. Recommended maximum internal chassis temperature for worst-case operating environment.	—
Z ≥ 38 °C	When the internal chassis temperature is above or equal to this set point, the fan operates at its highest speed.	1

NOTES:
1. Set point variance is approximately ±1°C from fan heatsink to fan heatsink.

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8 Debug Tools Specifications

Refer to the *ITP700 Debug Port Design Guide* for information regarding debug tools specifications. The *ITP700 Debug Port Design Guide* is located on http://developer.intel.com.

8.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Celeron D processor systems. Tektronix and Agilent should be contacted to obtain specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Celeron D processor systems, the LAI is critical in providing the ability to probe and capture FSB signals. There are two sets of considerations to keep in mind when designing a Celeron D processor system that can make use of an LAI: mechanical and electrical.

8.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the Celeron D processor. The LAI pins plug into the socket, while the Celeron D processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Celeron D processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the Celeron D processor heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

8.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the FSB; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

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