PRELIMINARY

Integrated Circuit Systems, Inc.

ICS83052I-01
2-BIT, 2:1, SINGLE-ENDED MULTIPLEXER

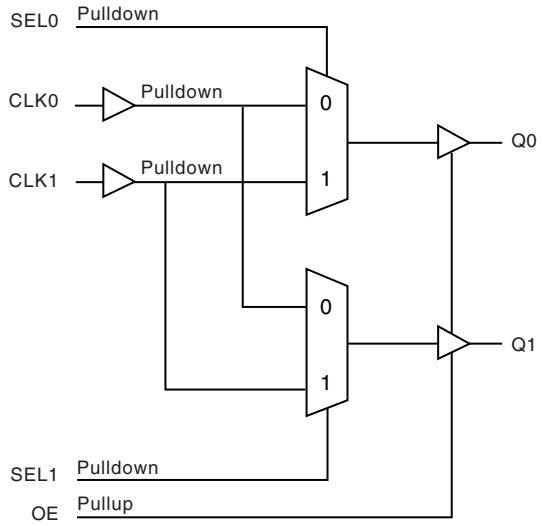
GENERAL DESCRIPTION

The ICS83052I-01 is a 2-bit, 2:1, Single-ended Multiplexer and a member of the HiPerClockS™family of High Performance Clock Solutions from ICS. The ICS83052I-01 has two selectable single-ended clock inputs and two single-ended clock outputs. The output has a V_{DDO} pin which may be set at 3.3V, 2.5V, or 1.8V, making the device ideal for use in voltage translation applications. An output enable pin places the output in a high impedance state which may be useful for testing or debug. Possible applications include systems with up to two transceivers which need to be independently set for different rates. For example, a board may have two transceivers, each of which need to be independently configured for 1 Gigabit Ethernet or 1 Gigabit Fibre Channel rates. Another possible application may require the ports to be independently set for FEC (Forward Error Correction) or non-FEC rates. The device operates up to 250MHz and is packaged in a 16 TSSOP.

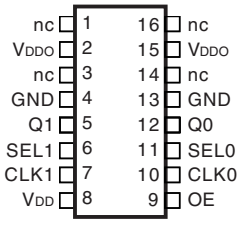
FEATURES

- 2-bit, 2:1 single-ended multiplexer
- Nominal output impedance: 15Ω (V_{DDO} = 3.3V)
- Maximum output frequency: 250MHz
- Propagation delay: 2.5ns (typical)
- Input skew: 45ps (typical)
- Part-to-part skew: TBD
- Additive phase jitter, RMS (12KHz - 20MHz): 0.07ps (typical)
- Operating supply modes:
  V_{DD}/V_{DDO}
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS83052I-01
16-Lead TSSOP
4.4mm x 3.0mm x 0.92mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 3, 14, 16	nc	Unused		No connect.
2, 15	V_{DDO}	Power		Output supply pins.
4, 13	GND	Power		Power supply ground.
5, 12	Q1, Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
6, 11	SEL1, SEL0	Input	Pulldown	Clock select inputs. See Control Input Function Table. LVCMOS / LVTTL interface levels.
7, 10	CLK1, CLK0	Input	Pulldown	Single-ended clock inputs. LVCMOS/LVTTL interface levels.
8	V_{DD}	Power		Core supply pin.
9	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)			11		pF
R_{OUT}	Output Impedance			15		Ω

TABLE 3. CONTROL INPUT FUNCTION TABLE

Control Inputs		Outputs	
SEL1	SEL0	Q1	Q0
0	0	CLK0	CLK0
0	1	CLK0	CLK1
1	0	CLK1	CLK0
1	1	CLK1	CLK1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5%, OR 2.5V±5%, OR 1.8V±0.2V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.6	1.8	2.0	V
I_{DD}	Power Supply Current			32		mA
I_{DDO}	Output Supply Current			4		mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 2.5V±5%, V_{DDO} = 2.5V±5%, OR 1.8V±0.2V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
			1.6	1.8	2.0	V
I_{DD}	Power Supply Current			30		mA
I_{DDO}	Output Supply Current			4		mA

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK0, CLK1	V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
		OE, SEL0, SEL1	V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK0, CLK1	V_{DD} = 3.3V ± 5%	-0.3		1.3	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
		OE, SEL0, SEL1	V_{DD} = 3.3V ± 5%	-0.3		1.3	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK1, SEL0, SEL1	V_{DD} = 3.3V or 2.5V ± 5%			150	µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, SEL0, SEL1	V_{DD} = 3.3V or 2.5V ± 5%	-5			µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%	-150			µA
V_{OH}	Output HighVoltage		V_{DDO} = 3.3V ± 5%; NOTE 1	2.6			V
			V_{DDO} = 2.5V ± 5%; NOTE 1	1.8			V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1	V_{DD} - 0.3			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1			0.5	V
			V_{DDO} = 2.5V ± 5%; NOTE 1			0.45	V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1			0.35	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 5A. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1			2.5		ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1			2.65		ns
*t*sk(i)	Input Skew; NOTE 5			45		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 5			TBD		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 4	Integration Range: 12KHz - 20MHz		0.07		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		535		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 3				5	ns
t_{DIS}	Output Disable Time; NOTE 3				5	ns
MUX_{ISOL}	MUX Isolation	@100MHz		45		dB

NOTE 1A: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: Driving only one input clock.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1			2.7		ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1			2.7		ns
*t*sk(i)	Input Skew; NOTE 5			38		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 5			TBD		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 4	Integration Range: 12KHz - 20MHz		0.04		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		550		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 3				5	ns
t_{DIS}	Output Disable Time; NOTE 3				5	ns
MUX_{ISOL}	MUX Isolation	@100MHz		45		dB

NOTE 1A: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: Driving only one input clock.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1			3		ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1			3		ns
*t*sk(i)	Input Skew; NOTE 5			38		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 5			TBD		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 4	Integration Range: 12KHz - 20MHz		0.05		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		595		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 3				5	ns
t_{DIS}	Output Disable Time; NOTE 3				5	ns
MUX_{ISOL}	MUX Isolation	@100MHz		45		dB

NOTE 1A: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: Driving only one input clock.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5D. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1			2.7		ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1			2.9		ns
*t*sk(i)	Input Skew; NOTE 5			45		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 5			TBD		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 4	Integration Range: 12KHz - 20MHz		0.10		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		540		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 3				5	ns
t_{DIS}	Output Disable Time; NOTE 3				5	ns
MUX_{ISOL}	MUX Isolation	@100MHz		45		dB

NOTE 1A: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: Driving only one input clock.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

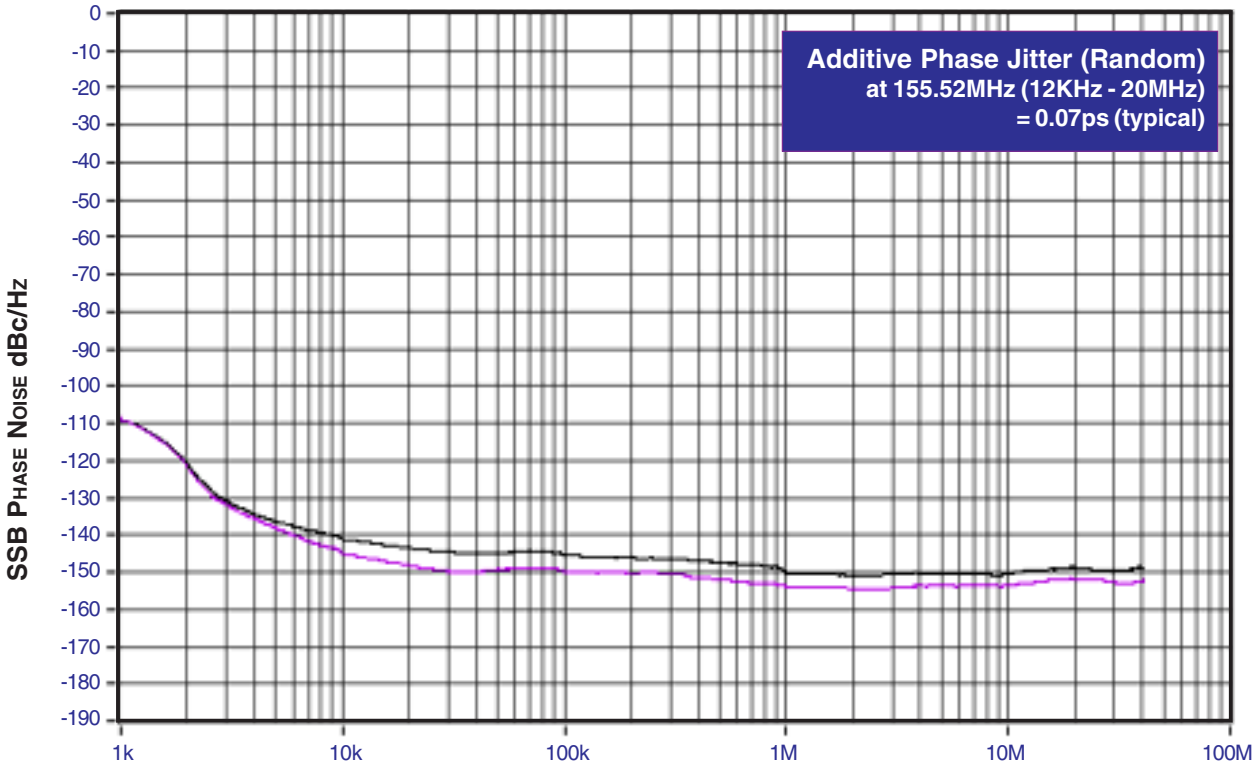
TABLE 5E. AC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm -0.2V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1			2.9		ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1			3		ns
*t*sk(i)	Input Skew; NOTE 5			43		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 5			TBD		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 4	Integration Range: 12KHz - 20MHz		0.07		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		590		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 3				5	ns
t_{DIS}	Output Disable Time; NOTE 3				5	ns
MUX_{ISOL}	MUX Isolation	@100MHz		45		dB

NOTE 1A: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: Driving only one input clock.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

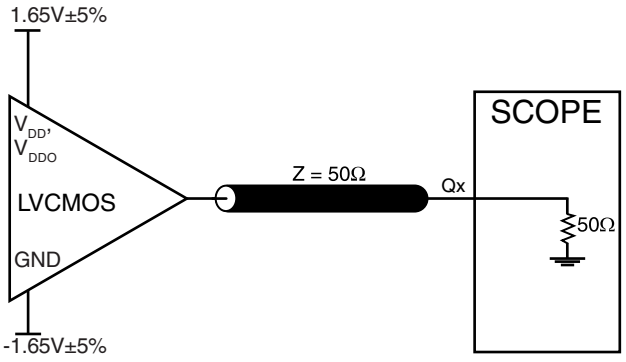
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

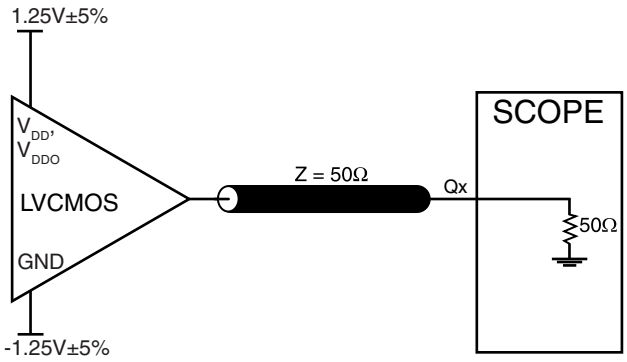


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

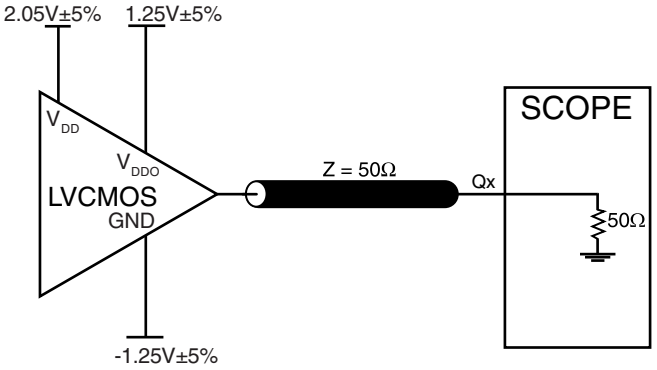
PARAMETER MEASUREMENT INFORMATION



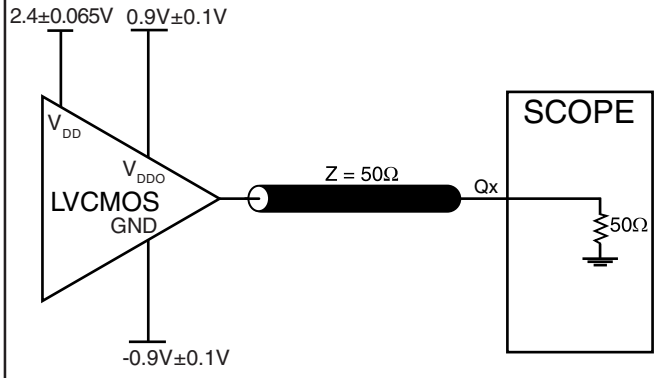
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



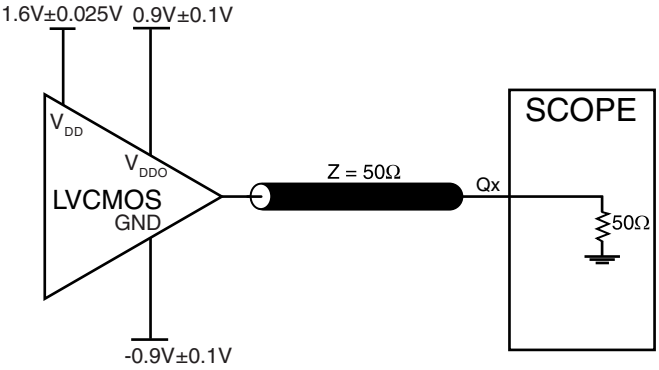
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



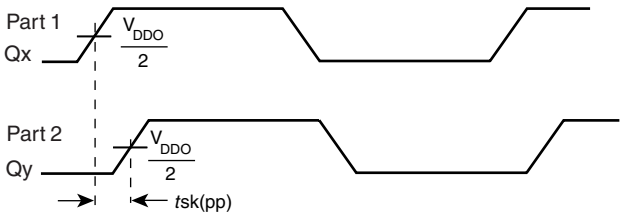
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



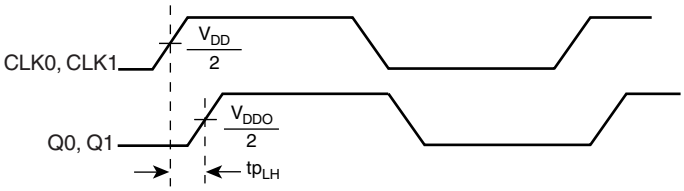
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



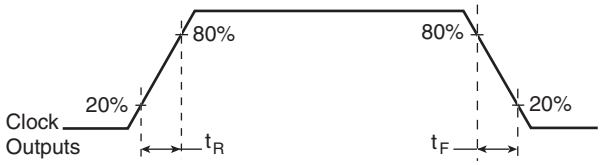
2.5 CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



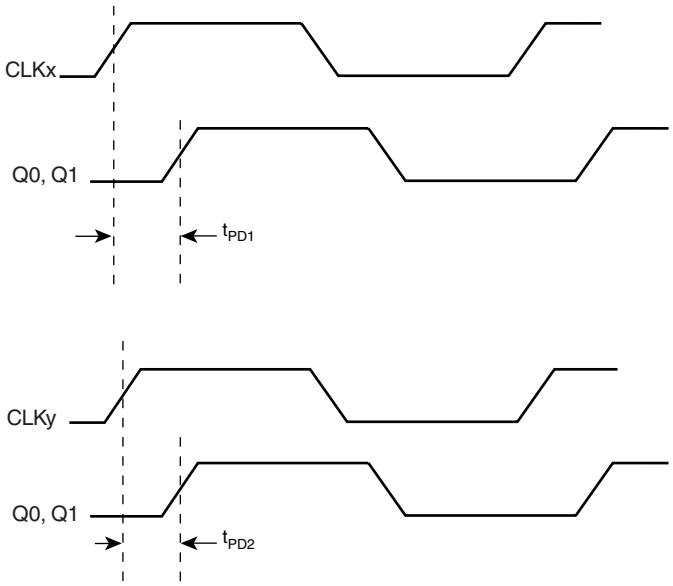
PART-TO-PART SKEW



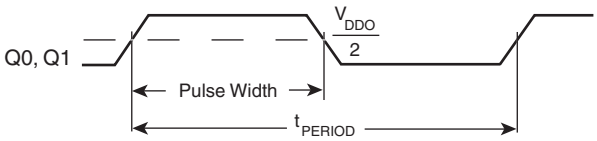
PROPAGATION DELAY



OUTPUT RISE/FALL TIME



INPUT SKEW



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83052I-01 is: 967

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

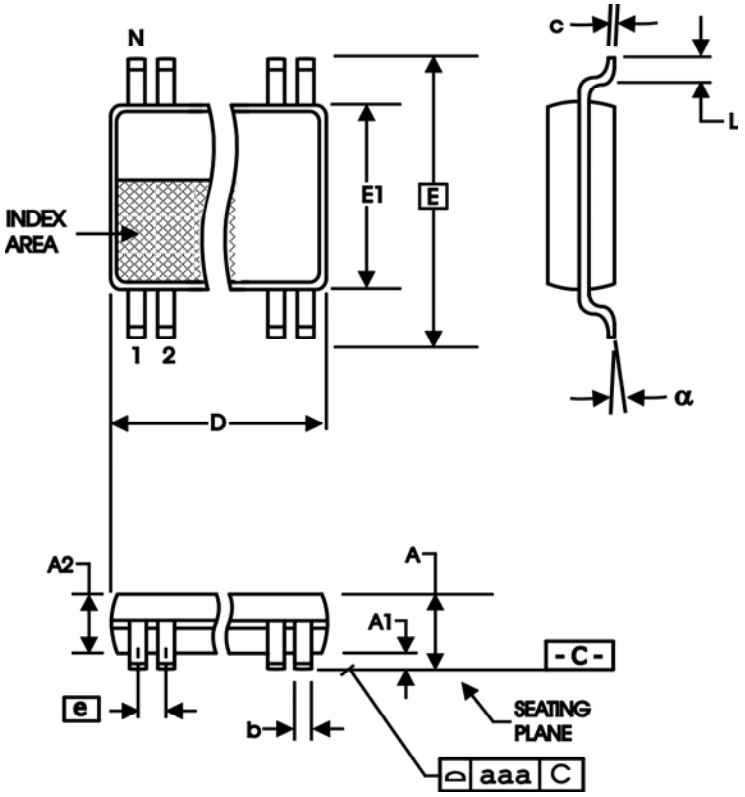


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83052AGI-01	3052AI01	16 Lead TSSOP	94 per tube	-40°C to 85°C
ICS83052AGI-01	3052AI01	16 Lead TSSOP on Tape and Reel	2500	-40°C to 85°C

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