2SK2800

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

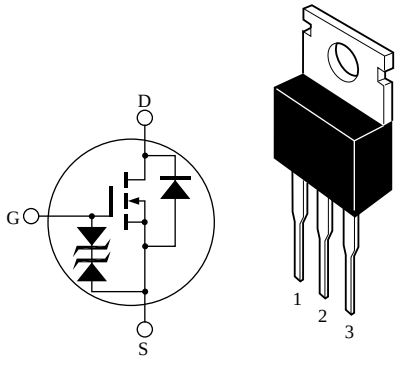
ADE-208-513G (Z)
8th. Edition
Jun 1998

Features

- Low on-resistance
  $R_{DS(on)}$ = 15 mΩ typ.
- High speed switching
- Low drive current
- 4V gate drive device can be driven from 5V source

Outline

TO–220AB



1. Gate
2. Drain (Flange)
3. Source

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$ Note1	160	A
Body-drain diode reverse drain current	I_{DR}	40	A
Avalanche current	I_{AP} Note 3	40	A
Avalanche energy	E_{AR} Note 3	137	mJ
Channel dissipation	Pch Note 2	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

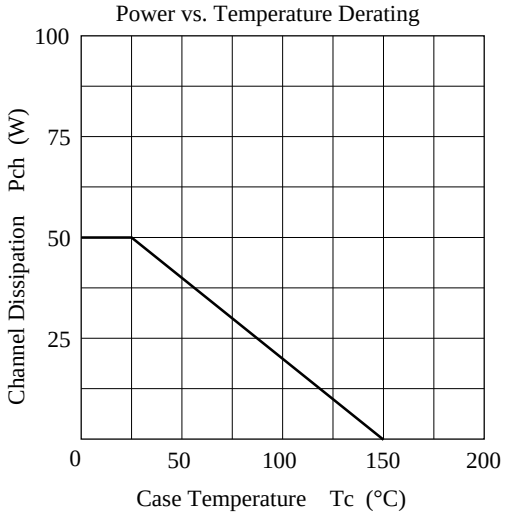
Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50Ω

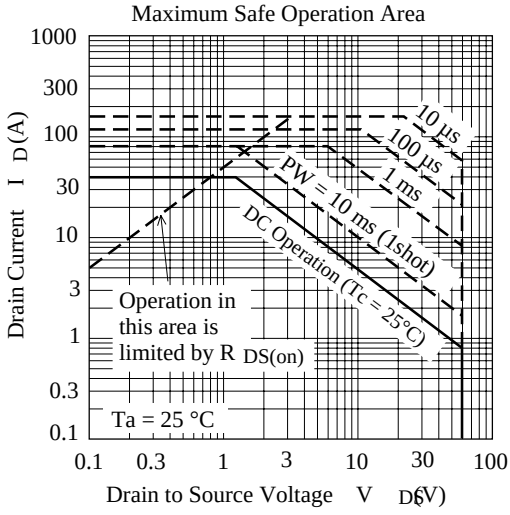
Electrical Characteristics (Ta = 25°C)

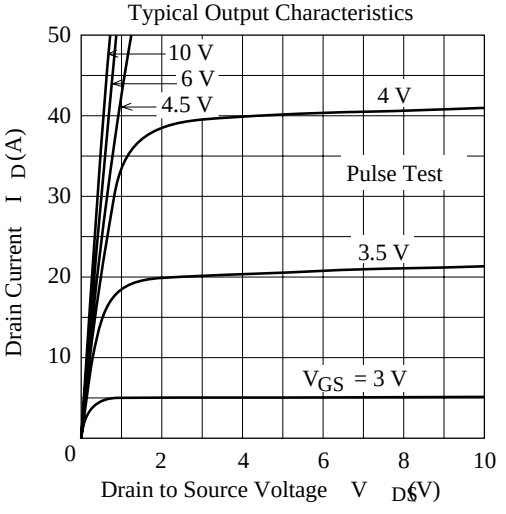
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±16V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	μA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	I_D = 1mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	15	20	mΩ	I_D = 20A, V_{GS} = 10V [Note4]
	$R_{DS(on)}$	—	25	40	mΩ	I_D = 20A, V_{GS} = 4V [Note4]
Forward transfer admittance	$\|y_{fs}\|$	20	35	—	S	I_D = 20A, V_{DS} = 10V [Note4]
Input capacitance	Ciss	—	1500	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	720	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	200	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	I_D = 20A, R_L = 1.5Ω
Rise time	t_r	—	180	—	ns	V_{GS} = 10V
Turn-off delay time	$t_{d(off)}$	—	200	—	ns	
Fall time	t_f	—	200	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = 40A, VGS = 0
Body–drain diode reverse recovery time	t_{rr}	—	70	—	V	I_F = 40A, VGS = 0 diF/ dt =50A/μs

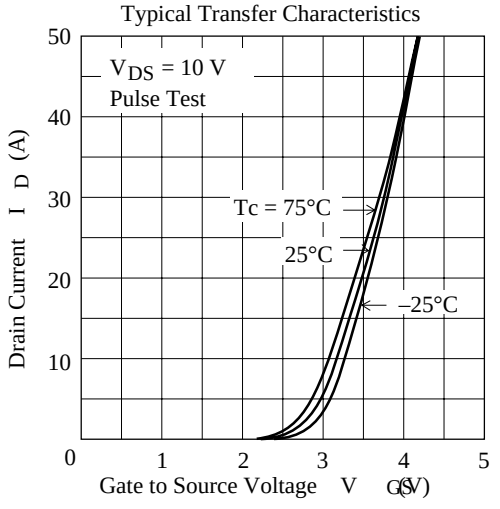
Note: 4. Pulse test

Main Characteristics

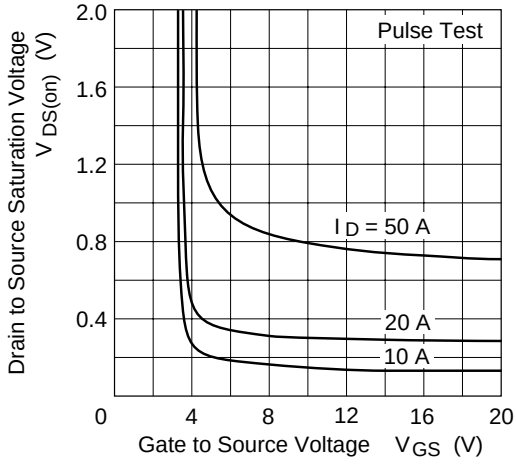




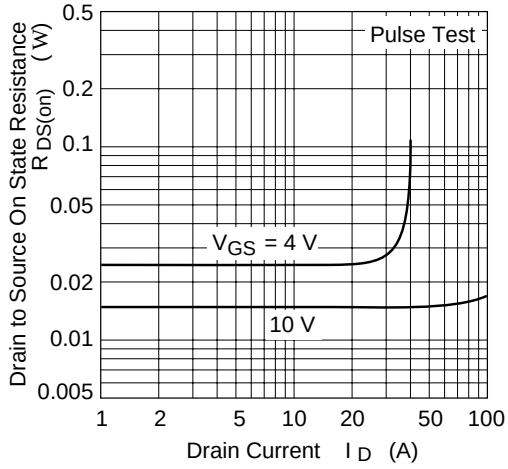




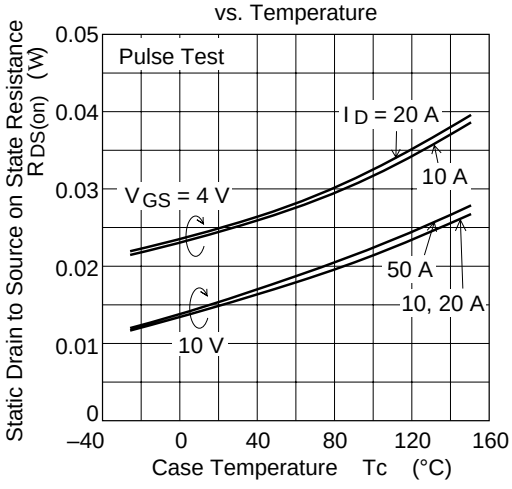
Drain to Source Saturation Voltage vs. Gate to Source Voltage



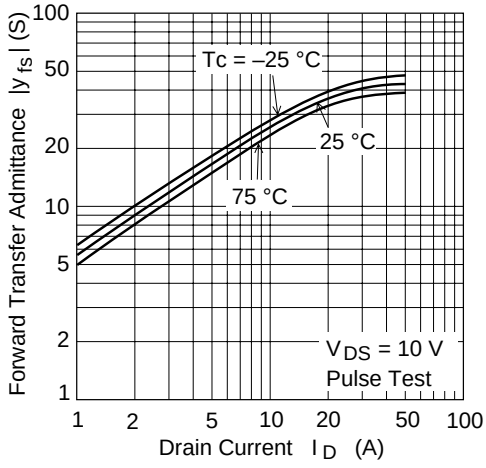
Static Drain to Source on State Resistance vs. Drain Current

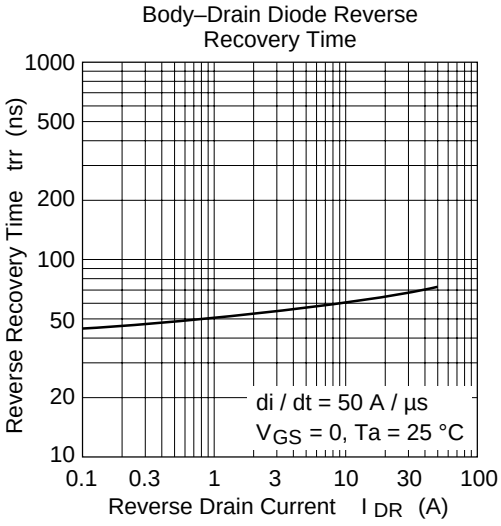


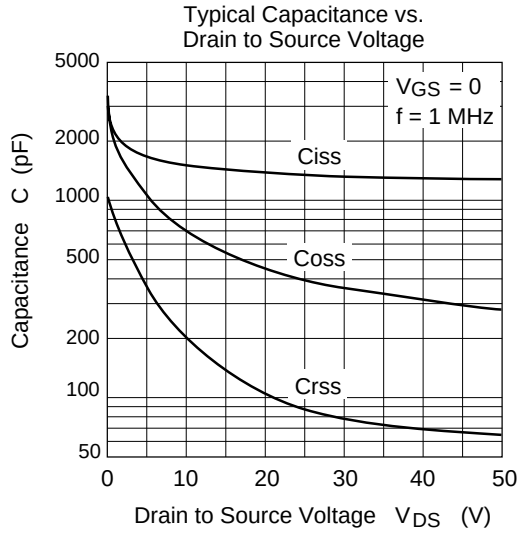
Static Drain to Source on State Resistance vs. Temperature

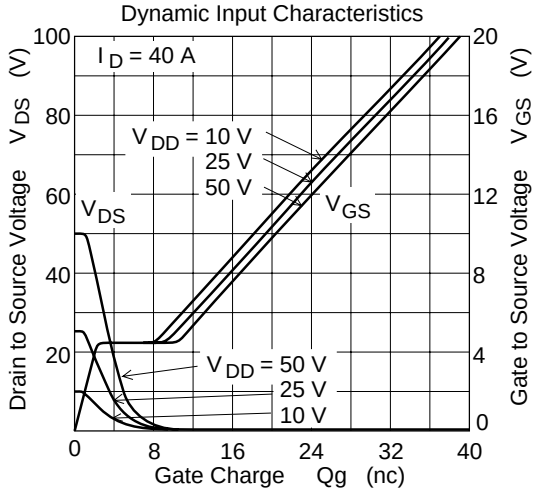


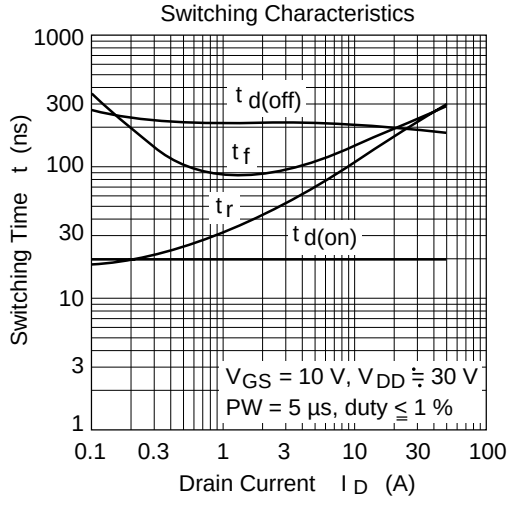
Forward Transfer Admittance vs. Drain Current



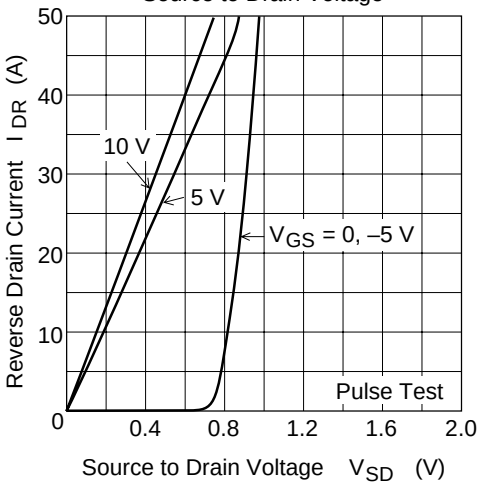

Body–Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
500
200
100
50
20
10
0.1
0.3
1
3
10
30
100
Reverse Drain Current I DR (A)
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
5000
2000
1000
500
200
100
50
0
10
20
30
40
50
Drain to Source Voltage VDS (V)
VGS = 0
f = 1 MHz
Ciss
Coss
Crss

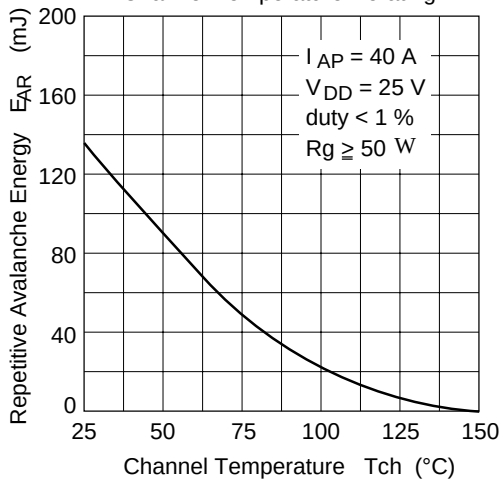

Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
100
80
60
40
20
Gate to Source Voltage VGS (V)
20
16
12
8
4
0
0
8
16
24
32
40
Gate Charge Qg (nc)
I D = 40 A
V DD = 10 V
25 V
50 V
VDS
VGS
V DD = 50 V
25 V
10 V


Switching Characteristics
Switching Time t (ns)
1000
300
100
30
10
3
1
0.1
0.3
1
3
10
30
100
Drain Current I D (A)
t d(off)
t f
t r
t d(on)
VGS = 10 V, V DD = 30 V
PW = 5 µs, duty ≦ 1 %

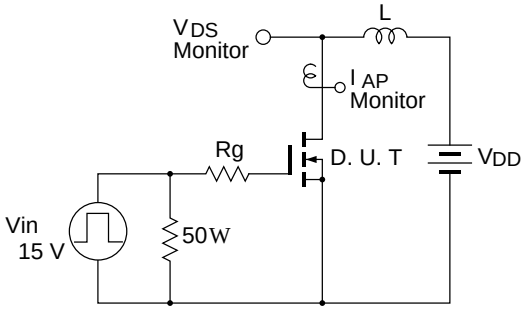
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

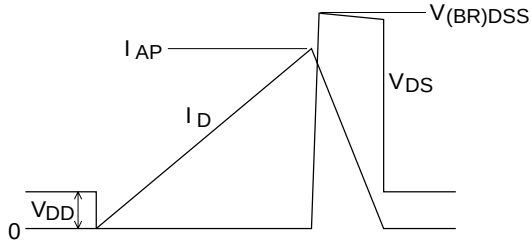


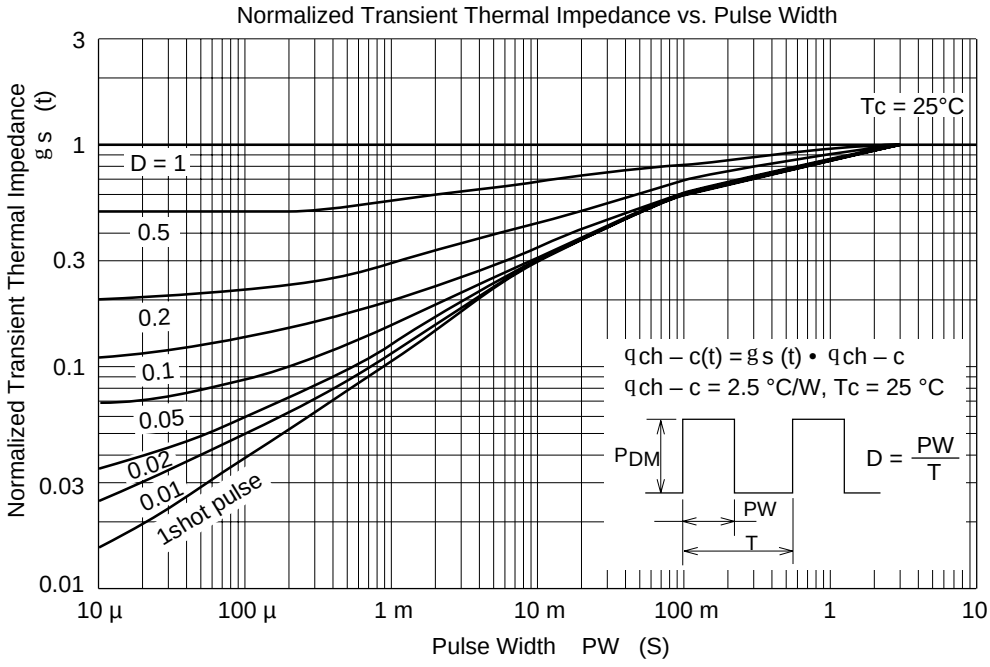
Avalanche Test Circuit



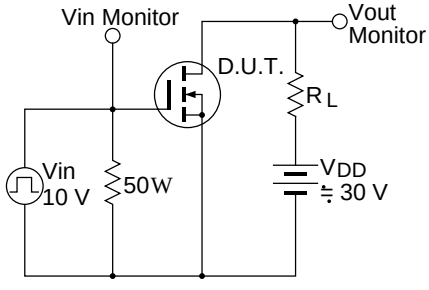
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

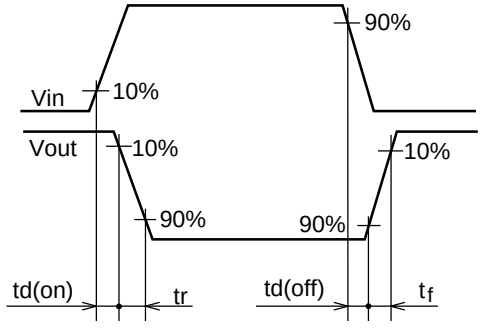




Switching Time Test Circuit

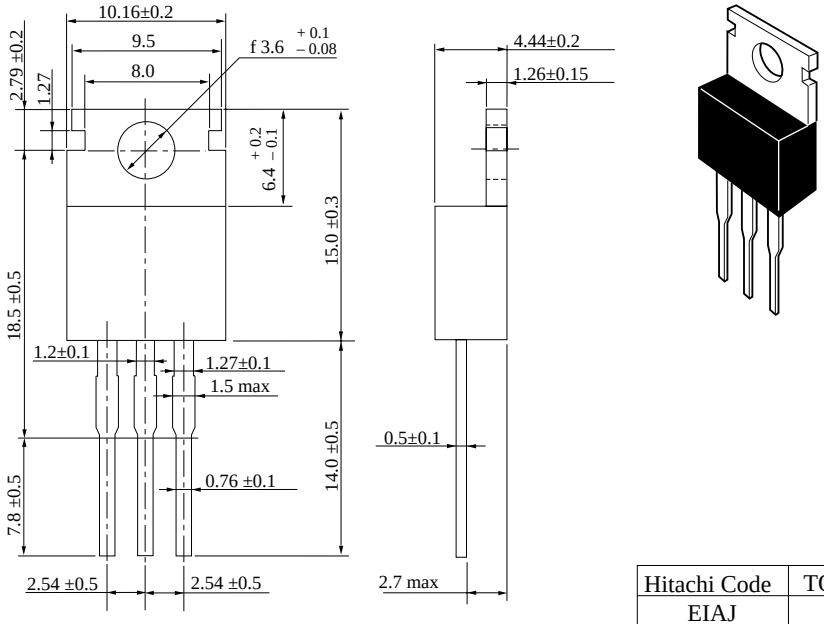


Waveform



Package Dimensions

Unit: mm



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